16th "TRENTO" WORKSHOP ON ADVANCED SILICON RADIATION DETECTORS

Bi-layered CMOS SPADs with coincidence-based DCR rejection for charged particle detection

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16 – 18 February 2021

Summary

- Single Photon Avalanche Diode
- ASAP project
- Chip floorplan
- Characterization results
- Conclusion

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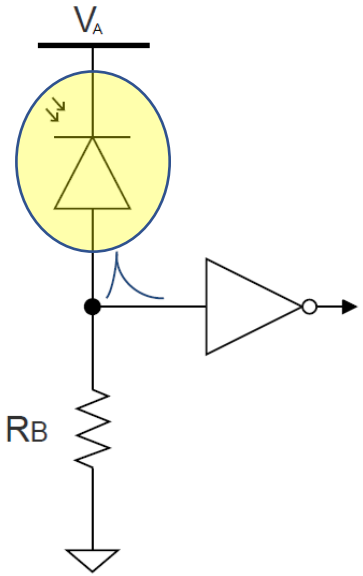
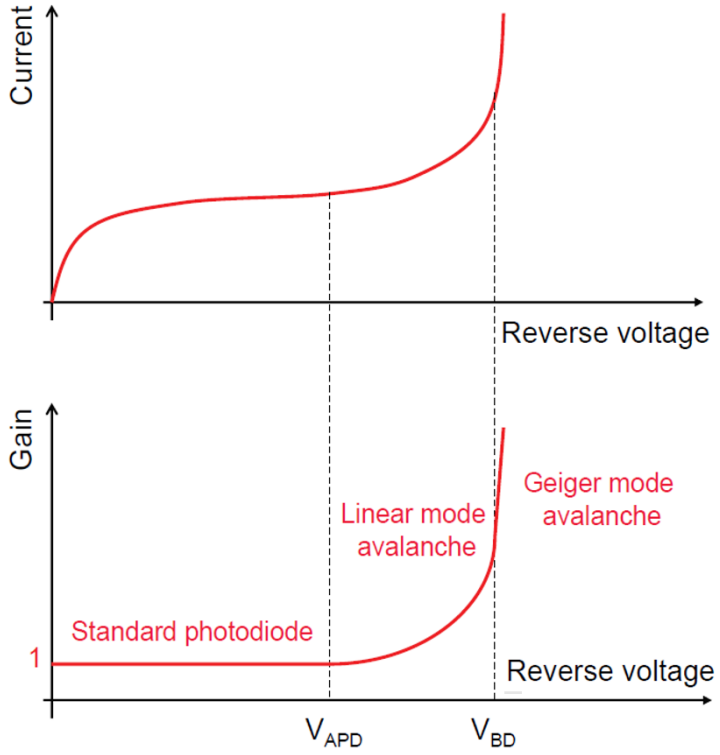
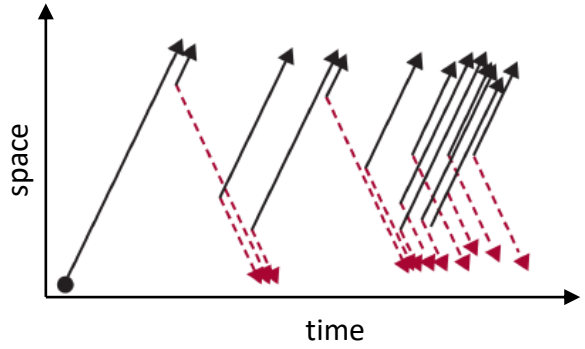
Single Photon Avalanche Diode



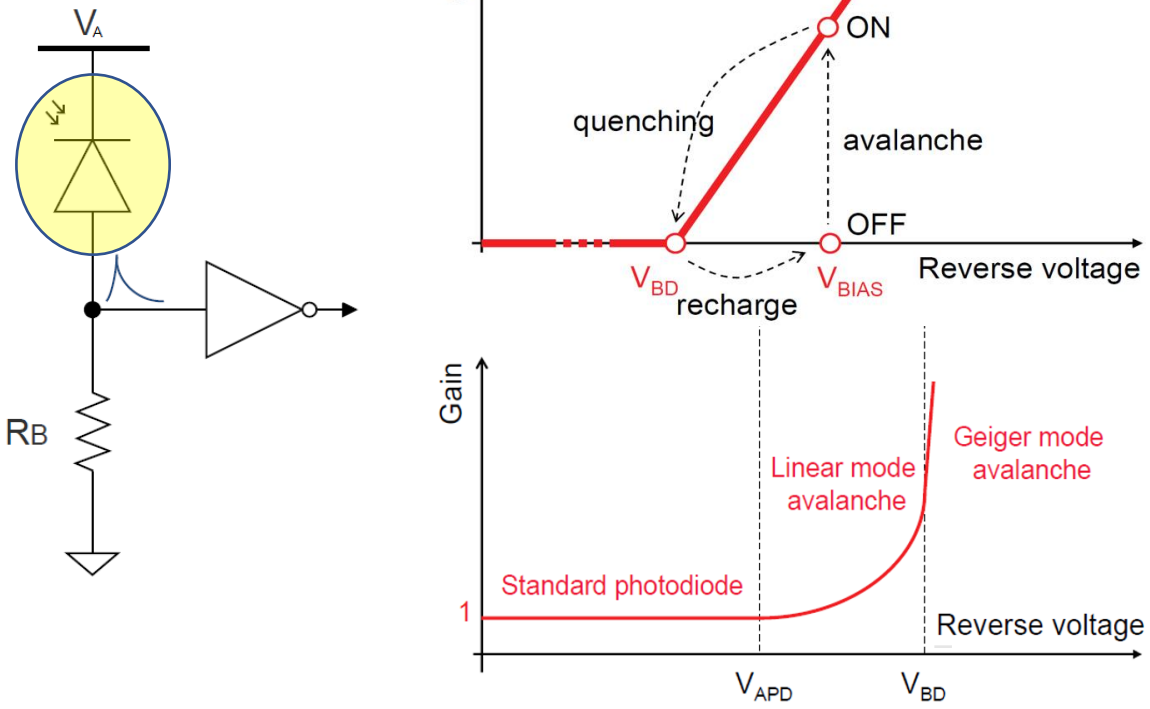


SPADs are photodiodes, biased to work in Geiger mode, offering:

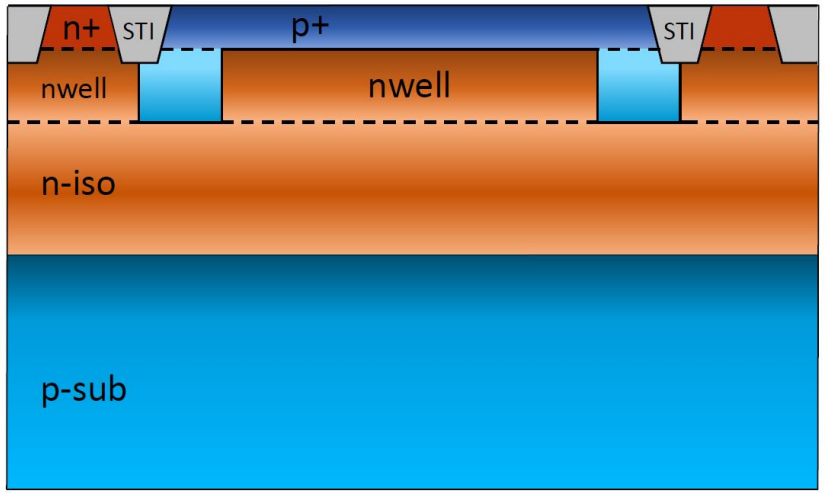
- large intrinsic **gain**, enabling single photon detection;
- no need for **preamplification**;
- **thin** sensitive layer;
- compatibility with standard **CMOS** process.



Single Photon Avalanche Diode

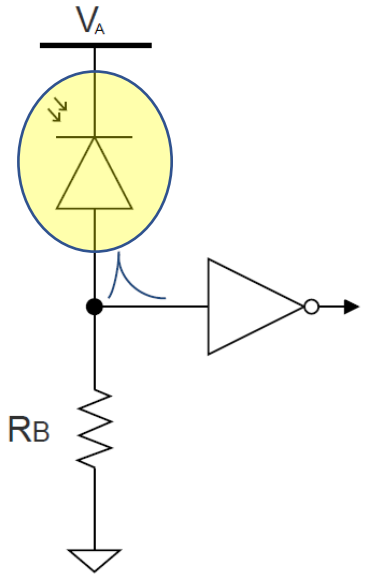


Junction of choice: **p+/n-well junction**, Better performance in terms of crosstalk effect as compared to p-well/deep n-well.



- Pancheri L. et al. First prototypes of two-tier avalanche pixel sensors for particle detection. Nucl Instrum Methods (2017)

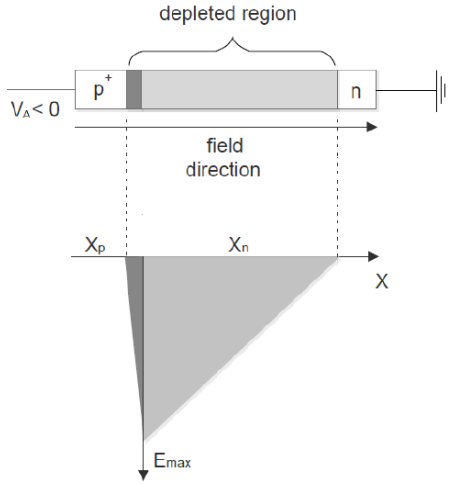
Single Photon Avalanche Diode



An important feature of SPADs is their noise performance, expressed in terms of **Dark Count Rate [Hz]**.

Possible reasons for dark pulses:

- trap-assisted **thermal generation** of carriers in the depletion region;
- **band to band tunneling**;
- thermal generation of **minority carriers** in the bulk **diffusing** to the active region (negligible);
- **afterpulsing**;
- **crosstalk** (at array level).



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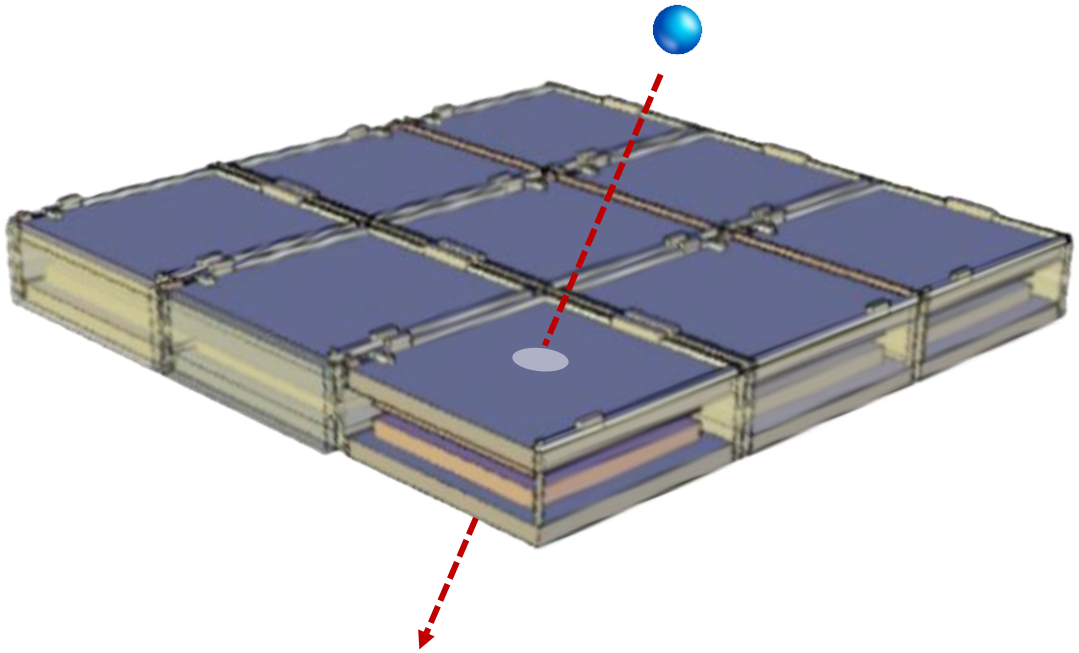
Asap project

Goal of the project: develop a new generation of layered avalanche detectors for ***charged particles***

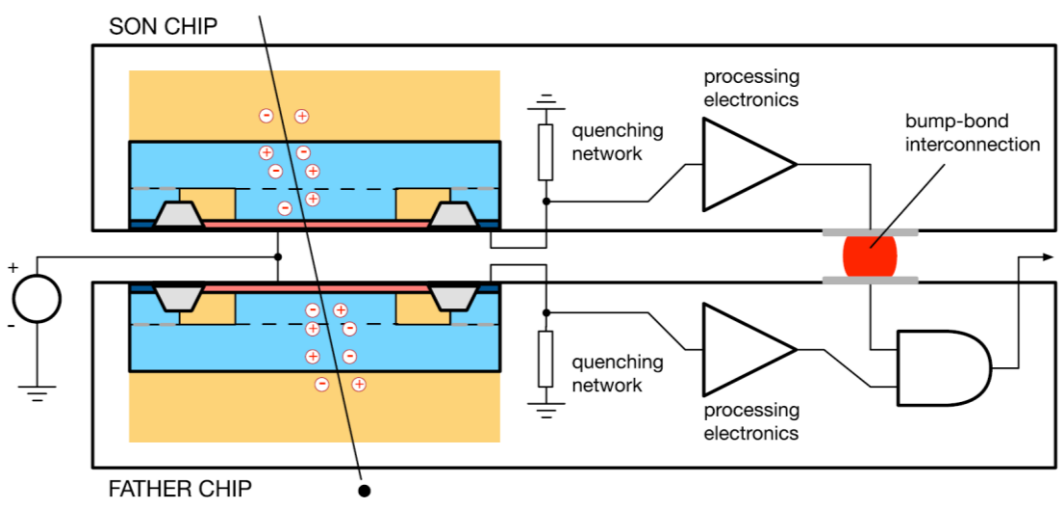
Leveraging: process scaling, thinning technology, monolithic integration, tridimensional approach

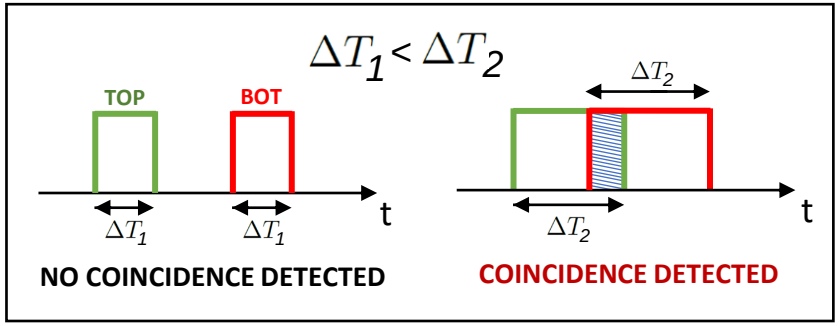
Pursuing: reduced sensor noise, reduced material budget



Asap project

- If a particle **simultaneously** strikes the overlapping SPADs, a coincidence signal with a programmable duration is produced.
- Noise contribution from the single diodes is **strongly mitigated**, since a "simultaneous" dark pulse from both the SPADs is **highly unlikely**.

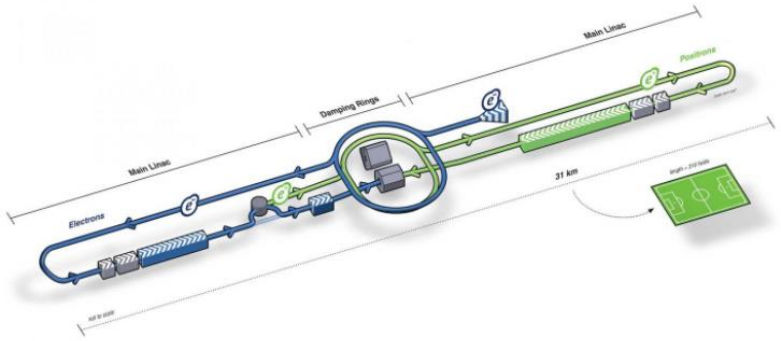




$$DCR_C = 2(\Delta T) \times DCR_T \times DCR_B$$

Asap project

- Charged particle **tracking in low rate environments**;
- **Medical application**: Employ single particle resolution and low noise of a dual tier structure to design a compact imaging probe for radio-guided surgery with β emitters.



➢ https://home.cern/news/news/accelerators/international-linear-collider-ready-construction

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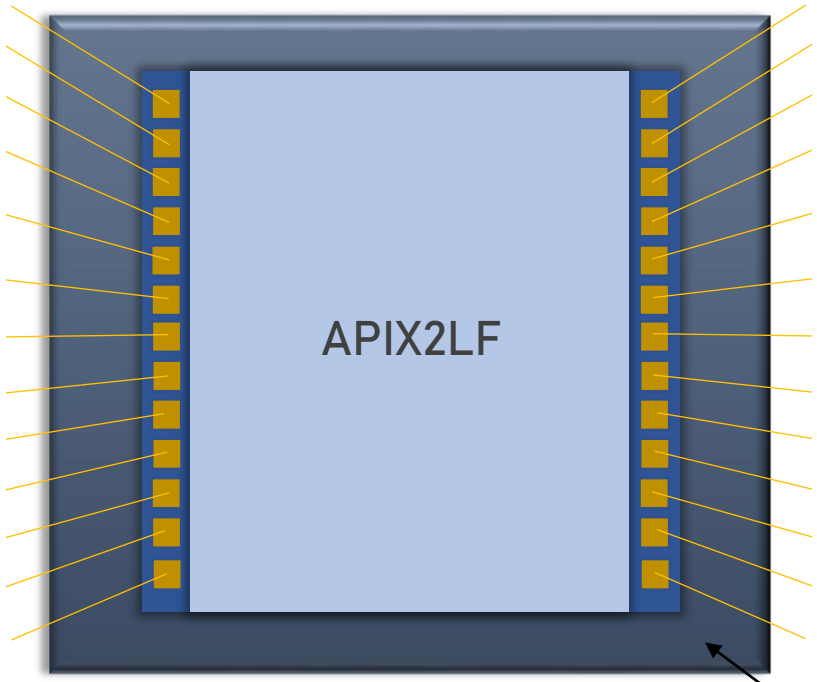
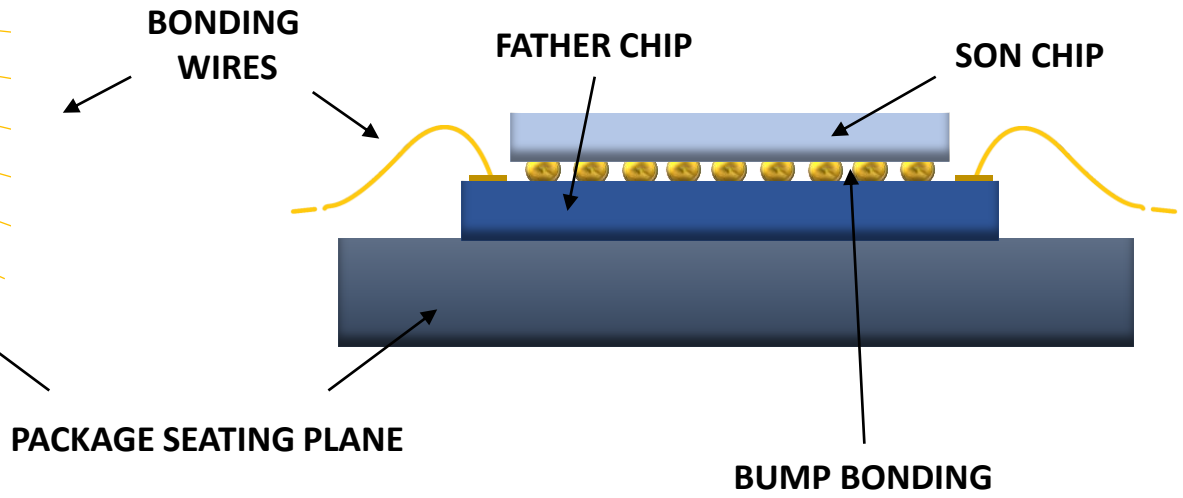
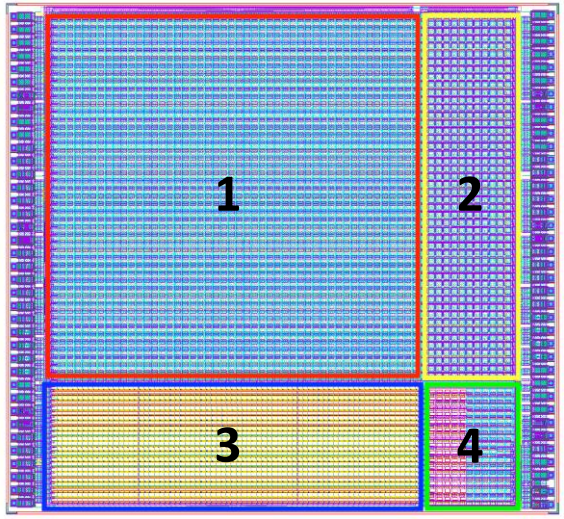
Chip floorplan



- **APIX2LF** was fabricated in **CMOS 150 nm** technology.
- The son chip is read out in coincidence and stimulated through the **bump bonded** father layer

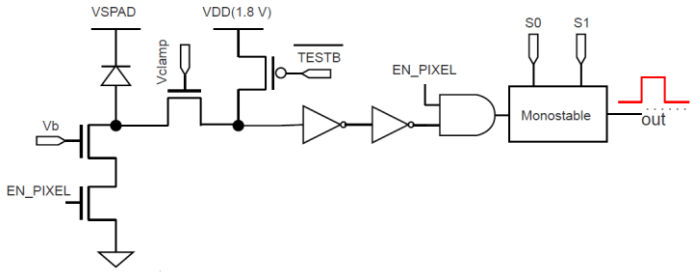


Chip floorplan

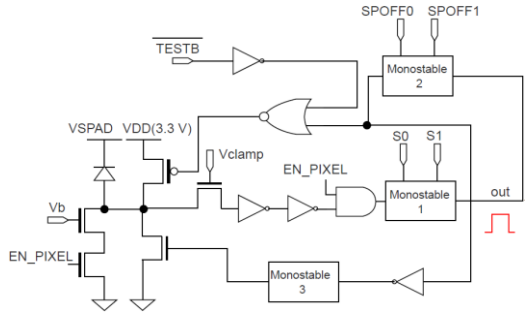


Four SPAD arrays:

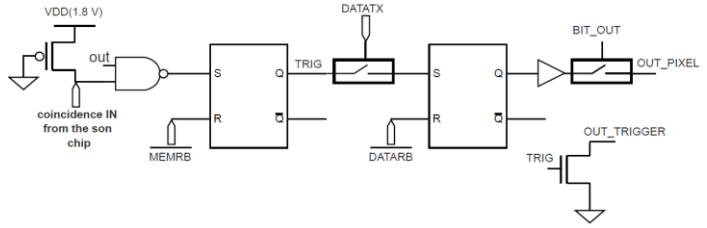
- **Array 1**: 48×48 pixels, pitch of 75 μm, SPAD active area of 70×52 μm^2, FF of 65%, passive quenching, 1-bit memory;
- **Array 2**: 48×12 pixels, pitch of 75 μm, SPAD active area of 47×57 μm^2, passive quenching, 10-bit pulse counter;
- **Array 3**: 24×72 pixels, pitch of 50 μm, SPAD active area of 44×24 μm^2, FF of 42%, passive quenching, 1-bit memory;
- **Array 4**: 7×6 pixels, pitch of 75 μm, SPAD active area of 70×42 μm^2, with active quenching.



Front end with passive quenching

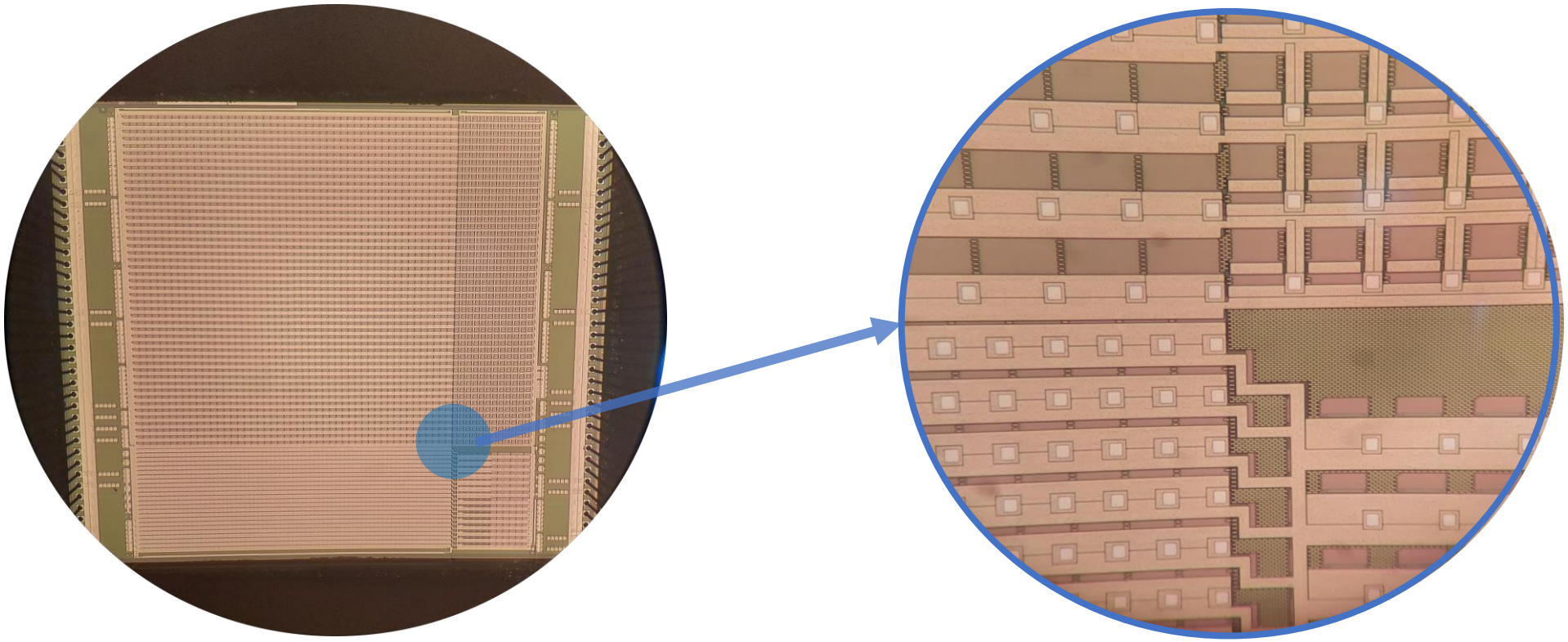


Front end with active quenching



1-bit memory

Chip floorplan



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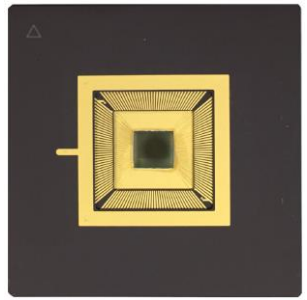
Characterization results

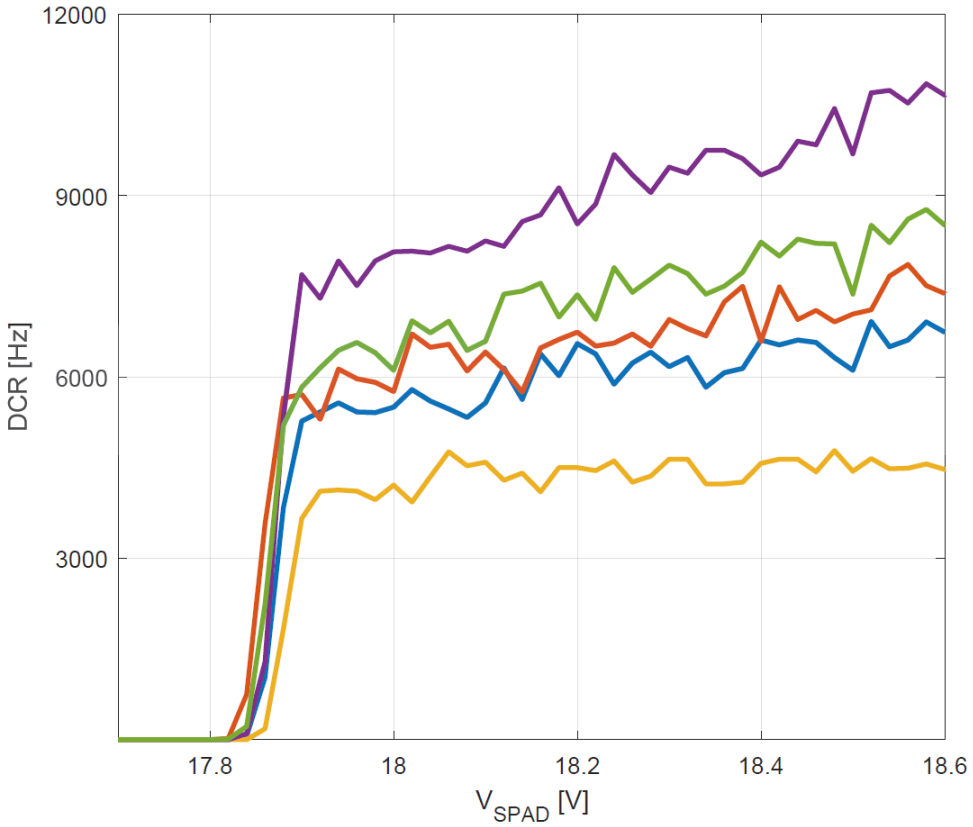
- **DCR** in different operating conditions, **Breakdown voltage**, **Crosstalk**.
- **Chips** involved in the characterization:
  - father (2 samples) and son (1 sample) chips tested separately;
    - ↳ Total Integration Time for a pixel DCR measurement (TIT): 100 ms.
  - dual tier chips (2 samples);
    - ↳ Total Integration Time for a pixel DCR measurement (TIT): 30 s / 300s.
- **Arrays** involved in the characterization:
  - array 1 (a1);
  - array 3 (a3);
  - array 4 – active quenching section (a4).
- Temperature of **25 °C ± 0.5 °C**.
- Microcontroller based **characterization setup** composed by a number of carrier boards, a single motherboard and a bluetooth module managed through MATLAB scripts.



Electronic Instrumentation Laboratory

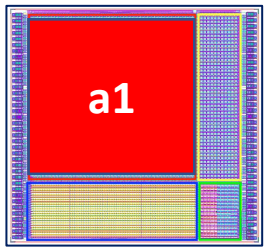
Characterization results

DCR vs V_{SPAD}
5 pixels



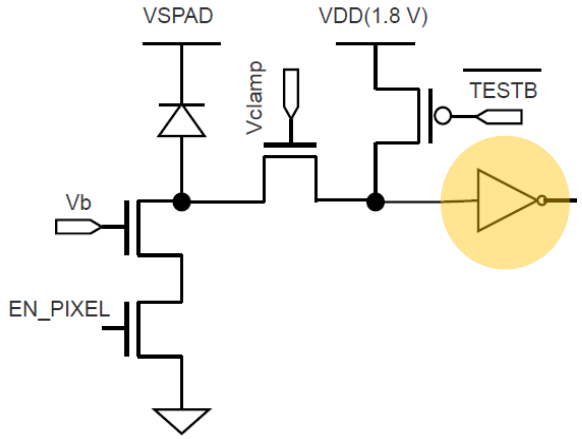
48×48 pixels
A.A.: 70×52 μm^2
PITCH : 75 μm

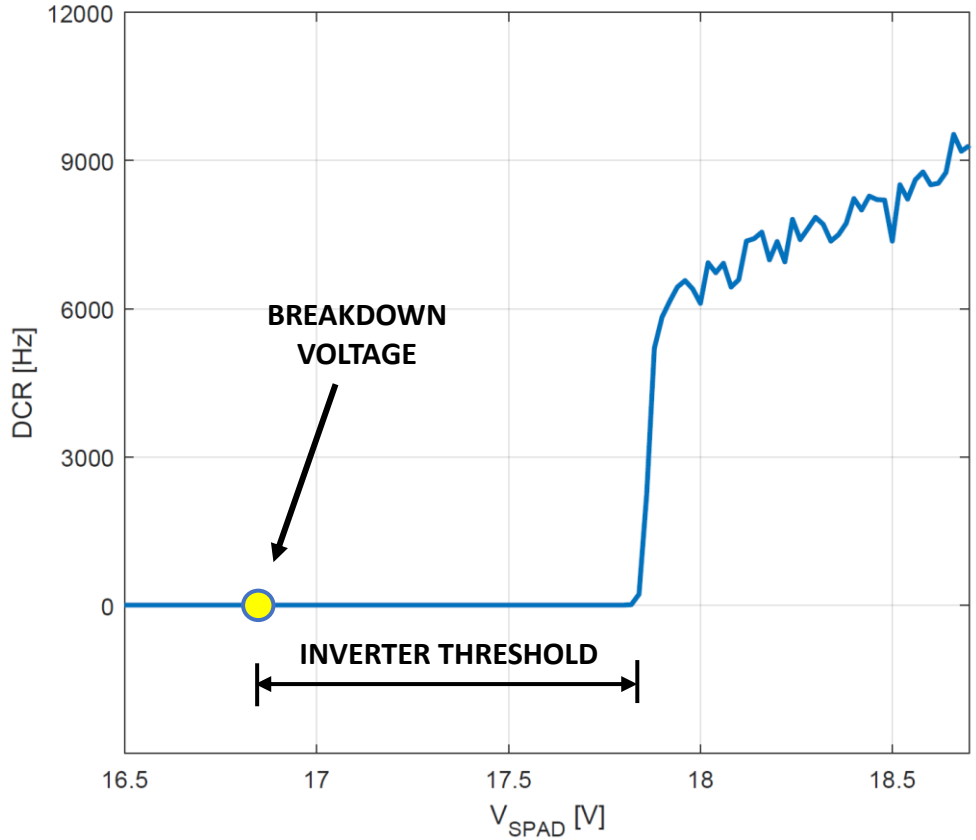
FATHER



Characterization results

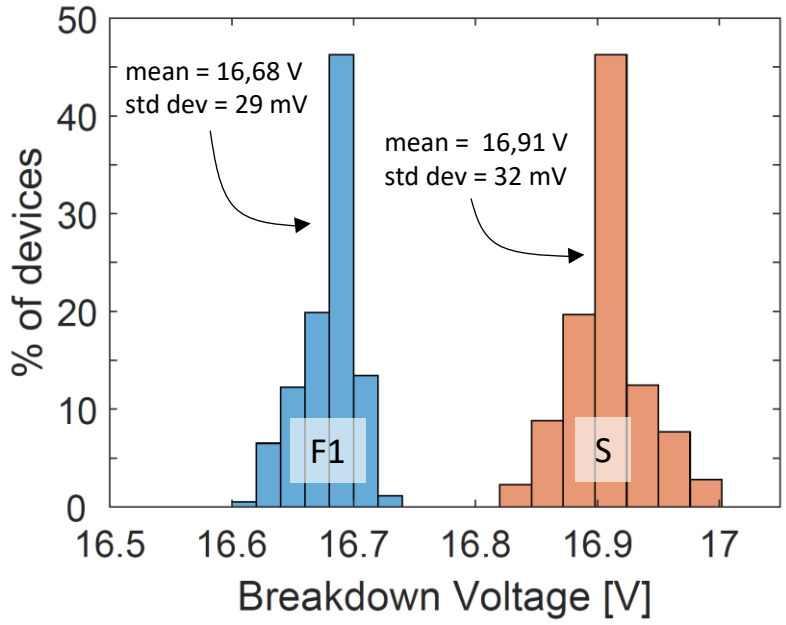
Breakdown voltage extraction using the front-end inverter switching threshold (~ 1 V)

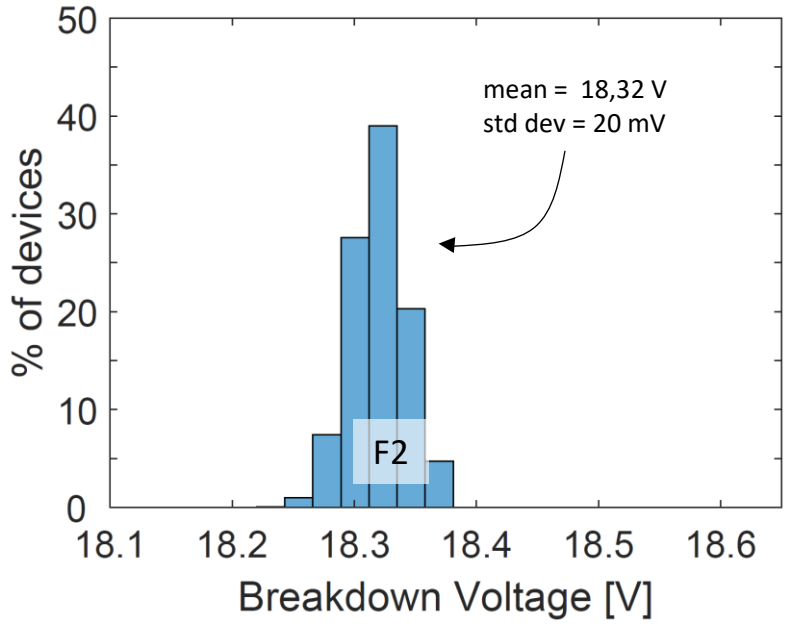




Characterization results

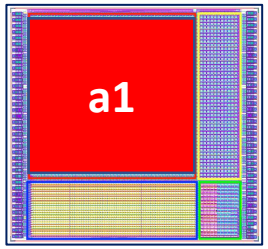
Breakdown voltages ranging between **16,6 V** and **18,4 V** were found for different DUTs but **much smaller variations** were detected among different SPADs **in the same array**.





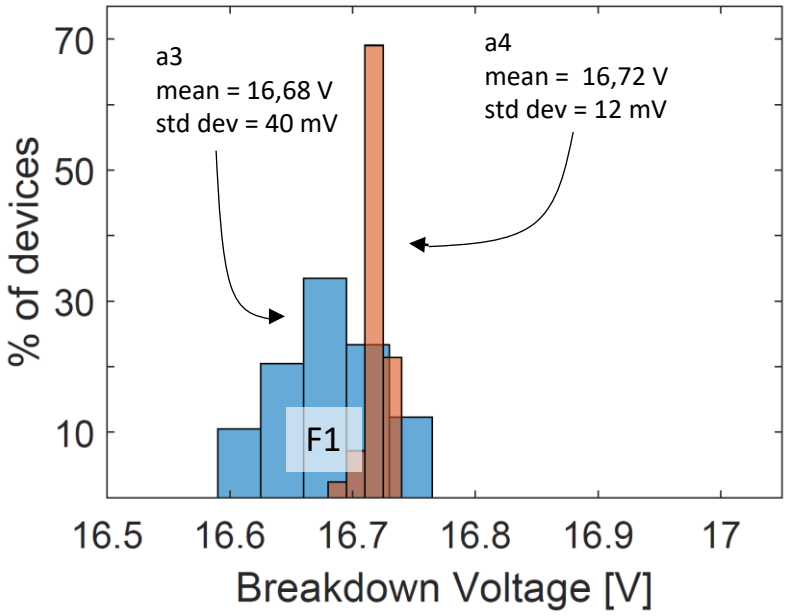
48×48 pixels
A.A.: 70×52 μm^2
PITCH : 75 μm

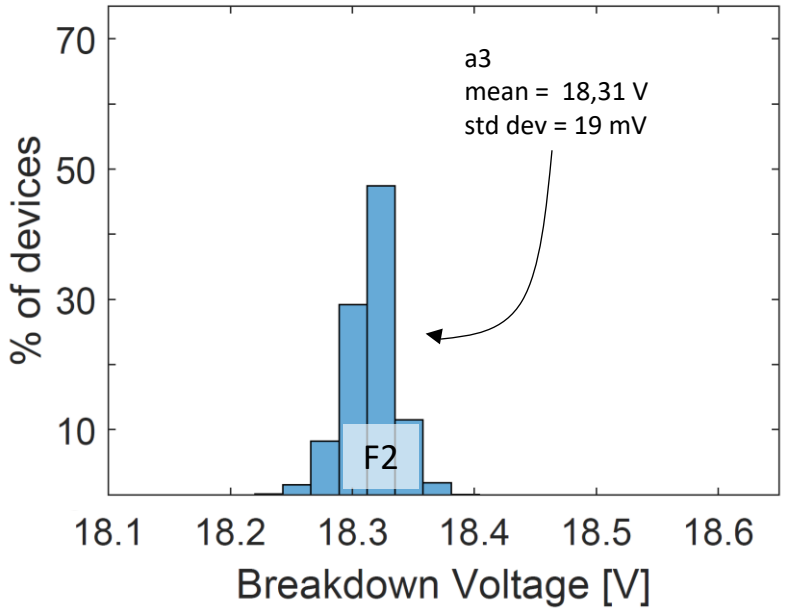
FATHER/SON



Characterization results

Breakdown voltages ranging between **16,6 V** and **18,4 V** were found for different DUTs but **much smaller variations** were detected among different SPADs **in the same array** and different arrays **in the same chip**.

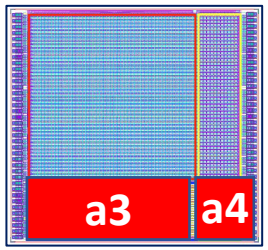




a3: 24×72 pixels
A.A.: 44×24 μm^2
PITCH : 50 μm

a4: 7×6 pixels
A.A.: 70×40 μm^2
PITCH : 75 μm

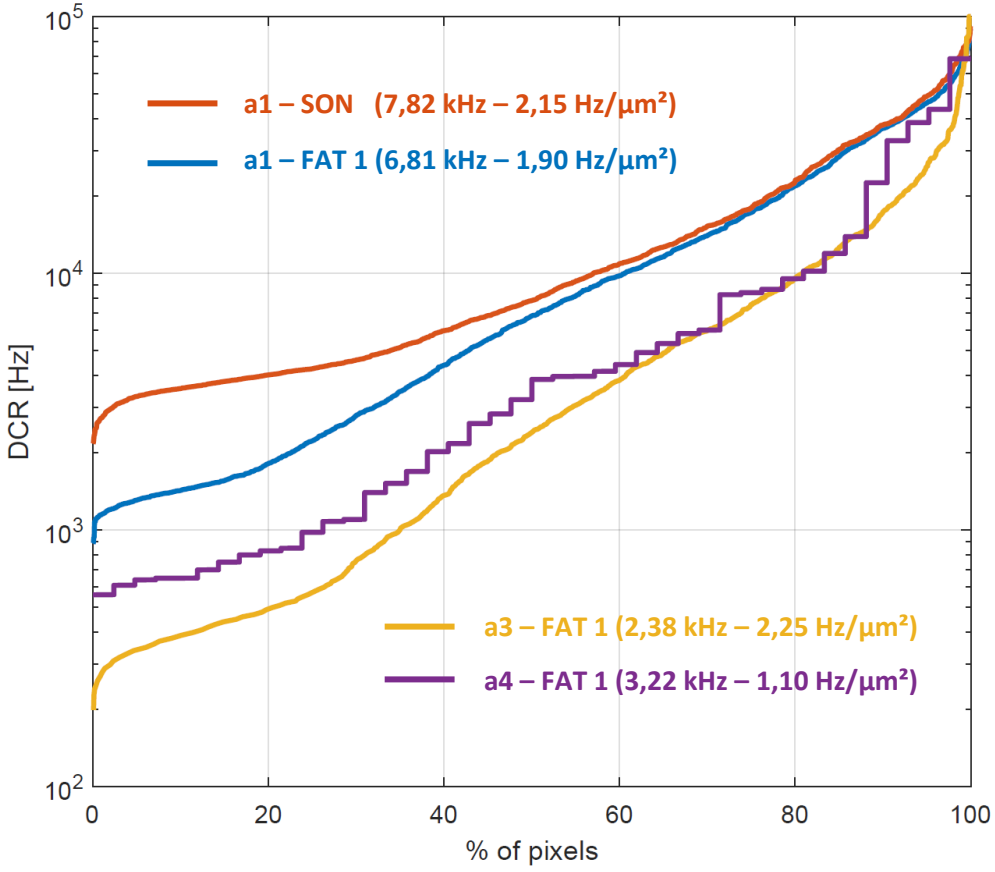
FATHER



Characterization results

DCR CUMULATIVE DISTRIBUTION

- For all the curves, DCR was measured with an **excess voltage** of 1,7 V.
- A **hold-off time** equal to 70 ns was chosen for SPADs in a4.



Characterization results

DCR DUAL LAYER CHIP: ESTIMATED vs MEASURED

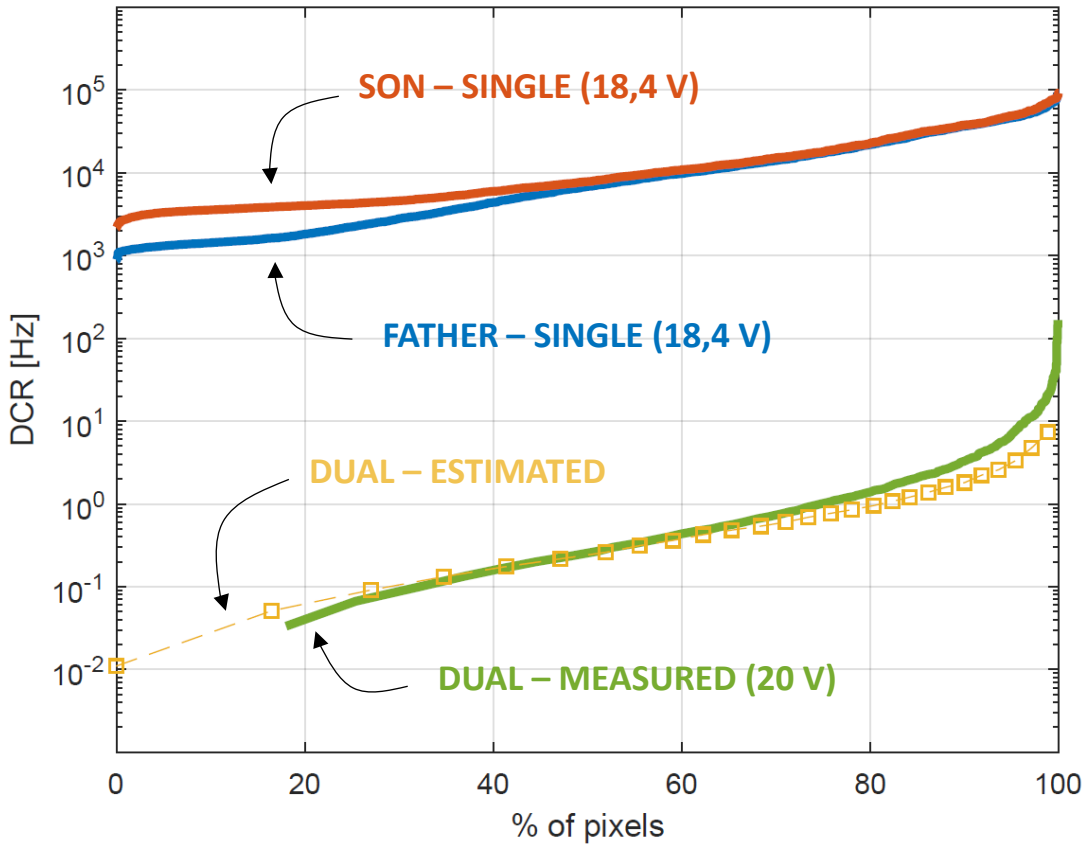
For the median values:

$$DCR_C = 2(\Delta T) \times DCR_T \times DCR_B$$

$$\mathbf{0,21\ Hz} = (4 \cdot 10^{-9} \times \ 7820 \ \times \ 6810)\ Hz$$

Measured DCR is **consistent** with the estimated one

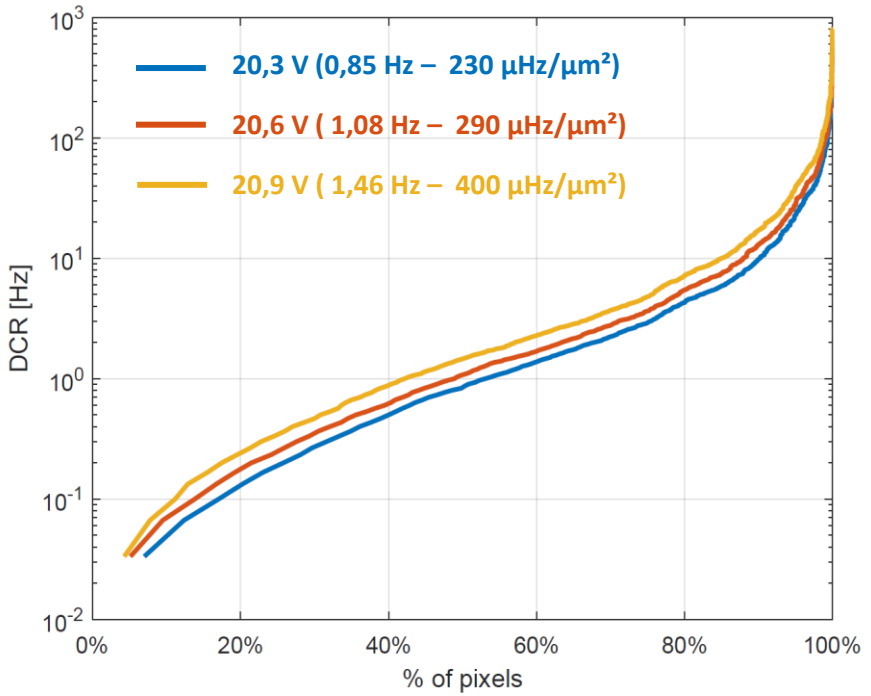
NOTE: for this measurement $V_{BD,DUAL} \neq V_{BD,SINGLE}$



Characterization results

DUAL LAYER DCR MEASUREMENT

- **Coincidence window** = 2 ns
- A **TIT** equal to 30 s was chosen to contain measurement time → some pixels were **non-responsive** because featuring a DCR smaller than 33 mHz



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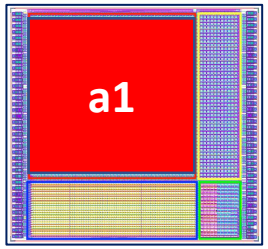
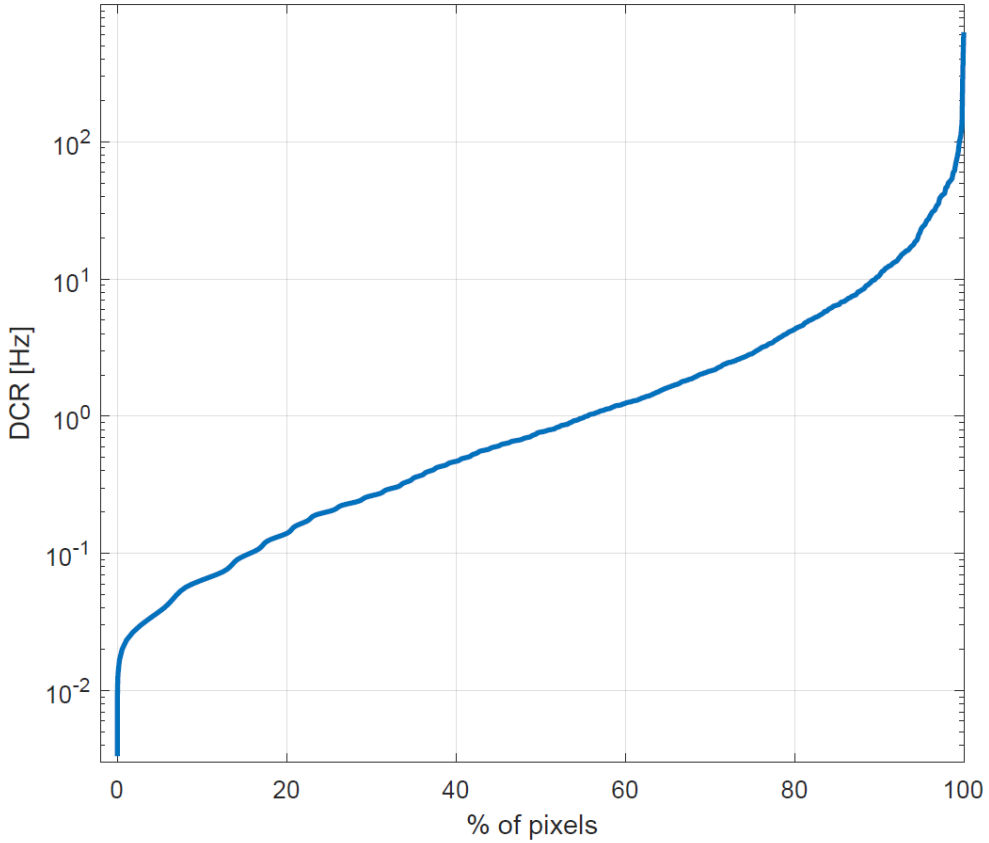
DUAL



Characterization results

DCR MEASUREMENT AT LONGER TOTAL INTEGRATION TIME (300 s)

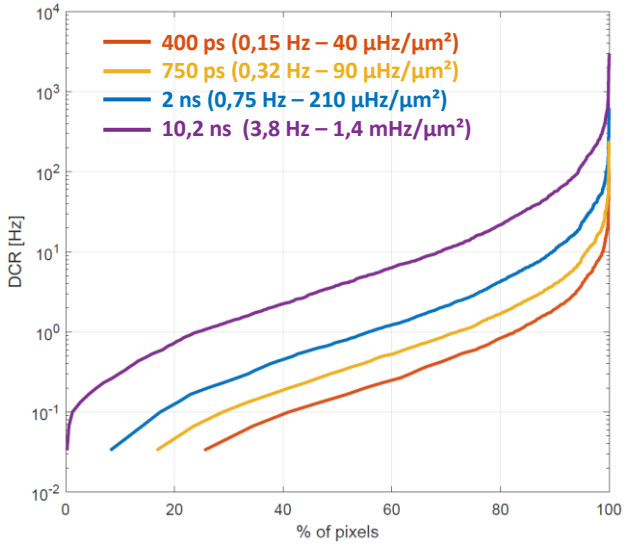


Characterization results

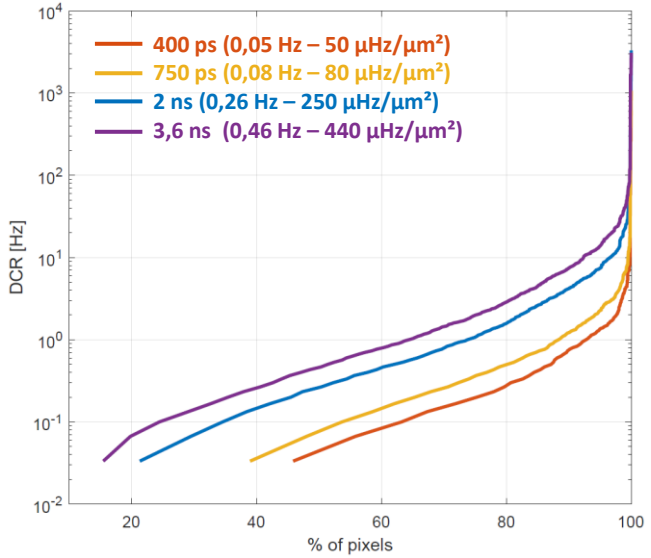
DCR MEASUREMENTS AT DIFFERENT COINCIDENCE WINDOWS

- **Bias voltage** = 21 V, **quenching voltage** = 900 mV.
- The duration of the coincidence window, set in **transparent mode**, was simulated considering different capacitance values for SPADs in different arrays.

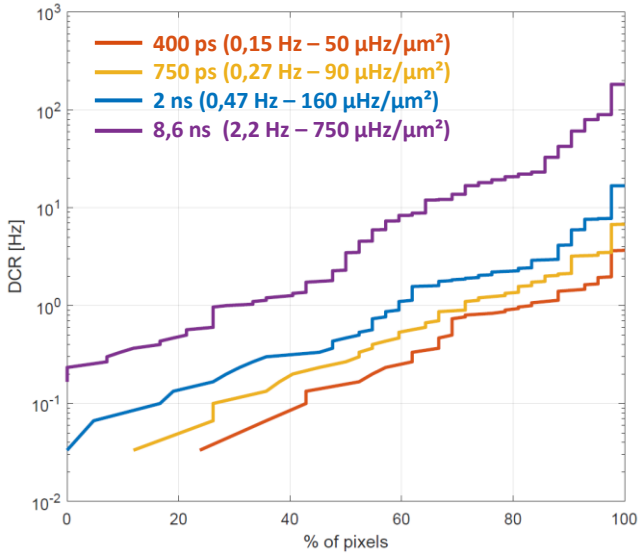
a1



a3

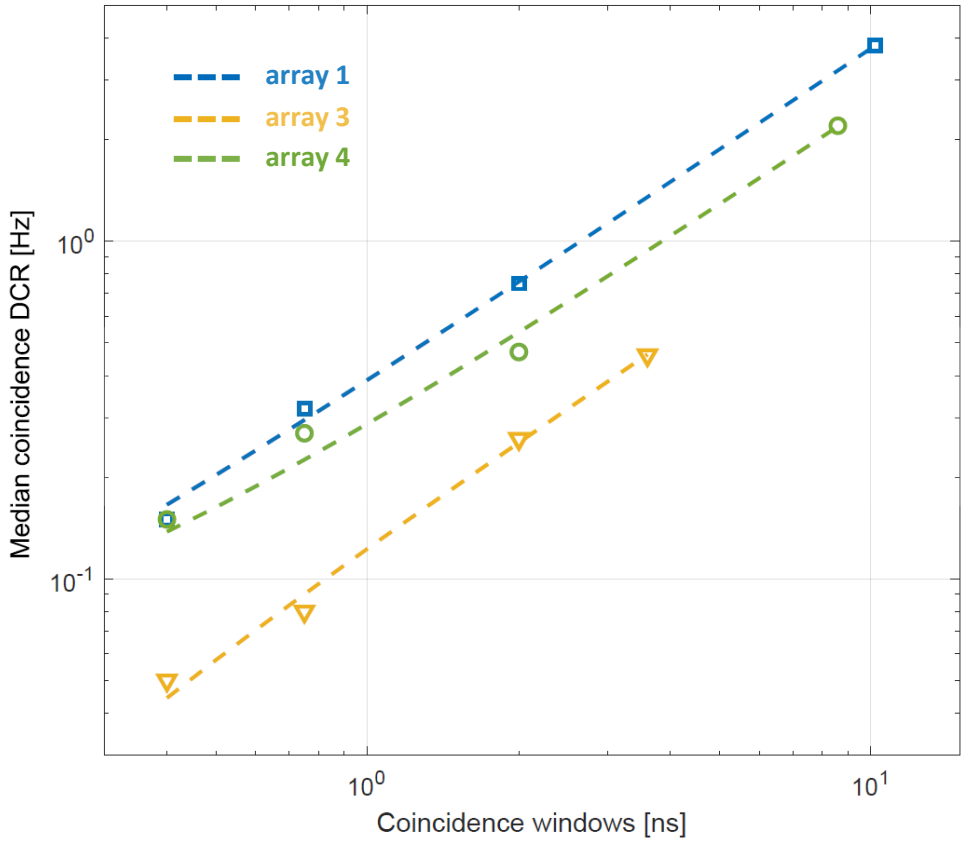


a4



Characterization results

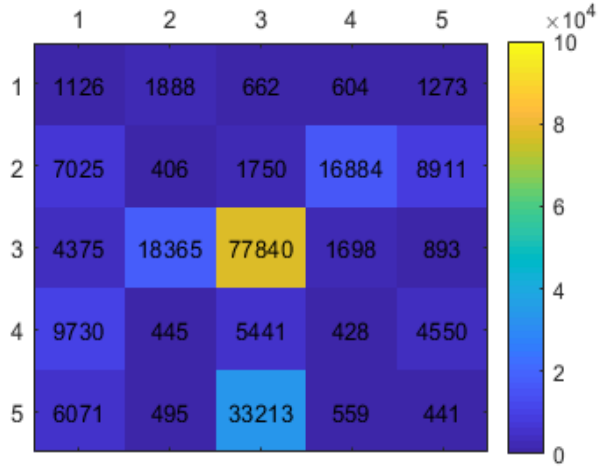
DCR WAS FOUND TO SCALE FAIRLY WELL WITH THE DURATION OF THE COINCIDENCE WINDOW



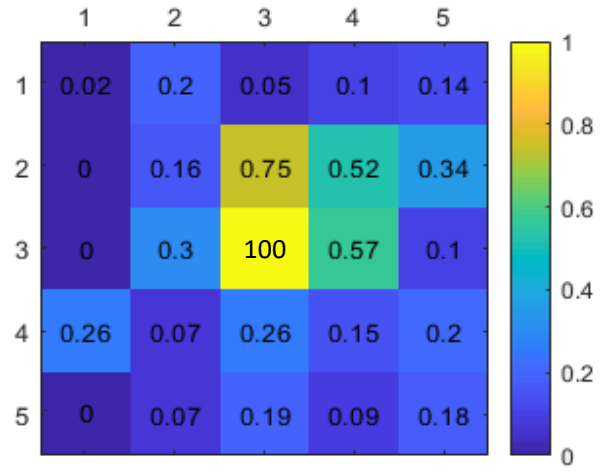
Characterization results

PRELIMINARY CROSSTALK MEASUREMENTS

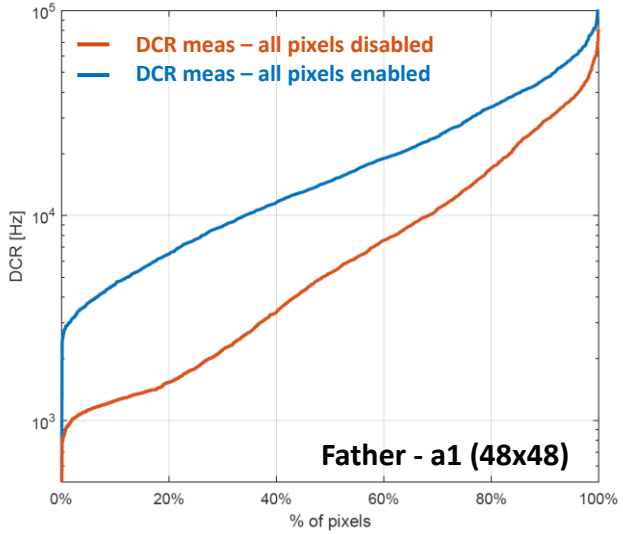
- Investigation on the behavior of some SPADs “screamers” affecting the DCR of surrounding pixels.
- Crosstalk probability expressed as: $$\left.\frac{(DCR_{current\ pixel,\ screamer\ on} - DCR_{current\ pixel,\ screamer\ off})}{DCR_{screamer}}\right|_{percentage}$$



DCR measurement - screamer off



Crosstalk probability (%) - screamer on



➢ Hesong Xu et al., Crosstalk characterization of single-photon avalanche diode (SPAD) arrays in CMOS 150nm technology, EUROSENSORS 2014

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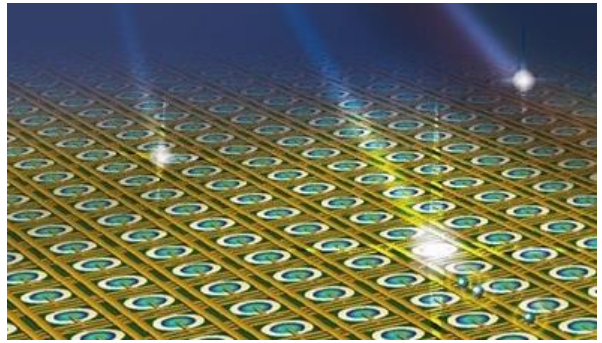
Conclusion

- A **DCR** median approximately equal to **2 Hz/µm²** (**Vex = 1,7 V**) was found for single tier chips;
- The **dual layer** approach revealed successful at drastically reducing DCR (median DCR from **60 µHz/µm²** to **400 µHz/µm²** for V_{SPAD} going from **20 V** to **21 V**);
- DCR was found to scale fairly well with the **active area** of the sensors;
- DCR was found to scale fairly well with the **duration of the coincidence window**.

Work in progress:

- Design of a new chip in **CMOS 110 nm technology**;
- **Radiation damage** studies;
- DCR characterization as a function of **temperature**;
- **Efficiency measurement** using a test beam;
- Design of a **probe prototype** for radio-guided surgery.



THANK YOU FOR YOUR KIND ATTENTION