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Bi-layered CMOS SPADs with coincidence-based DCR rejection for charged particle detection

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The features of SPADs, mainly used for the detection of faint optical signals in applications such as optical ranging, fluorescence lifetime imaging, position emission tomography and Raman spectroscopy, can be exploited also for charged particle detection. SPADs can leverage their huge internal gain to make charge pre-amplification unnecessary and reduce power dissipation. Moreover, on account of the very thin sensitive volume around the SPAD junction, the amount of sensor material can be minimized, therefore complying with the severe material budget requirements for future linear collider experiments. Use of CMOS processes in SPAD development offers the advantage of integrating the readout and processing electronics in a common substrate, resulting in a monolithic detector structure. This lends itself to improving the mechanical robustness of the system, simplifying the assembly of large detectors and optimizing the front-end circuits in terms of signal integrity and timing performance. On the other hand, noise performance of SPADs, usually represented through the dark count rate (DCR) parameter, can jeopardize their capabilities as charged particle detectors.

This work presents the characterization of arrays of SPADs, targeting charged particle detection, fabricated in a 150 nm CMOS technology. The devices under test (DUTs) include both single layer and vertically interconnected, bi-layered SPAD arrays with coincidence readout, the latter approach being proposed as a DCR mitigation strategy. The results presented in this work are mainly focused on the study of the breakdown voltage and its uniformity in the single layer arrays and of the dark count rate, measured in different working conditions, in both single- and dual-layer structures. In particular, the DCR in dual-layer SPAD assemblies is proved to comply with the statistical model accounting for the coincidence between random avalanche signals, with median DCR values well below 1 kHz/mmˆ2. The comparison between the DCR performance of the two configurations emphasizes the advantage of the coincidence readout over the standard, single-tier architecture. Preliminary results from cross-talk characterization of the DUTs will also be introduced and discussed.

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