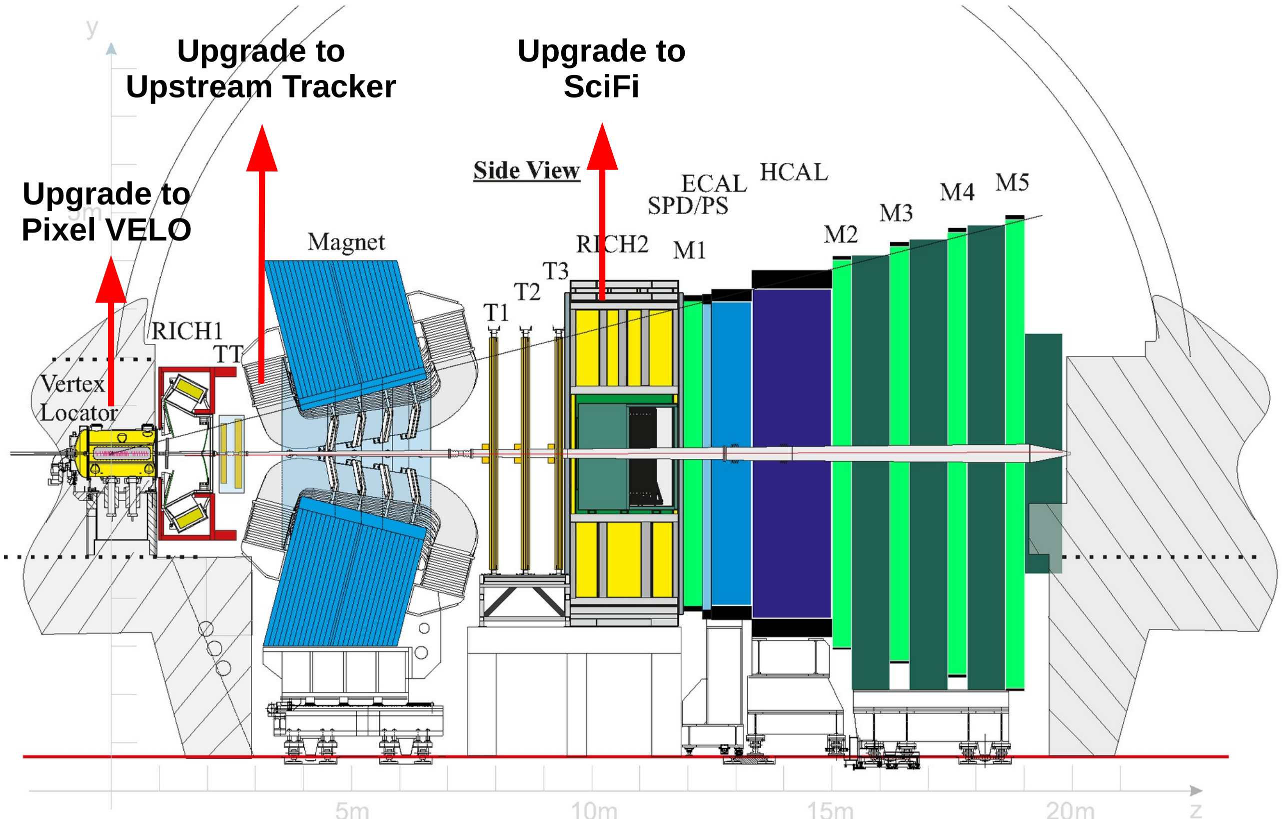
The Upstream Tracker: the silicon strip detector for the LHCb upgrade

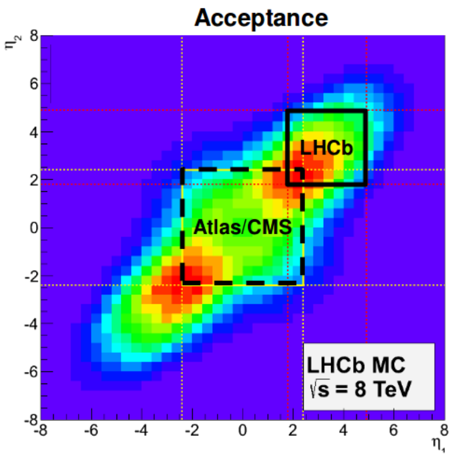
Marco Petruzzo
INFN, Milano

On behalf of the LHCb UT group



Single arm forward spectrometer

- Coverage: $2<\eta<5$
- Designed for CP violation studies in b and c hadrons decays and their rare decays



Run 1 → 3 fb^{-1} collected
Run 2 → 6 fb^{-1} collected

Precision of many physics measurements at LHCb statistically limited at the end of Run 2

LHCb Upgrade I - Run 3

- 5x luminosity → L= $2*10^{33} cm^{-2}s^{-1}$
- 5 fb^{-1} / year
- 40 MHz readout and full software trigger
- New tracker (VELO, UT, SciFi)
- New optics and PMTs of RICH 1, RICH 2

Upstream Tracker upgrade

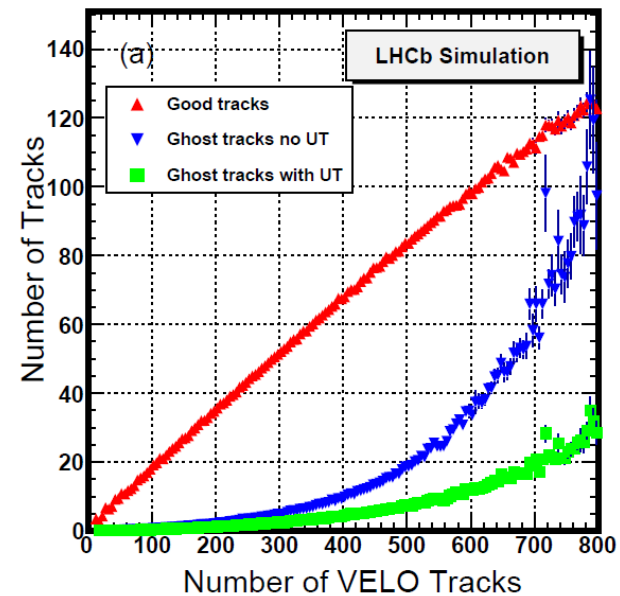
← 9 fb^{-1} → Upgrade I ← Goal: 50 fb^{-1} →

Run 1			LS1		Run 2				LS2			Run 3			LS3			Run 4		
2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

UT in the LHCb tracking:

- Intermediate measurements between VELO and downstream tracking → **ghost tracks reduction**
- Fast estimate of the particle momentum
  → $\sigma(P_T)/P_T$~15% VEL0+UT momentum resolution
  → sufficient to measure the sign of tracks and suppress low-momentum tracks
  → 3x reduction of the time required by the forward tracking algorithm
- Increase reconstruction efficiency of long lived particles:

  e.g. $K^0_S \to \pi^+\pi^-$, $\Lambda \to p\pi^-$.



Run 3

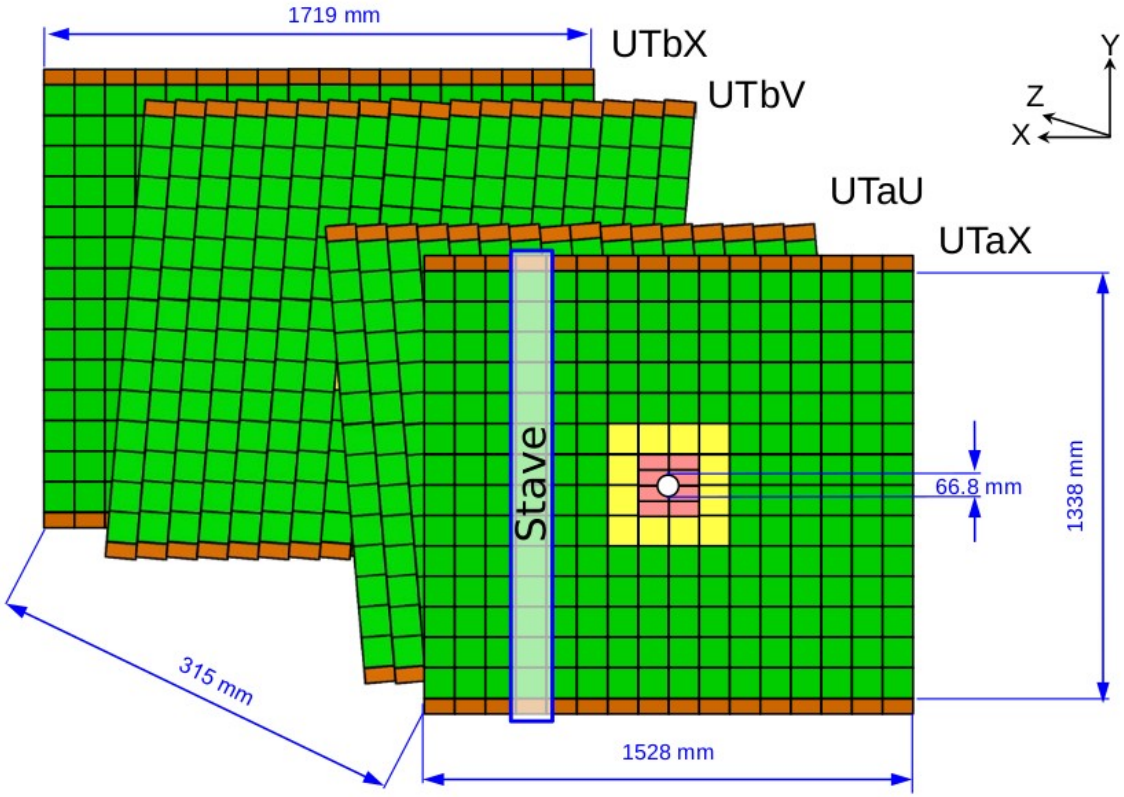
5x luminosity
Increase of detector **occupancy**
Increase of **radiation** level

→

UT upgrade

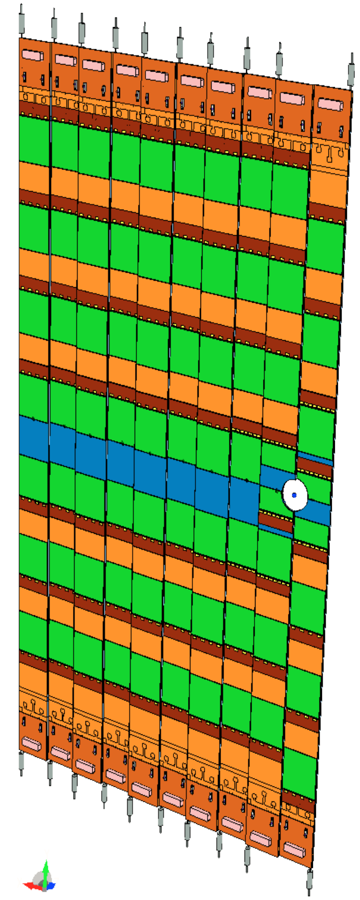
Finer granularity and improved **coverage**
40 MHz readout
Improved **radiation hardness**

UT overview



Four detection layers constructed using vertical "staves".

Measure of XUVX coordinates: 0° and ±5° strips providing **stereo information**

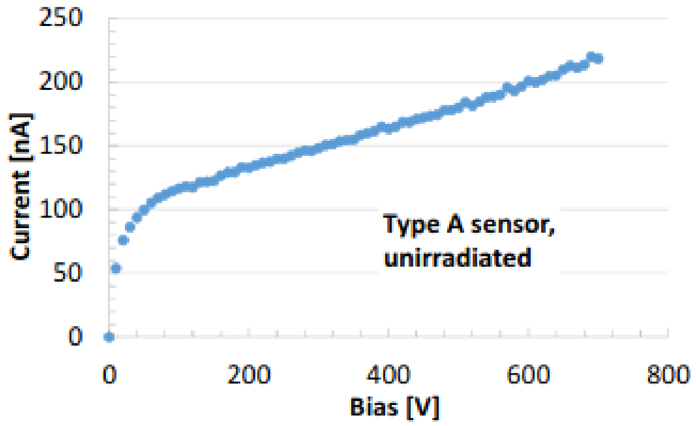


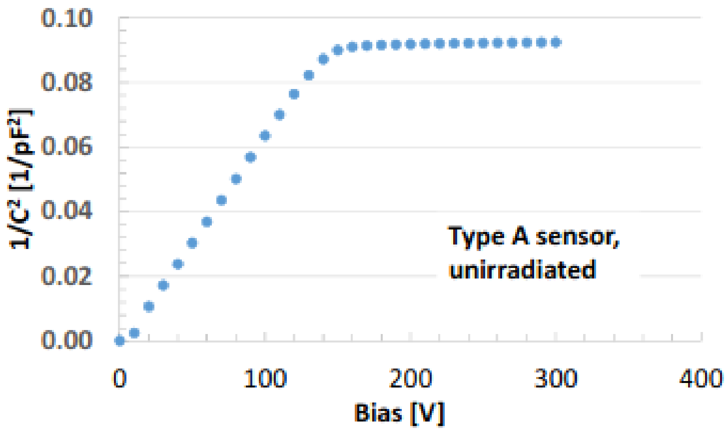
Single-sided silicon strip sensors on both sides of the stave

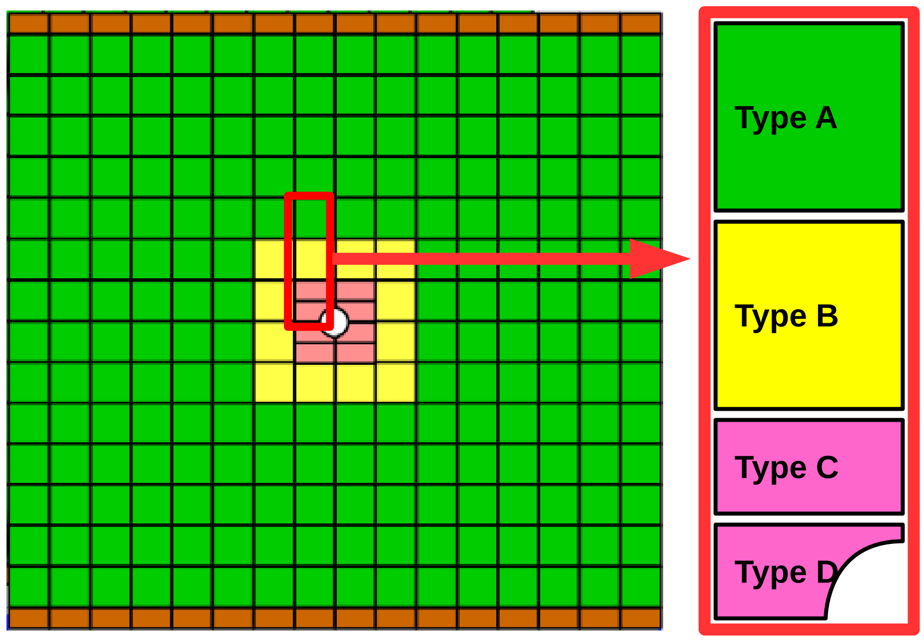
- Sensors/staves overlapping to **reduce gaps** in acceptance
- **Finer segmentation** in high-occupancy region
- Inner-most sensors with circular cut-outs to **maximize the acceptance** near the beam line

Silicon sensors

- **Four designs** to cope with **occupancy** and **radiation**. Sensors produced by **Hamamatsu**
-
- **Top-side** HV biasing
- **Inner region: n-in-p** type with 93.5 um pitch and circular cutout near the beam pipe
- **Outer region: p-in-n** type with 187.5 um pitch and embedded pitch adapter





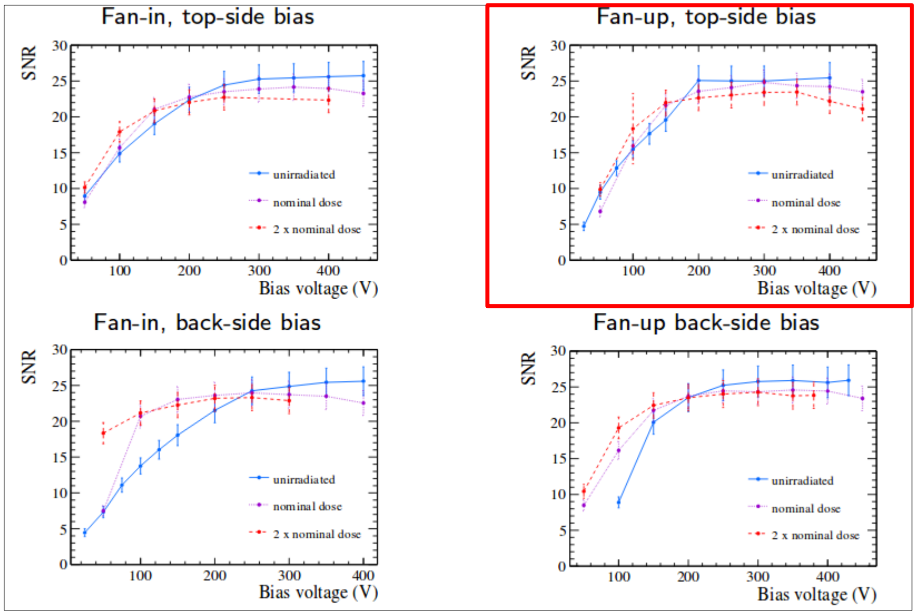


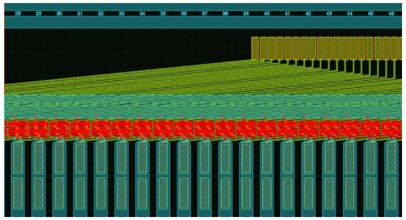
Sensor	Type	Thickness	Length	Pitch	#
A	p-in-n	320 um	99.5 mm	187.5 um	888
B	n-in-p	250 um	99.5 mm	93.5 um	48
C	n-in-p	250 um	50.0 mm	93.5 um	16
D	n-in-p	250 um	50.0 mm	93.5 um	16

Sensor R&D

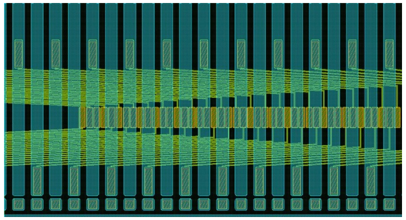
Sensor R&D:

- Different designs investigated and tested in 2014-2017 testbeams
- **Embedded pitch adapter** for Type A sensor: → **FanIn** vs **FanUp**
- **Top side** vs **Back side** biasing scheme
- Different technologies: **p-in-n** vs **n-in-p**





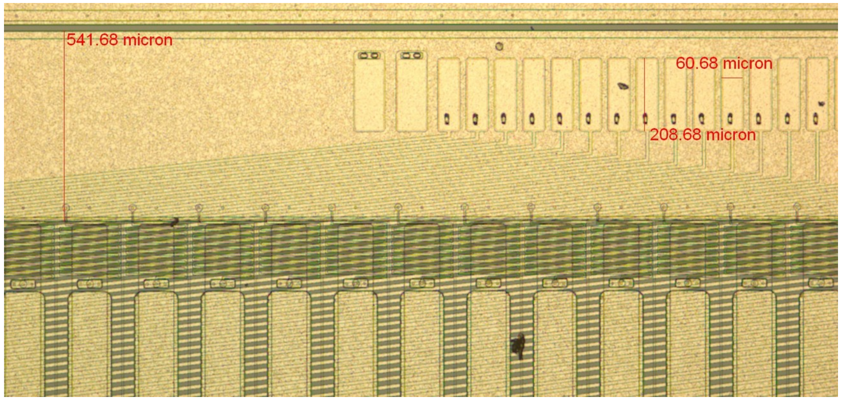
FanUp : routing in inactive region



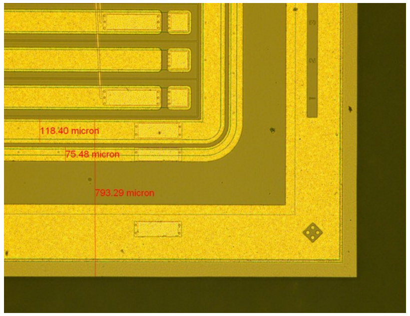
FanIn : active strips with routing on top

Final version

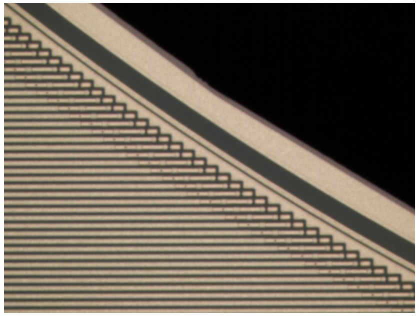
Embedded pitch adapter



Top side HV biasing



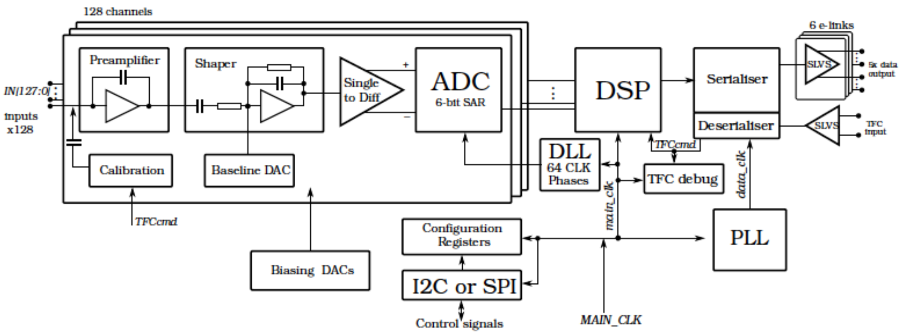
Circular cut-out

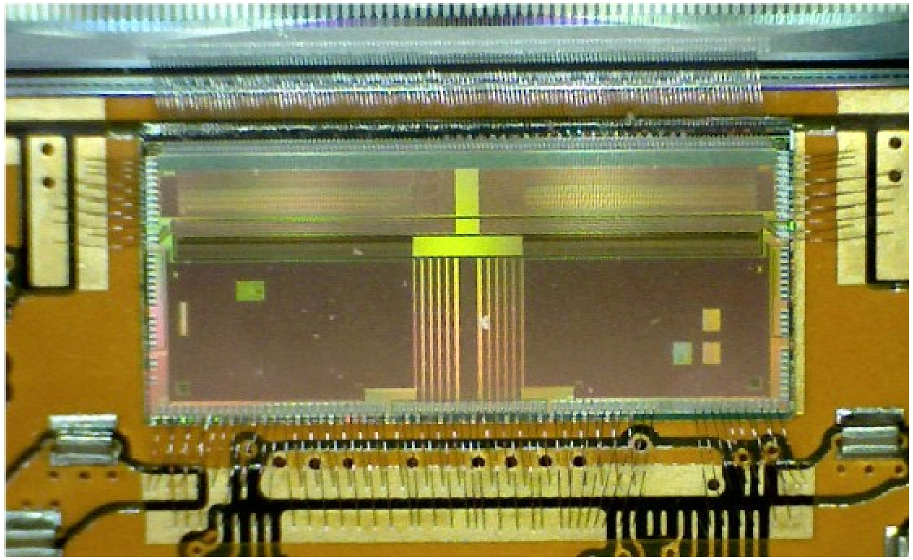


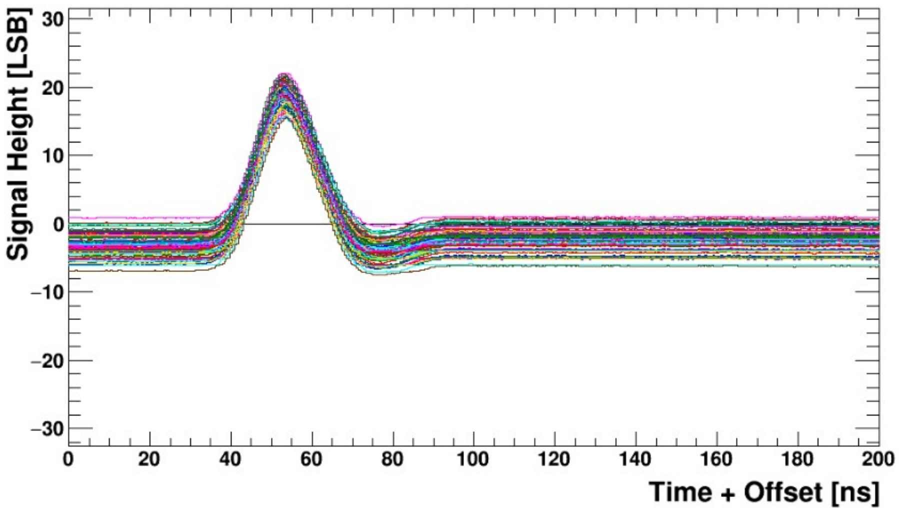
SALT chip

“Silicon ASIC for LHCb Tracking”

Good shaping time:
- T_peak ≤25 ns
- <5% after 2 T_peak







TSMC CMOS **130 nm** technology

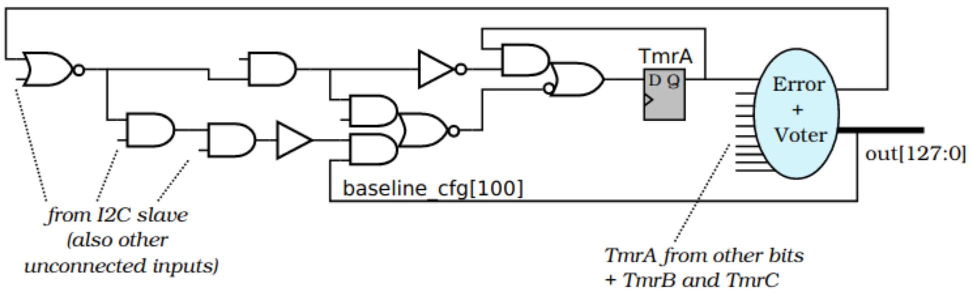
- **128 channels**, wirebonded to sensors
- Input pitch **80μm**

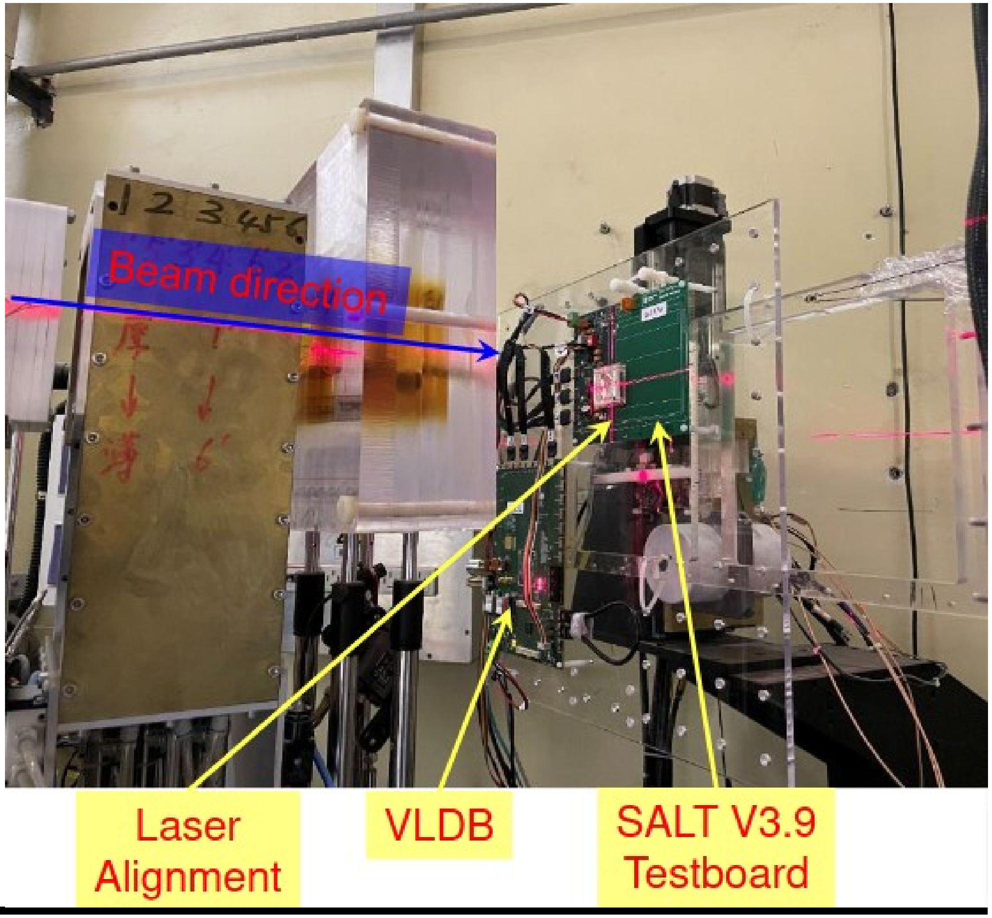
- **30 MRad** radiation tolerance
- **40 MHz** readout
- Up to 5 SLVS e-links @ 320 Mbps

- **DSP functions :**
  → pedestal subtraction
  → common mode noise subtraction
  → zero suppression

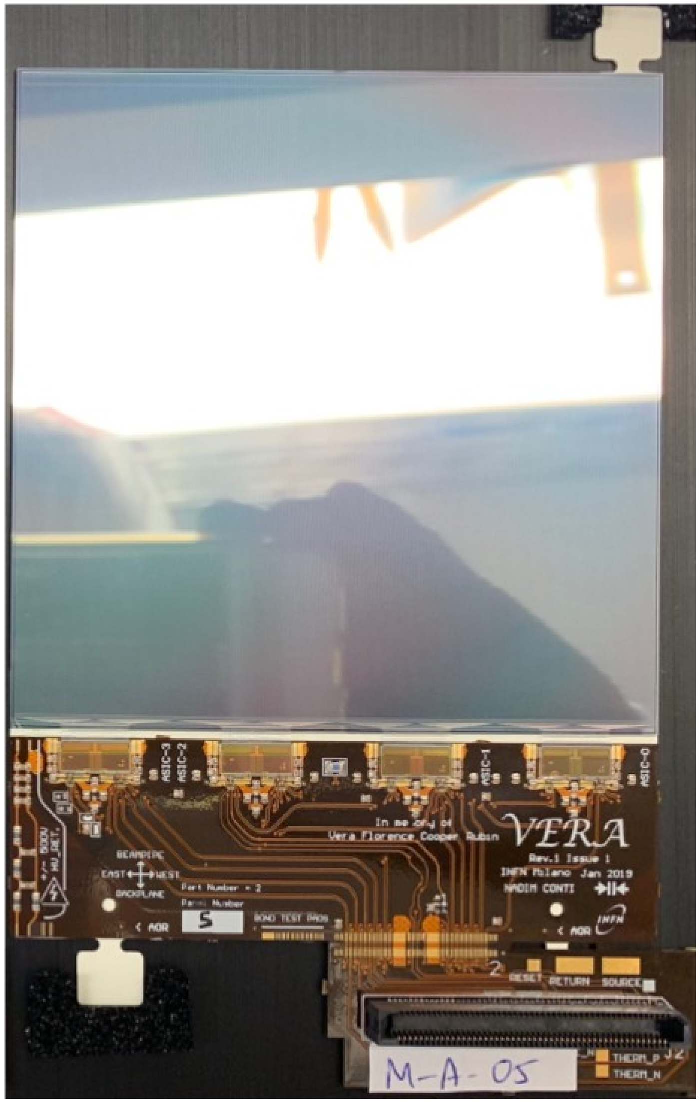
SALT SEU issues

- **SALT v3.5** is vulnerable to radiation in its **TrimDAC and Pedestal registers**
- **Issues** due to:
  → **increased combinatorial logic when moving** from RTL Compiler/Encounter to Genus/Innovus
  → **Some registers grouped** for SEU corrections
- **New SALT v3.9** version with more synchronizers, reduced logic, no register grouping
- **SALT v3.9 tested** at CIAE 100 MeV proton synchrotron facility in late 2020
- **SEUs** in TrimDAC and Pedestal registers rates reduced from V3.5 **by factors of 165 and 21, respectively**
- SALT v3.9 will be used for the readout of the **innermost sensors** with higher particle fluence





Flex Hybrids and Modules



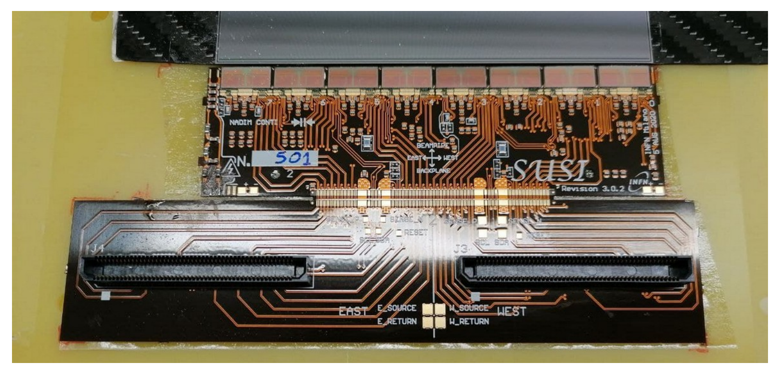
Module hosting a **4-chip hybrid** and a type A sensor

Flex hybrid:
- **Hosts** the front-end **ASICs**
- **Routes power and data** between sensor and periphery

- **Two designs:**
  → **VERA**, hosts 4 ASICs and is used for type A sensors
  → **SUSI** , hosts 8 ASICs and is used for type B,C,D sensors

- **ASICs are glued** to the hybrid with thermally and electrically conductive glue, **then wirebonded** to both the hybrid and the sensor

A **Module** is composed of:
- **A ceramic stiffener** for support and thermal conductivity
- **Flex hybrid** and **sensor**



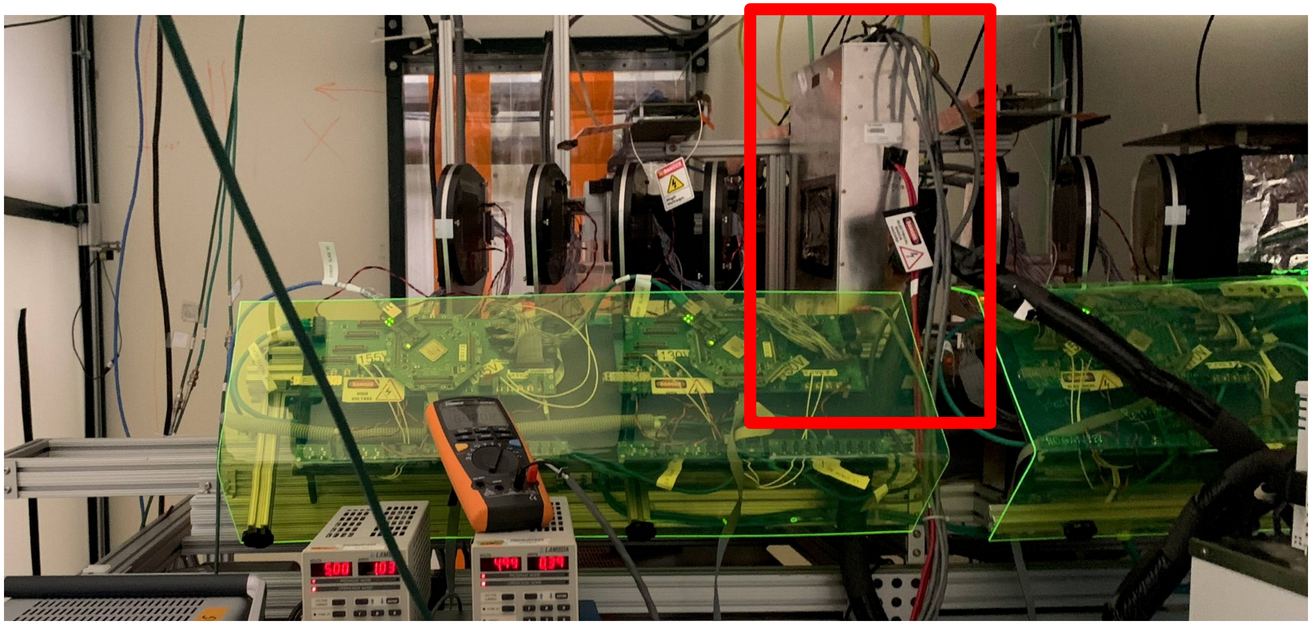
8-chip hybrid and sensor mounted on a on a prototype test board

Sensor and ASIC testbeam

Testbeam at Fermilab in March 2019

First test with nearly final **modules,** with Type A and B sensors**:**

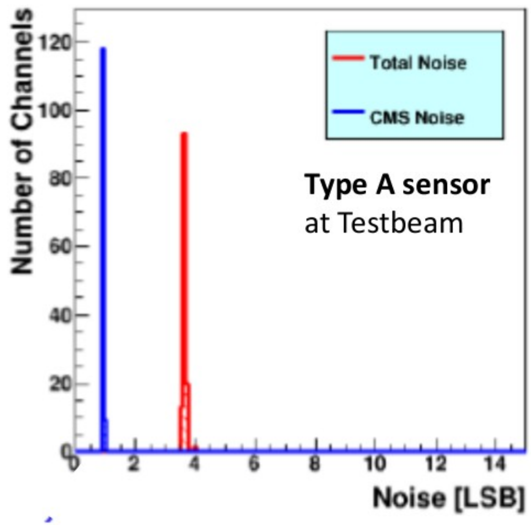
- DELTA hybrid (4-chip prototype not for production)
- SALT v3.5 ASICs
- Excess noise due to interference with external tracking system

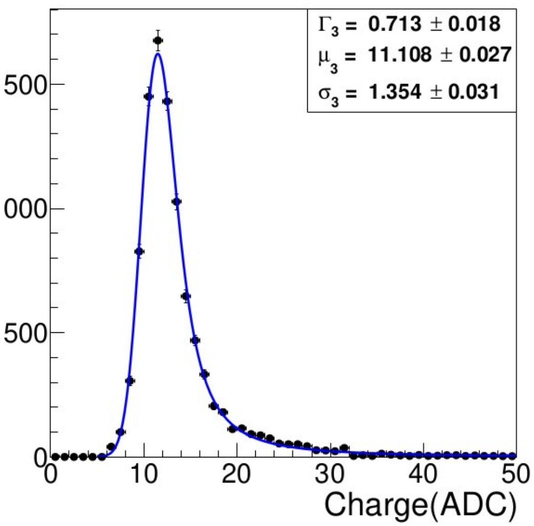


Testbeam results

Testbeam at Fermilab in March 2019:

- Type A **non-irradiated** sensor:
  → 99.5% efficiency with **S/N ~ 12**
- Type B **irradiated** sensor:
  → 6.2 * 10^{13} n_{eq}/cm^2 : ~ 2 x max. exp. dose
  → 94% efficiency and **S/N ~ 11**
- **Lower efficiency** mostly due to readout limitations:
  → **will be recovered** with LHCb readout





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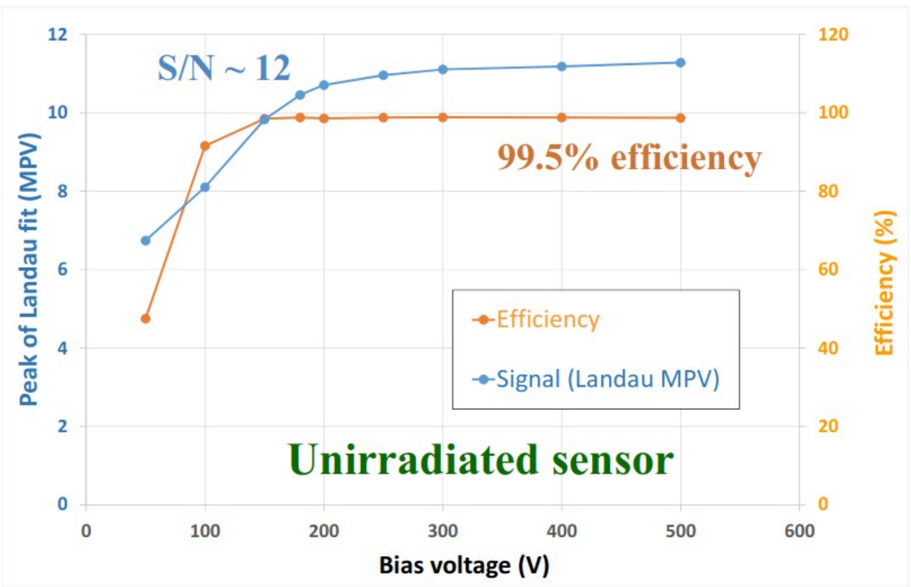
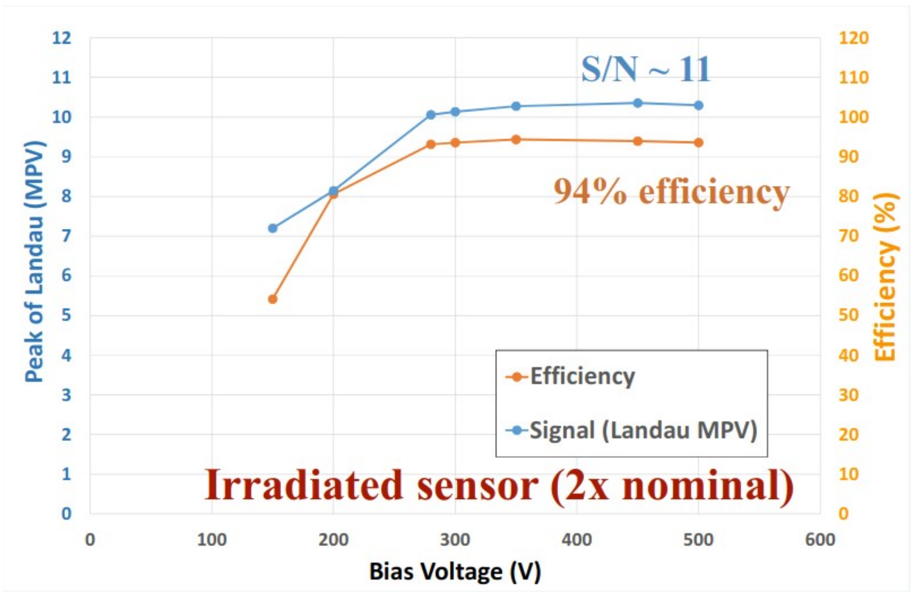
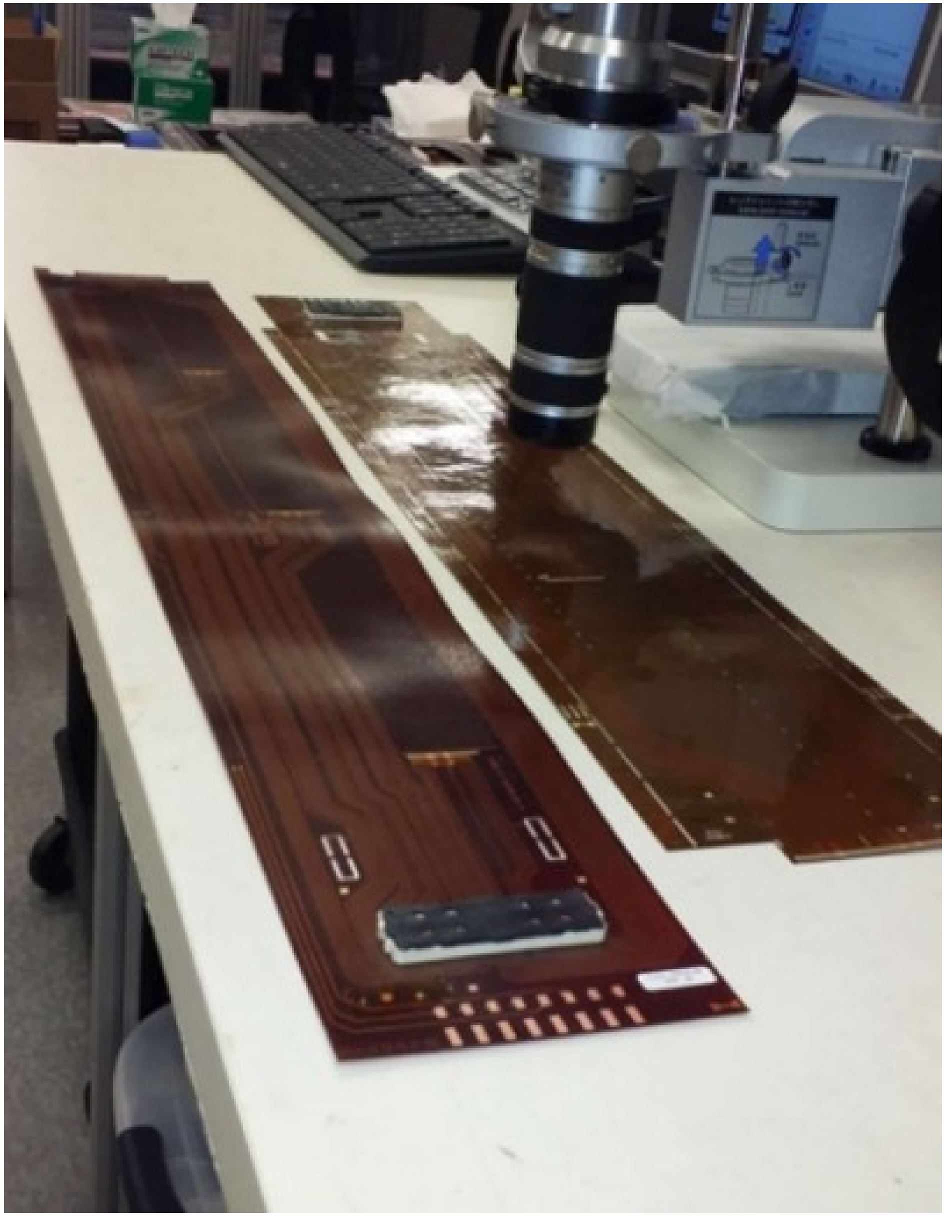


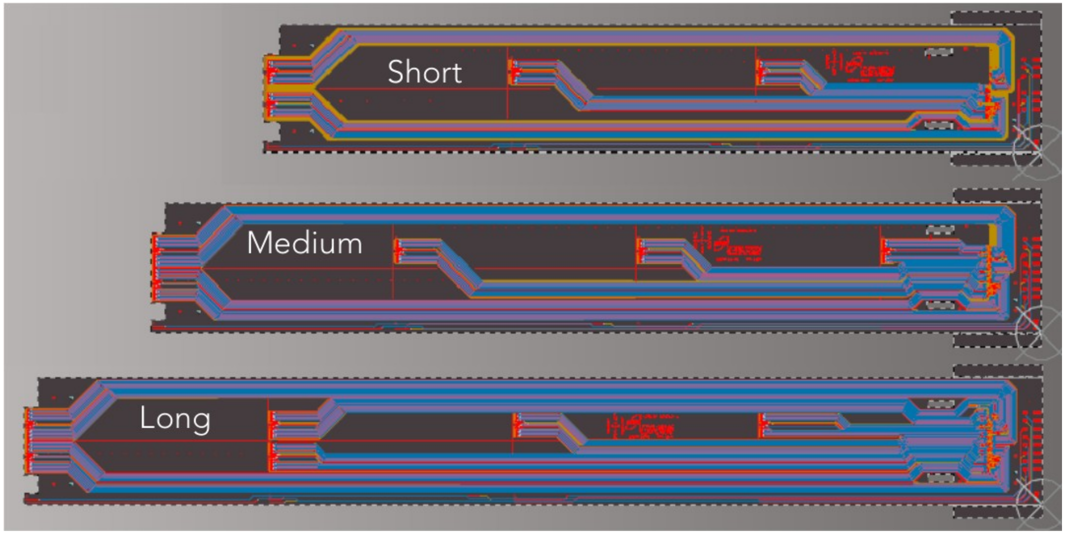


Dataflex



Dataflex:

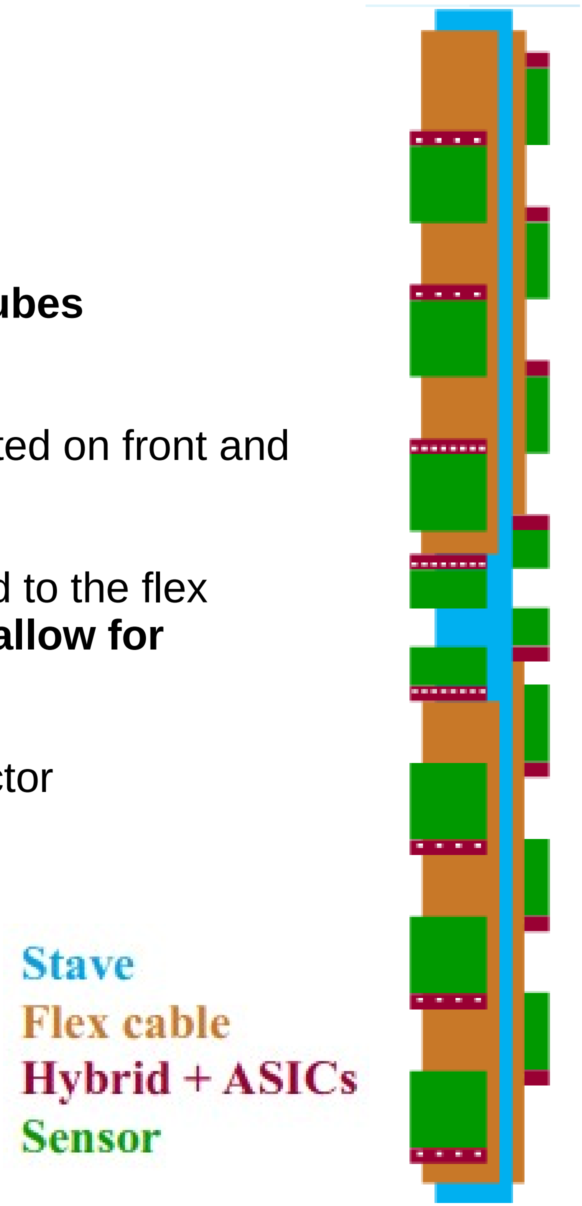
- **Low mass kapton flex cables** for readout, power and grounding
- Sensor **modules are wirebonded** to the flex cables
- **100 Ω** differential input impedance traces
- **Up to 1000 V** between adjacent lines
- **Less than 500 mV** roundtrip voltage drop



Staves

Stave:

- 1.6 m x 10 cm **low-mass support**
- Foam support with **CO_2 cooling tubes** sandwiched in carbon fiber
- **Overlap between sensors**, mounted on front and back of the stave
- Wirebonded modules are anchored to the flex cables using epoxy at 3 points, to **allow for replacement** in case of damage
- Total of **68 staves** for the UT detector



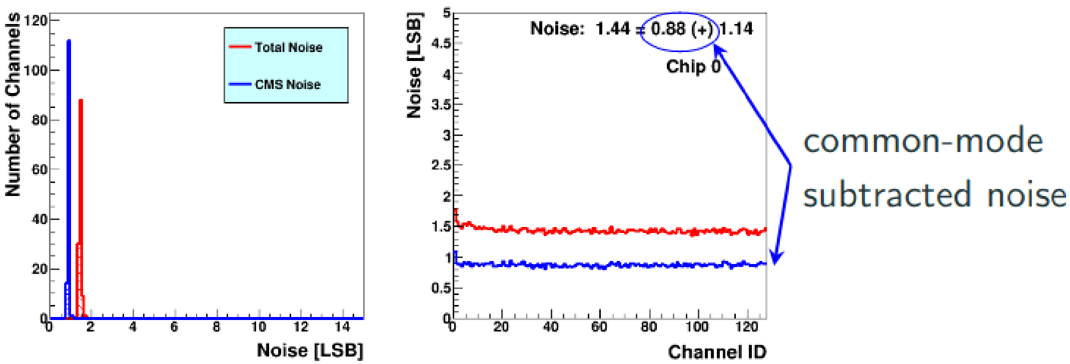
Slice test

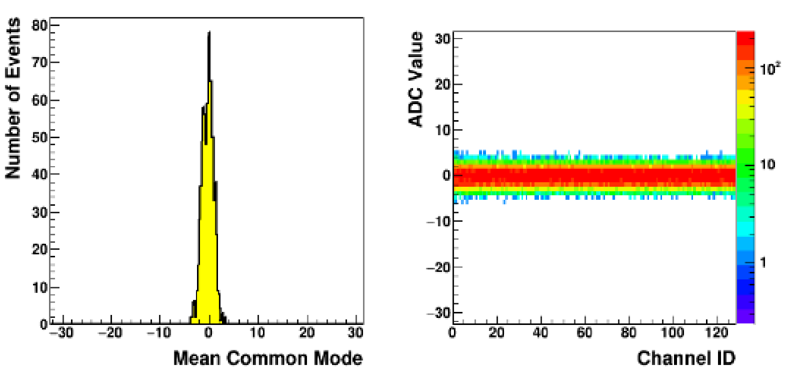
Assembled stave tested at CERN in the UT Slice Test setup, which allows for:

- Connection to the **CO_2 cooling** system
- **Humidity** control
- **Light-tight** environment

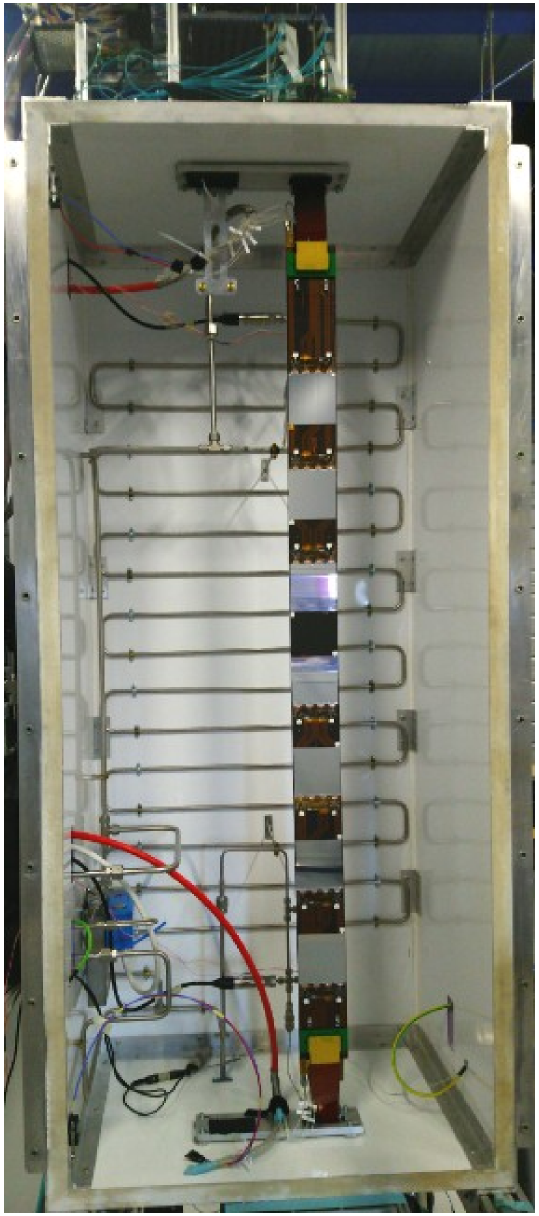
Results:

- Similar to the single-module tests
- example at 5°C, 400V bias: noise∼0.88, MIP signal∼13 → S/N∼15

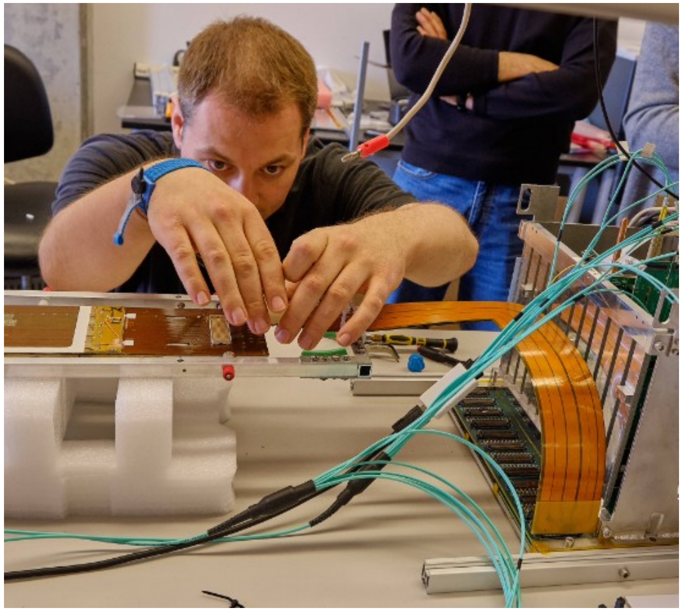




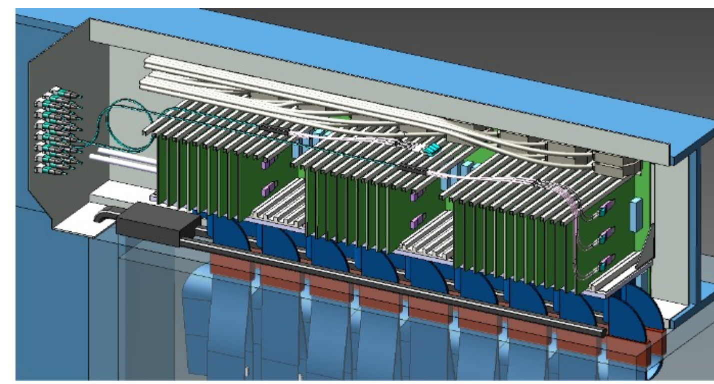
- The slice test is also useful to **develop the readout software**.
- **Production staves** will be fully tested once installed in the UT.



Peripheral electronics (PEPI)

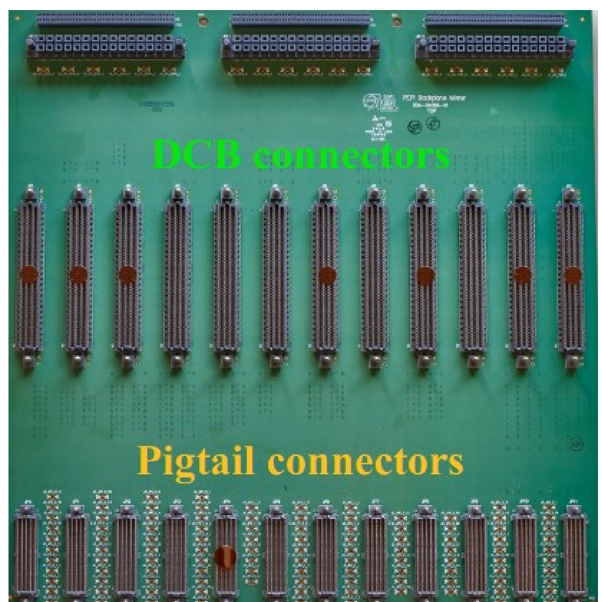


- **DCBs** send data to the **DAQ**
- **7 GBTx** ASICs per board
- **3 VTTx + 1 VTRX**
  (6 Tx, 2 Rx optic links @4.8Gbps)



- A **flexible pigtail** connects the each stave to the peripheral electronics (**PEPI**)
- The **backplane distributes balanced loads** to the data concentrator boards (DCB)

  → ultra-dense 28 layers layout at the limit of the manufacturability

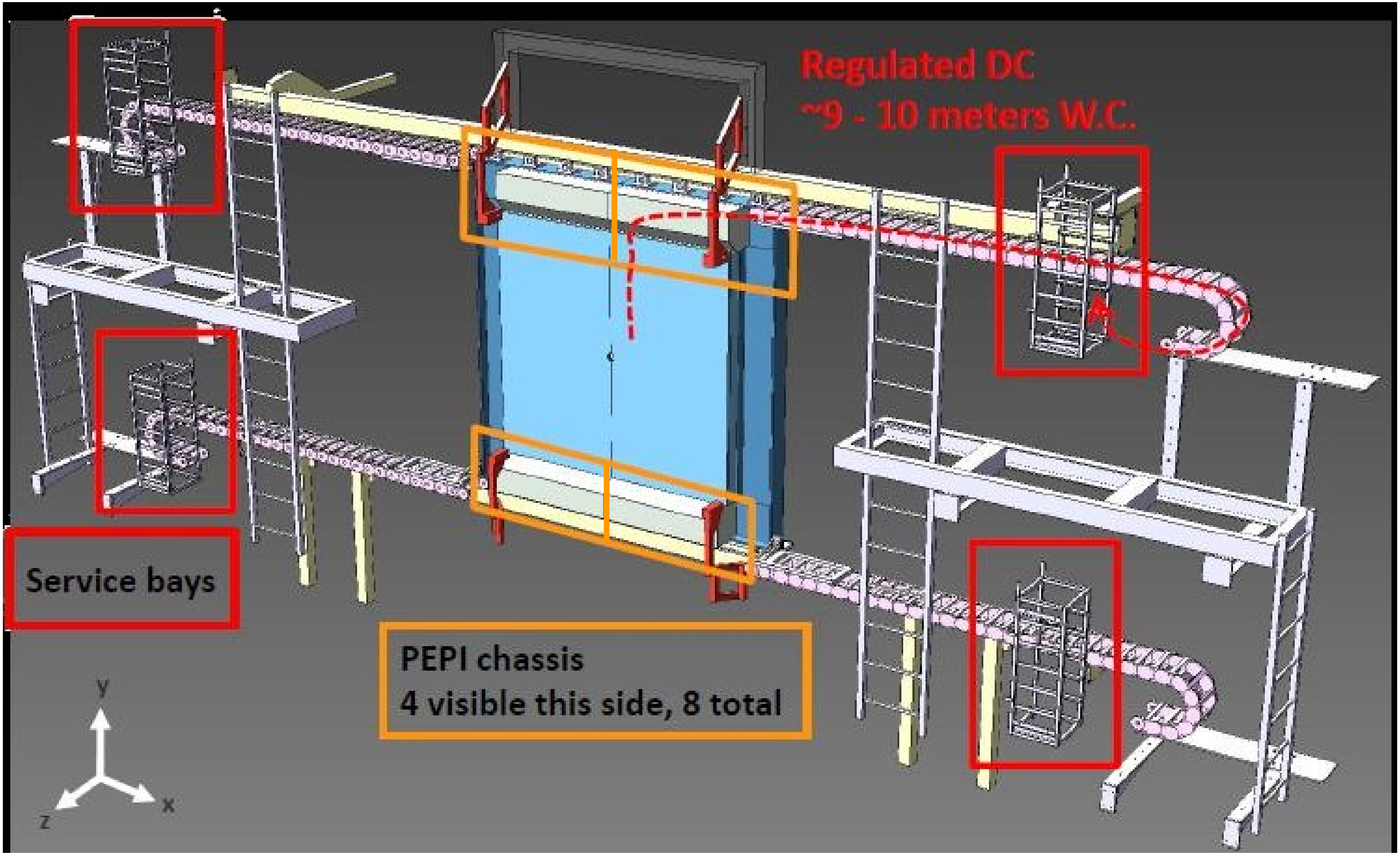


- **248 DCBs:**

  → **7.1 Tbps** output bandwidth

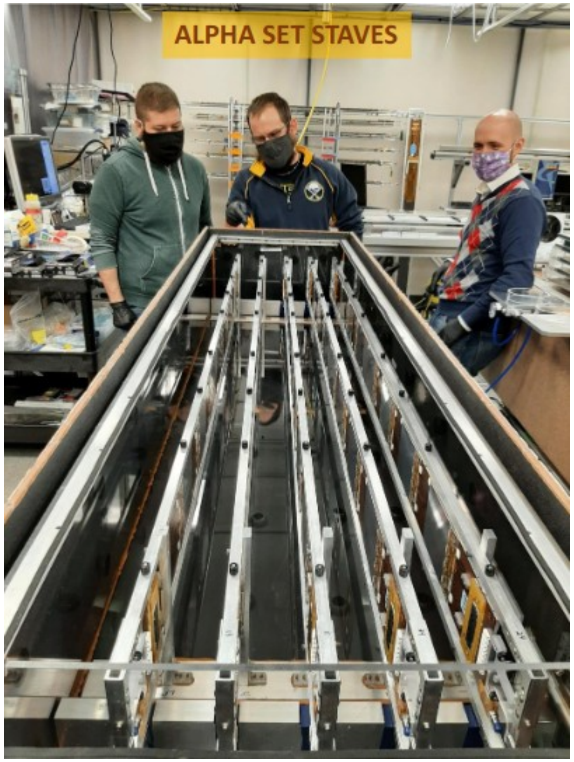
  → organized into **8 PEPI crates**

UT integration



Production status

- **VERA** (4-chip) **hybrids** production and assembly almost complete and **SUSI** (8-chip) **hybrids** production starting
- **Dataflex** and **pigtail** cables production being finalized
- **PEPI** electronics (backplane, DCB, LVR) **produced, QA-ed,** and currently being re-tested at CERN
- **Modules and Staves** assembly is ongoing
- First **fully instrumented staves** shipped to CERN



Summary

The **Upstream Tracker** plays a critical role in the tracking for the LHCb Upgrade

Major upgrades with respect to the current TT tracker

- **Finer granularity** in the inner region
- Improved **radiation hardness**
- Fast readout at **40 MHz**

The UT is currently being built, and **most components have been produced** and delivered

- **Silicon sensor** and **ASICs** have been tested in multiple testbeams
- **Hybrid production** and ASIC mounting almost finished
- **PEPI** electronics being tested at CERN
- **Modules and Staves** assembly is ongoing
- **Mechanics, cabling**, etc. being prepared at CERN

- Aiming for **installation** underground **by the end of 2021**