Charge collection efficiency of a thinned, backside biased, neutron irradiated High Voltage-CMOS active matrix

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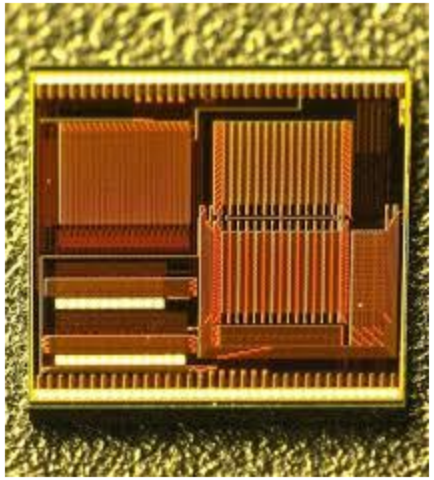
Motivation

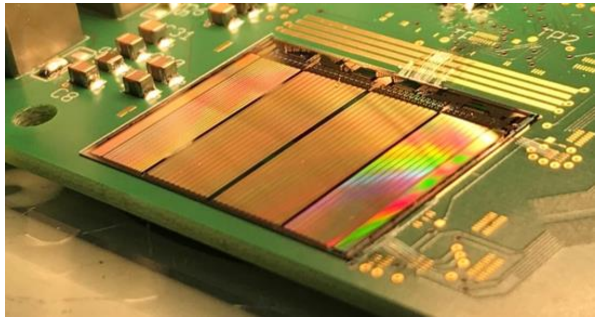
The proposed 10x luminosity upgrade of the Large Hadron Collider (LHC) is just one example of the field moving forward with respect to particle energies and rates.

High Voltage CMOS is designed to be radiation tolerant, highly granular with small monolithic active pixels and able to be thinned for minimum interaction with experimental particles trajectories.

One must characterize what has been achieved with the technology so far to determine how to further develop it.



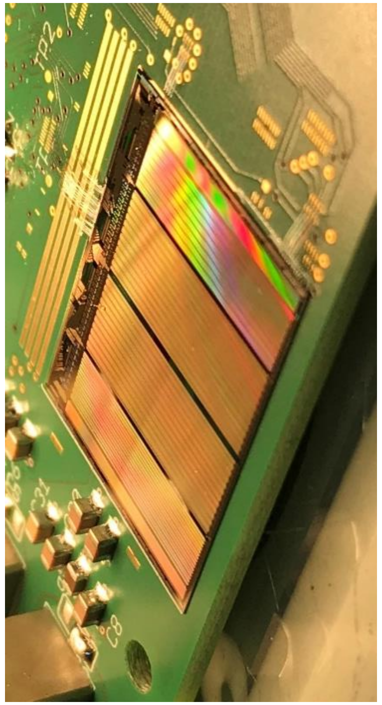
HVPixel1: 2006

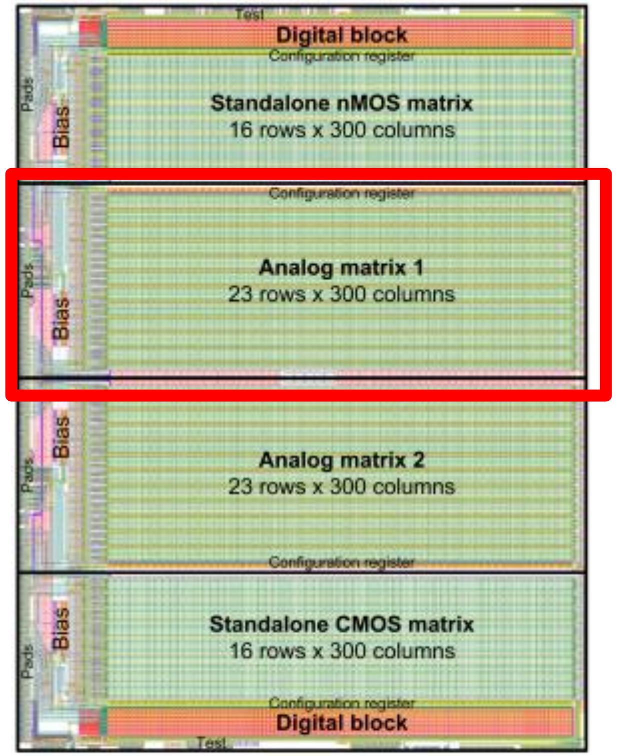


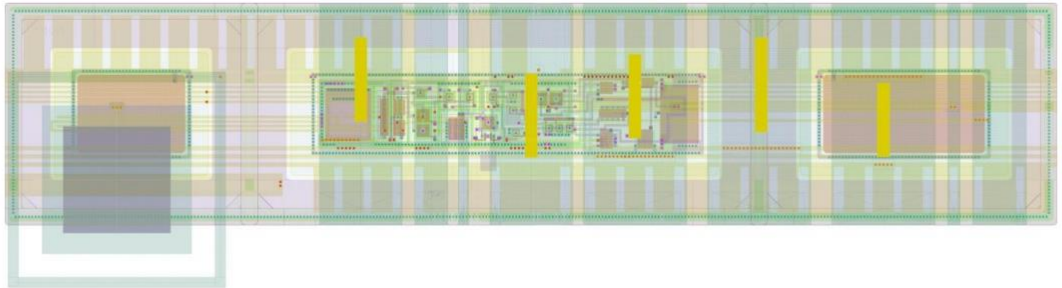
H35DEMO: 2016

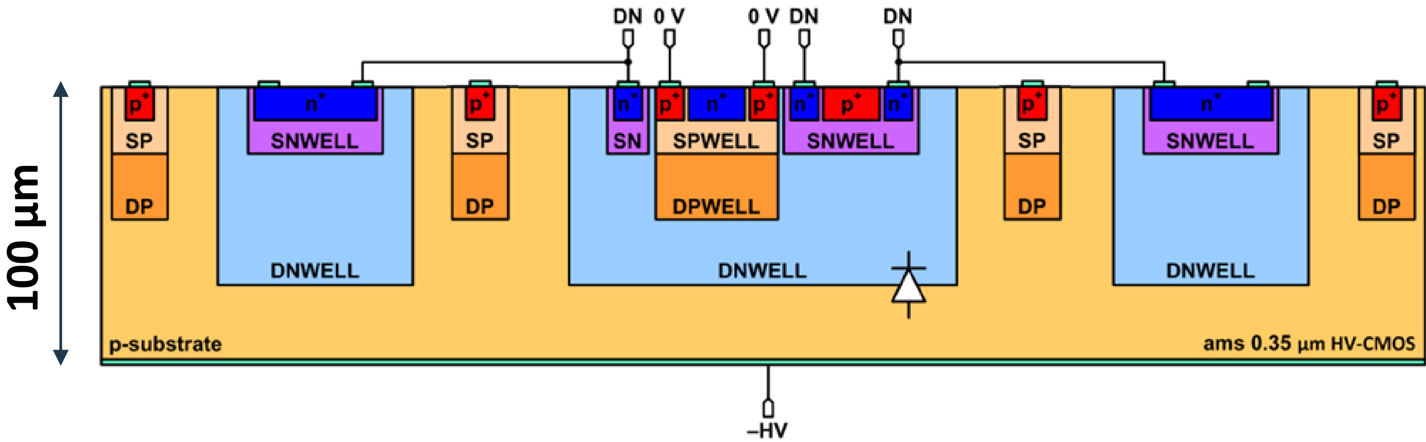
H35DEMO

- 4 Matrices – Active monolithic pixels (No external readout ASIC)
- Designed in the 0.35 µm process from AMS
- **100 µm thin**
- Chip dimensions are 24.40 mm x 18.49 mm
- **Backside biased**
- Substrate resistivities (20 Ω · cm, 80 Ω · cm, 200 Ω · cm, **1000 Ω · cm**)
- 300 columns and either 16 or 23 rows of pixels per matrix
- **Pixel size 250 x 50 µm**



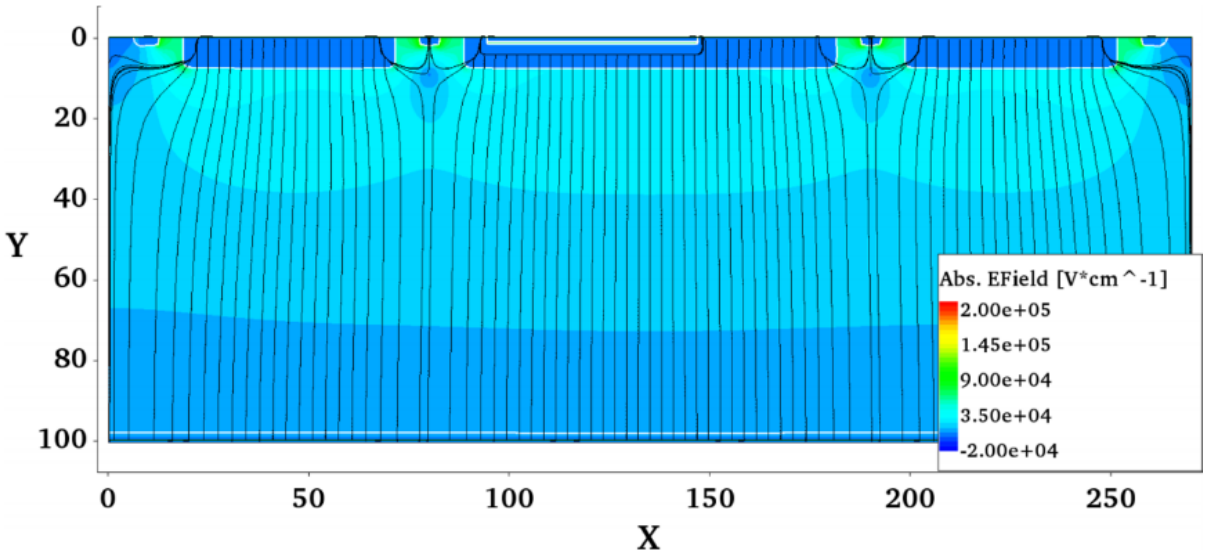




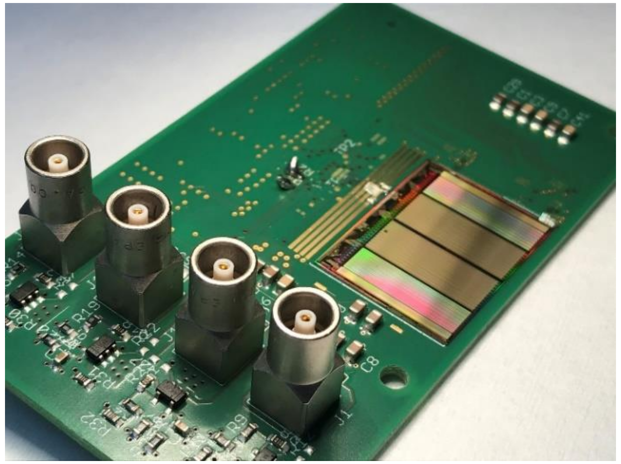


H35DEMO

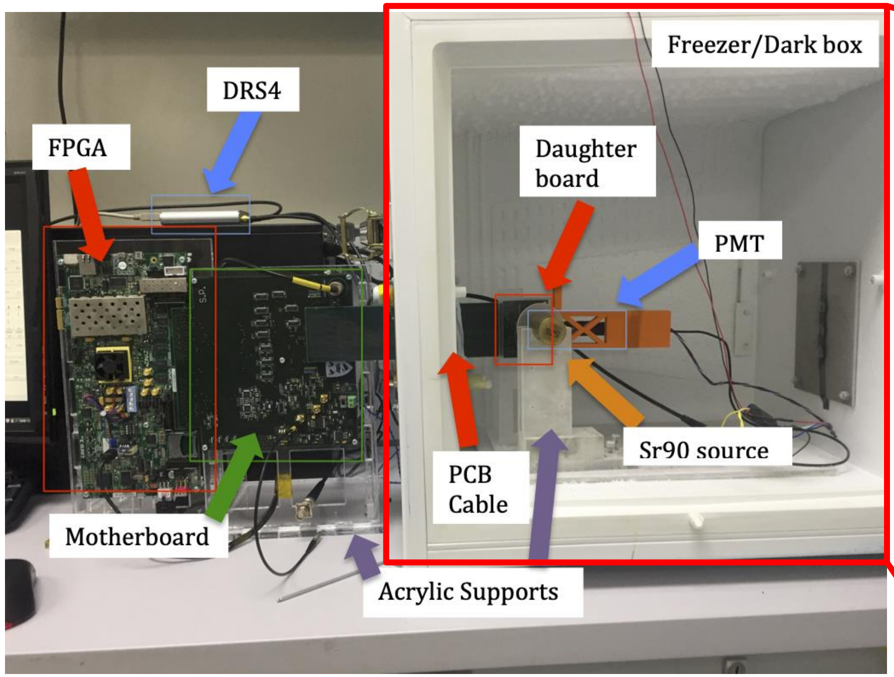
- From TCAD simulations, we know that with thinned, backside biased sensors produced in high resistivity substrate have:
  - Stronger electric field lines
  - Shorter charge collection times
  - Potentially better radiation tolerance

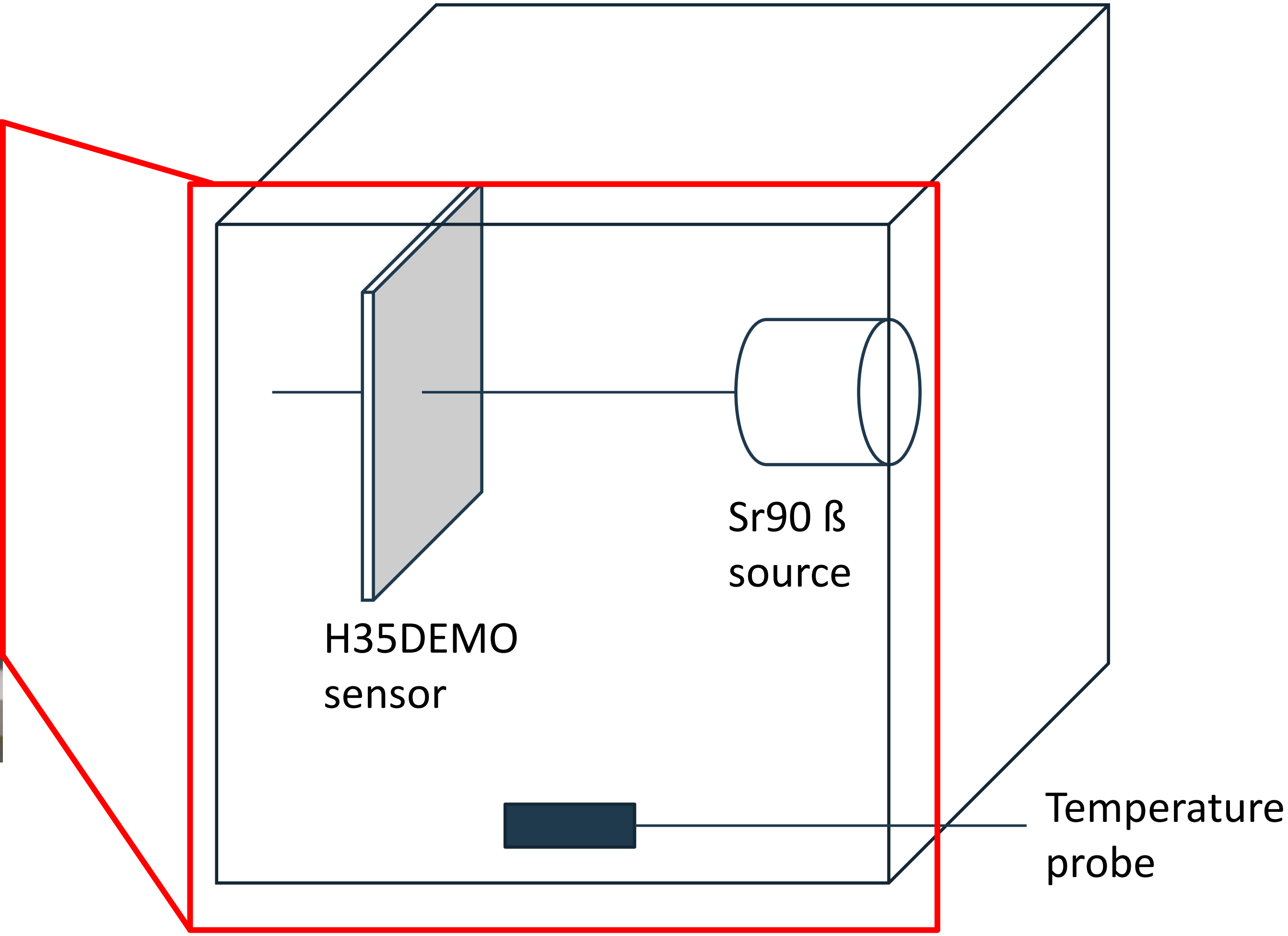


L. Meng, PhD thesis, 2018



Setup





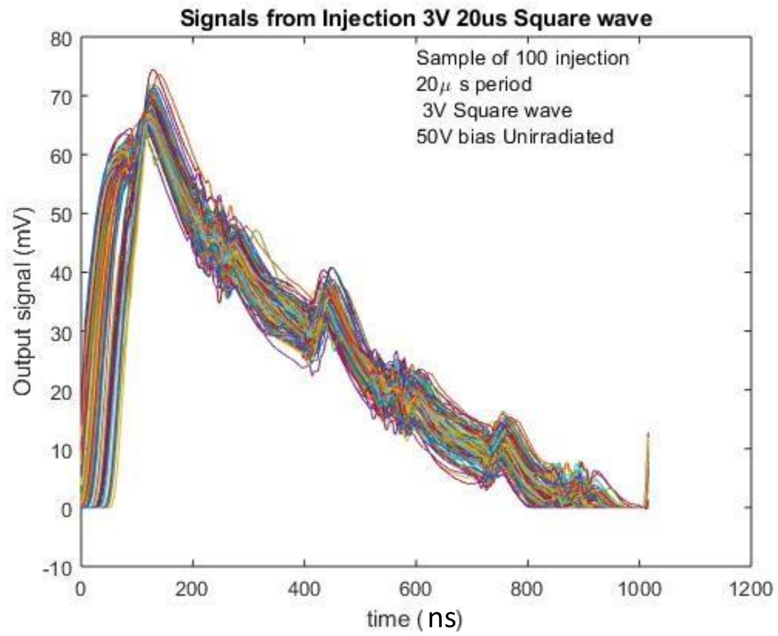
1. Injection Pulses to test in-pixel amplification circuit
2. Use radioactive sources to stimulate the sensing junction 1.6 µs with 1024 sampling points using a DRS4 board to digitize analogue signal
3. Trigger on analogue output itself -> Find a way to determine real vs dark hits

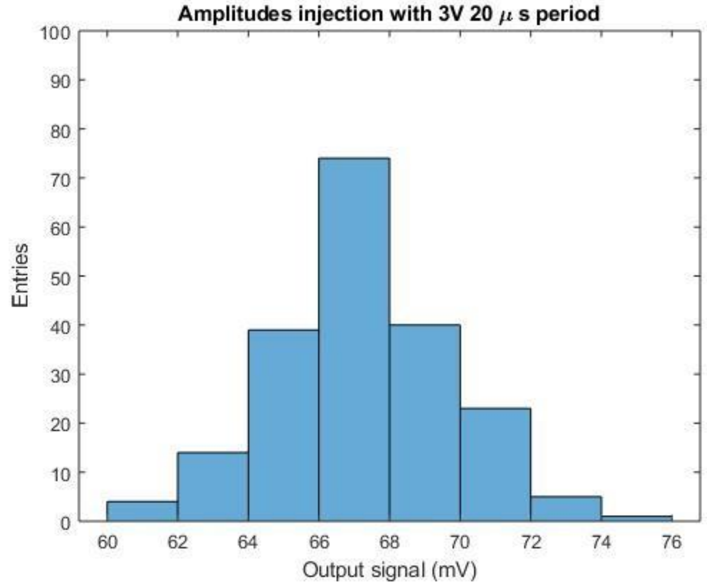
Charge Injection

Firstly the CSA electronics have been tested using a 0 - 5 V square wave test pulse through the injection circuit.

The injection circuit does not use the sensing junction of the sensor.

Therefore the charge collected should not depend on the bias voltage used, but a standard shaped signal output is expected.

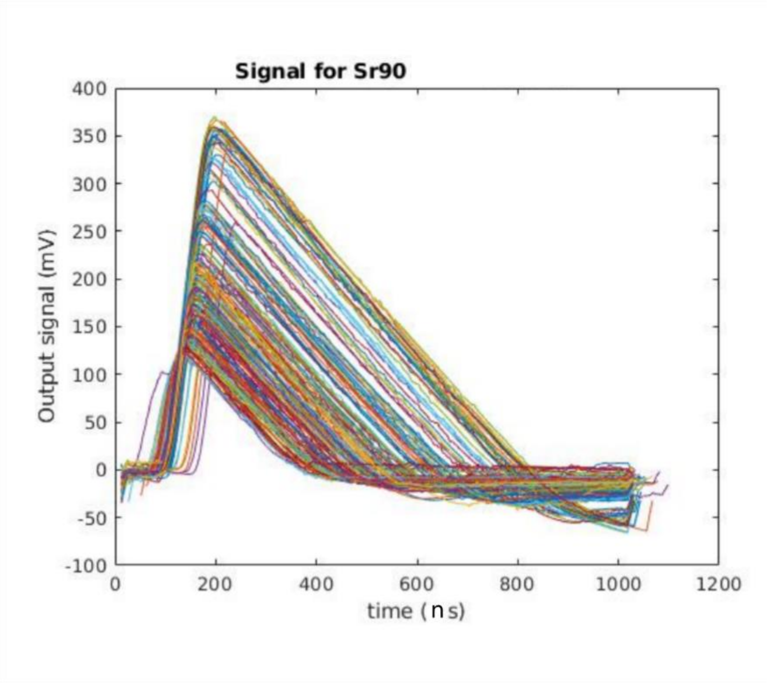


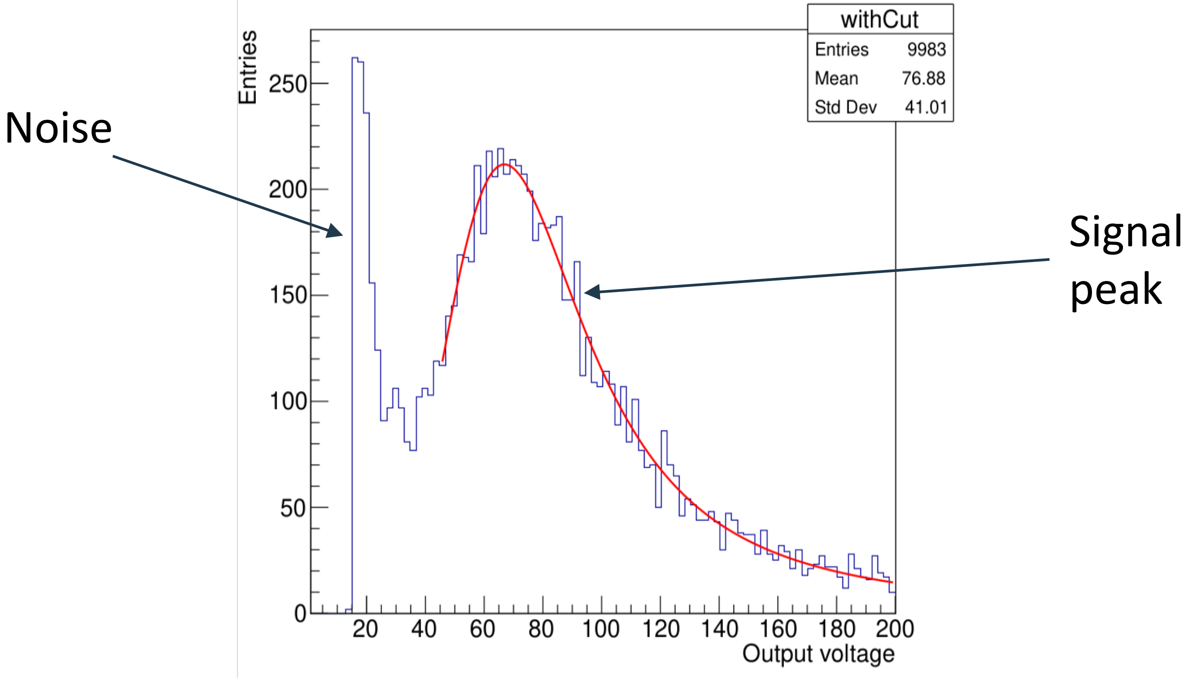


Sr90 Testing

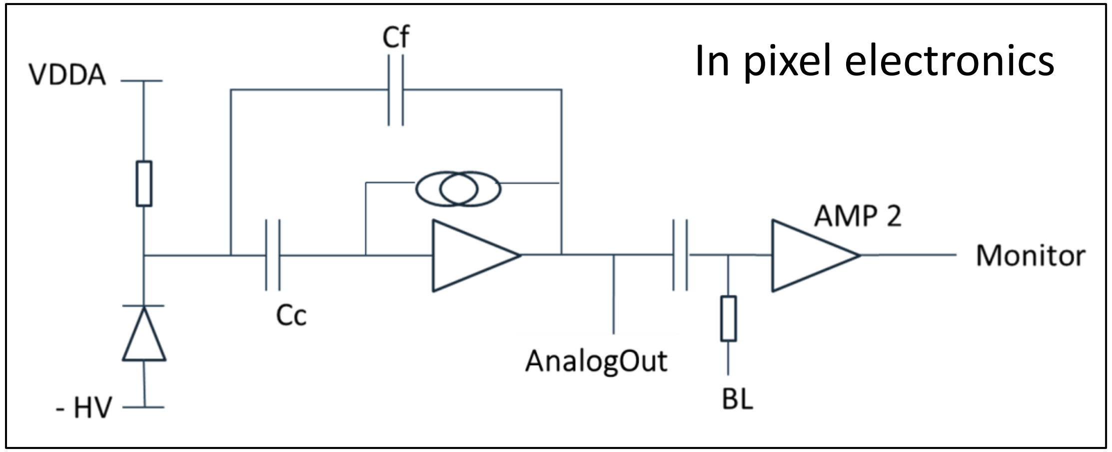
Source measurements are expected to give a spectrum of response which is seen but we see a much larger spreads at low energies.

Source is collimated to a thin beam but still emits in an area larger than a single pixel, some responses are seen from pixels neighbouring the readout pixels.





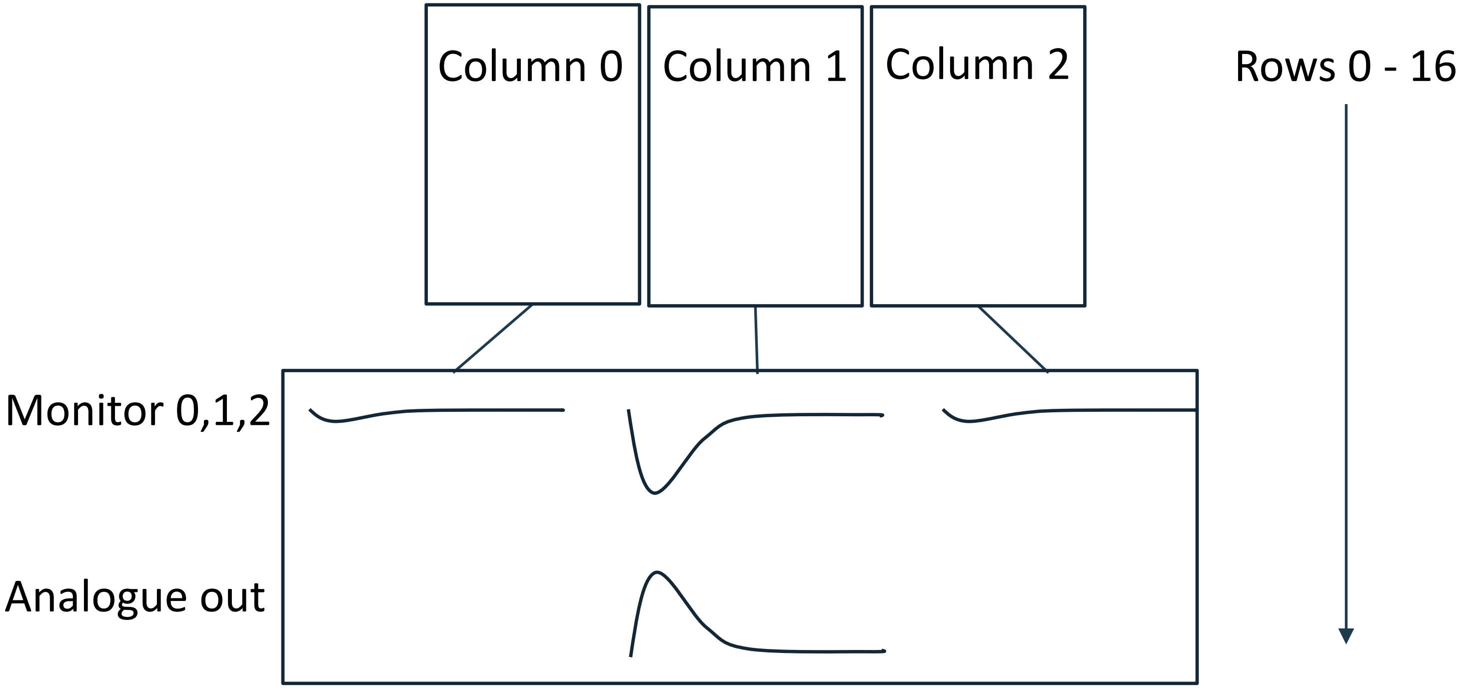
Monitor Line Setup



The analogue matrices have 3 monitor outputs and 1 amplifier output (AnalogOut) meaning the 3 adjacent pixels can be read out simultaneously.

AnalogOut → Output of the pixel after the source follower (SFOut) + one buffer at the periphery.

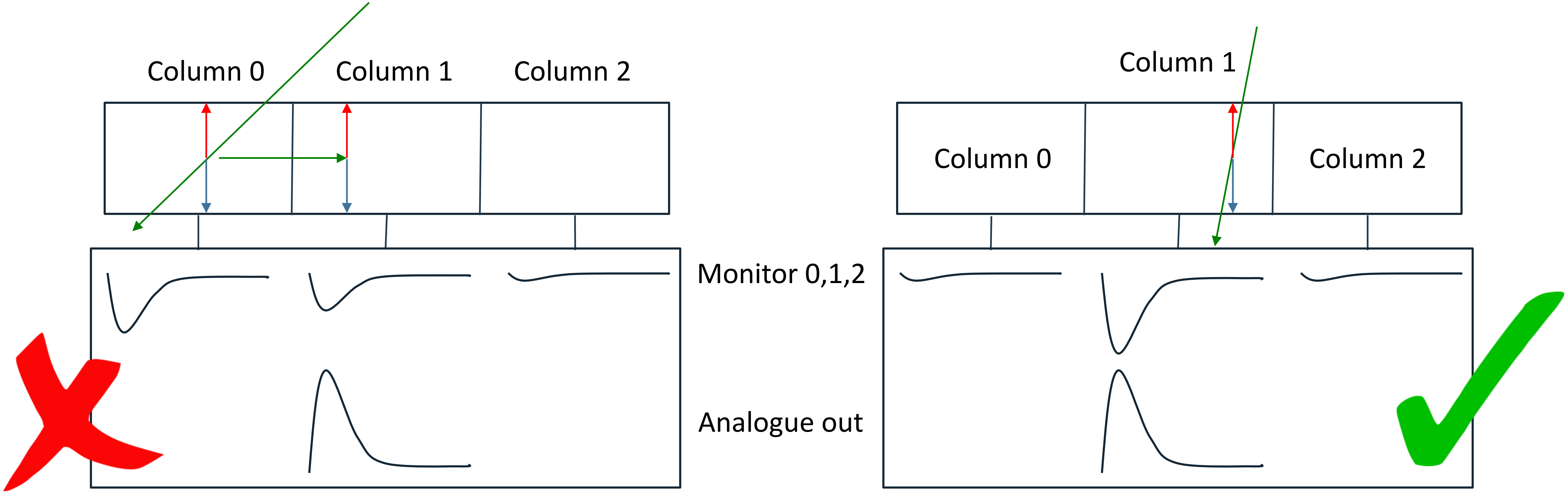
Monitor → Output of the pixel after the output buffer (Test) + one buffer at the periphery



Charge Sharing Detection

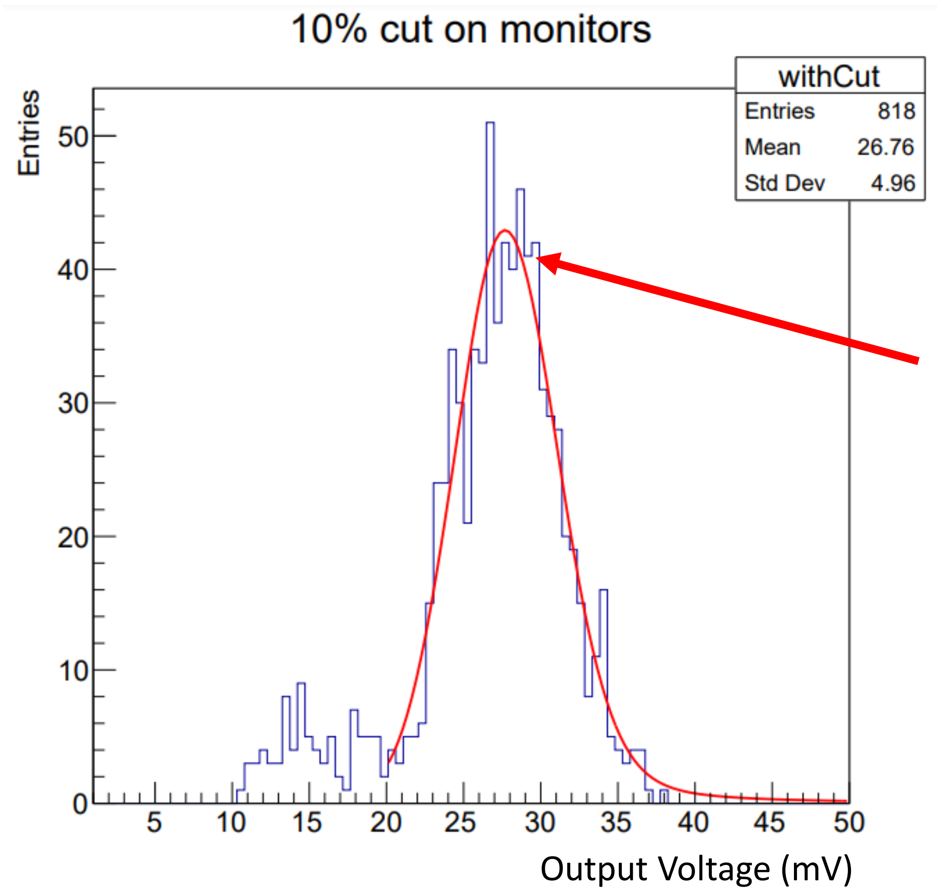
For a hit to be counted:

- Column 1 Aout must be triggered on.
- Column 1 monitor must be above a certain threshold (50% Aout<1>)
- Column 0 and 2 monitor outputs must be below a certain threshold. (10-20% Aout<1>))



Conversion Ratio

The X-rays produced by the Fe-55 source create electron/hole pairs in the depletion region.



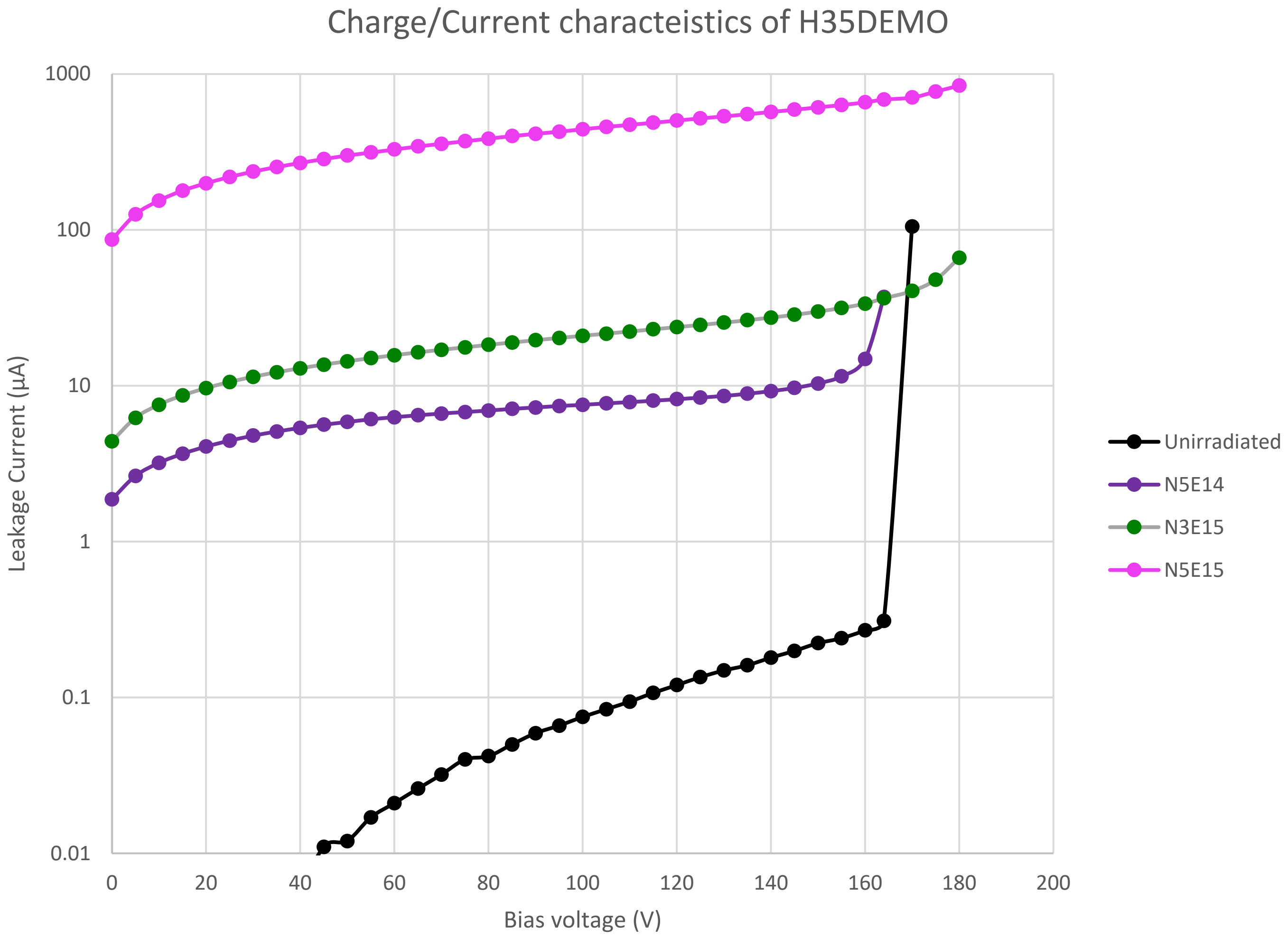
Average peak
25.51 mV

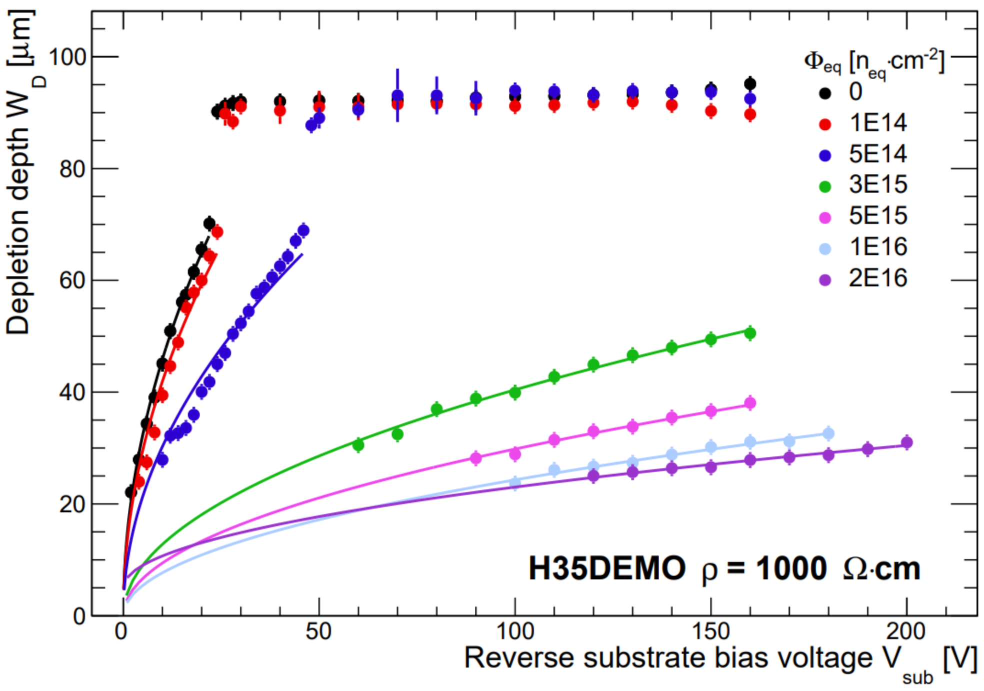
$$\frac{X - ray\ (5.9\ keV)}{e - h\ production\ (3.6\ eV)} = 1639\ electrons$$

Full Depletion has an average output voltage of 25.51 mV for each hit creating 1639 electrons.

$$Conversion = 64.25\ \frac{\mathrm{e}}{\mathrm{mV}}$$

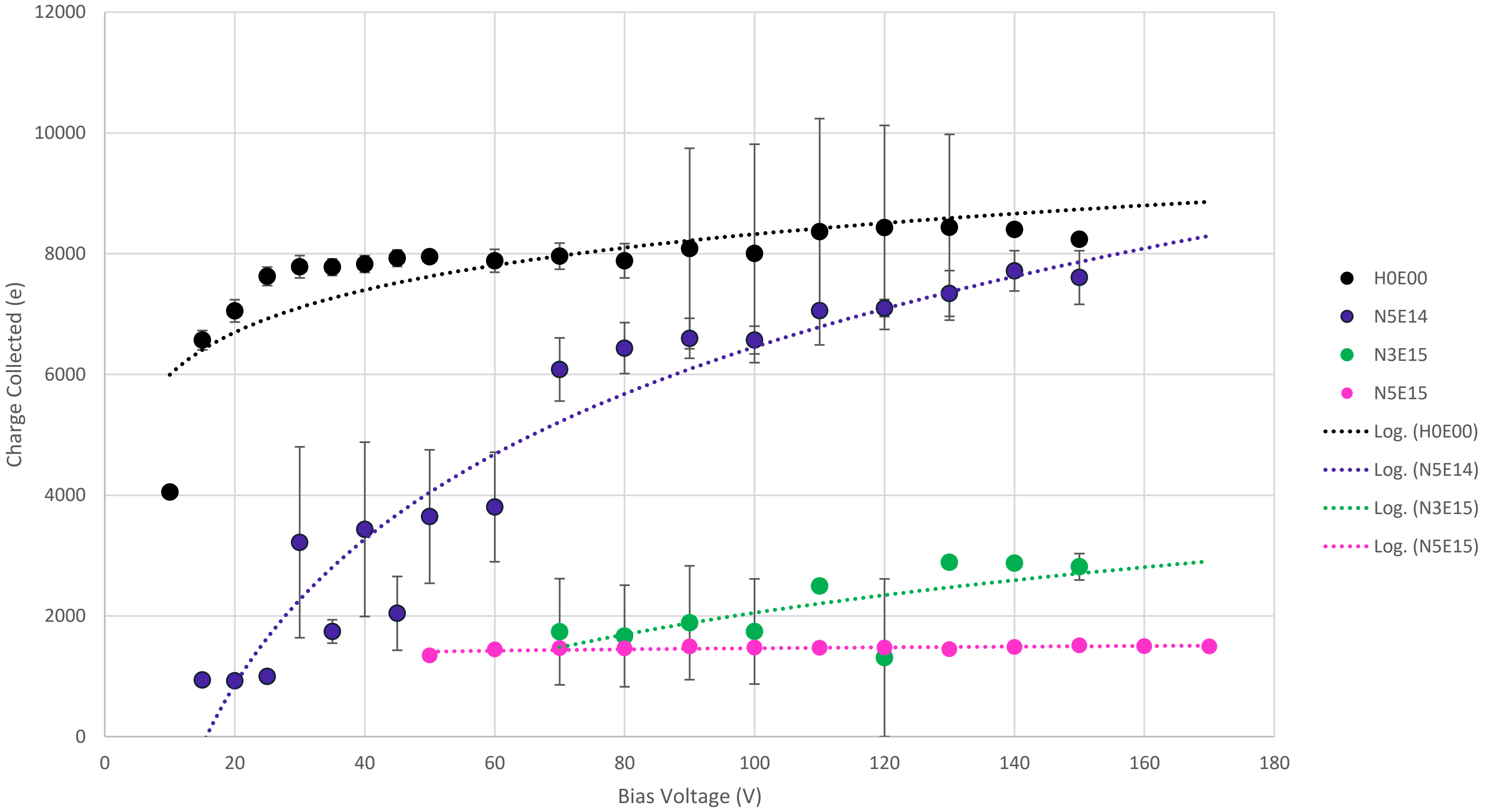
High Voltage Range to Measure



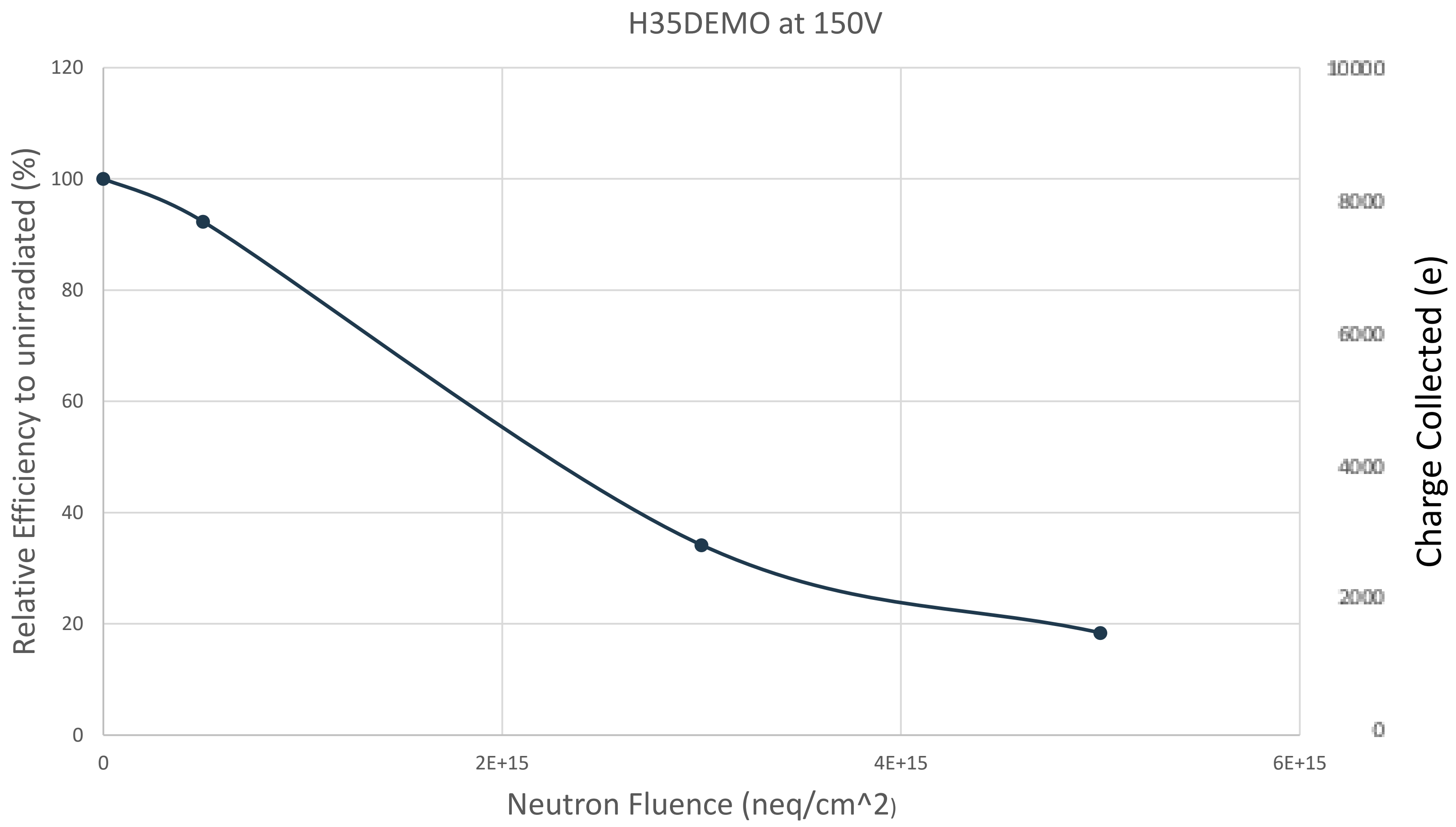


M.Franks et al:
E-TCT characterization of a thinned, backside biased, irradiated HV-CMOS pixel test structure
https://doi.org/10.1016/j.nima.2020.164949

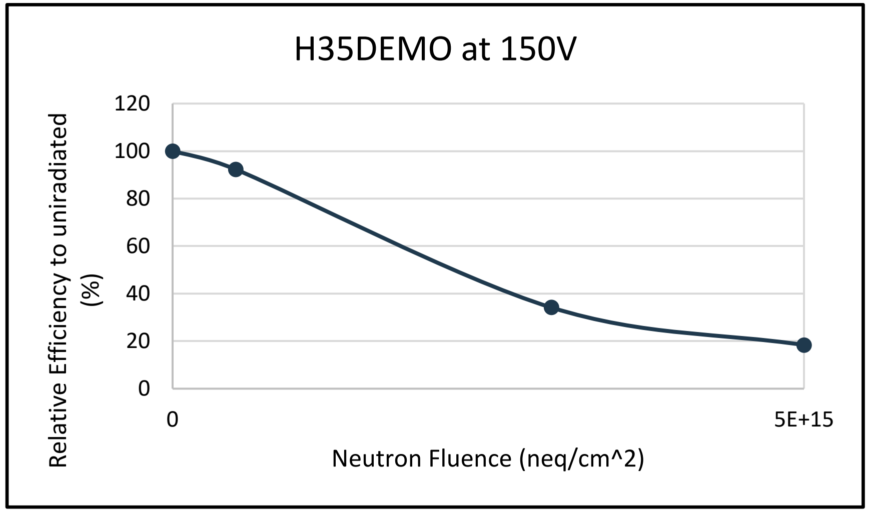
Charge Collection Efficiency dependence on fluence



Charge Collection Efficiency dependence on fluence



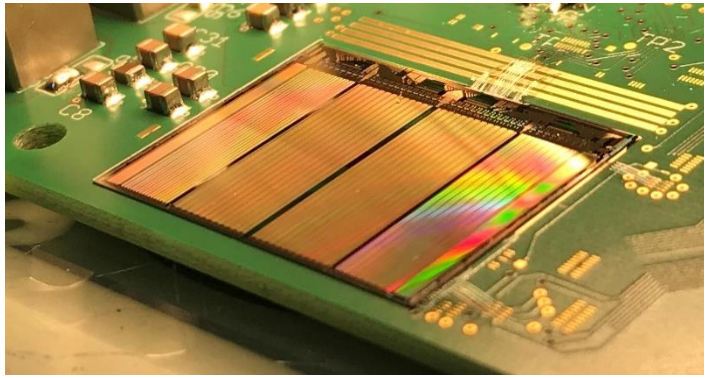
Summary and Goals



At Liverpool we have established and tested apparatus for measuring the charge collection efficiencies of irradiated sensors.

We have investigated the charge collection efficiencies of the a high resistivity, thinned and backside biased HV-CMOS sensor to fluences comparable to that inside large high energy physics experiments.

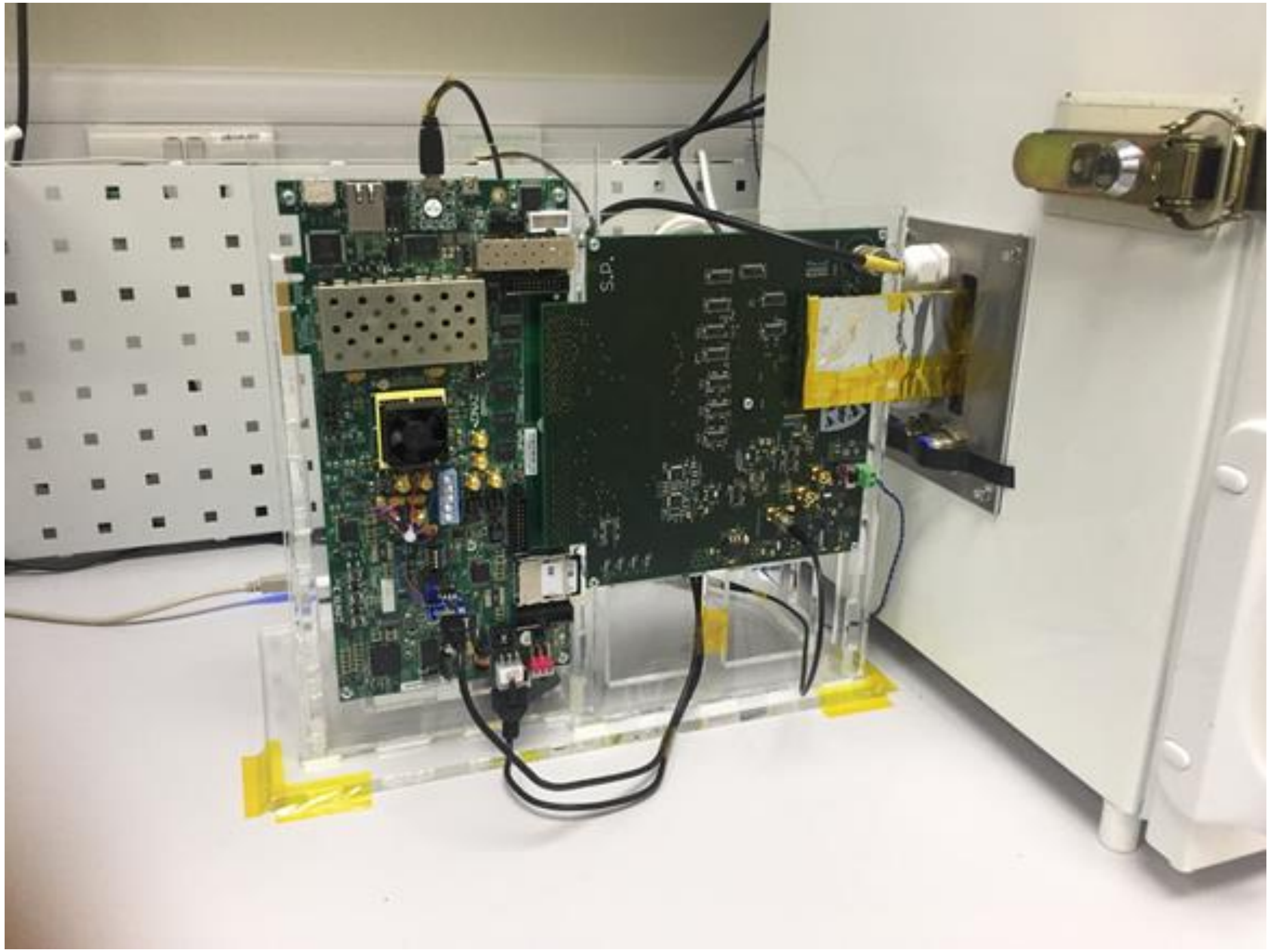
This experiment is ongoing and we have fluences up of $1 \times 10^{16} \frac{n_{eq}}{cm^2}$ and $2 \times 10^{16} \frac{n_{eq}}{cm^2}$ still to test



Thank you all for listening!

Any Questions?

DAC settings

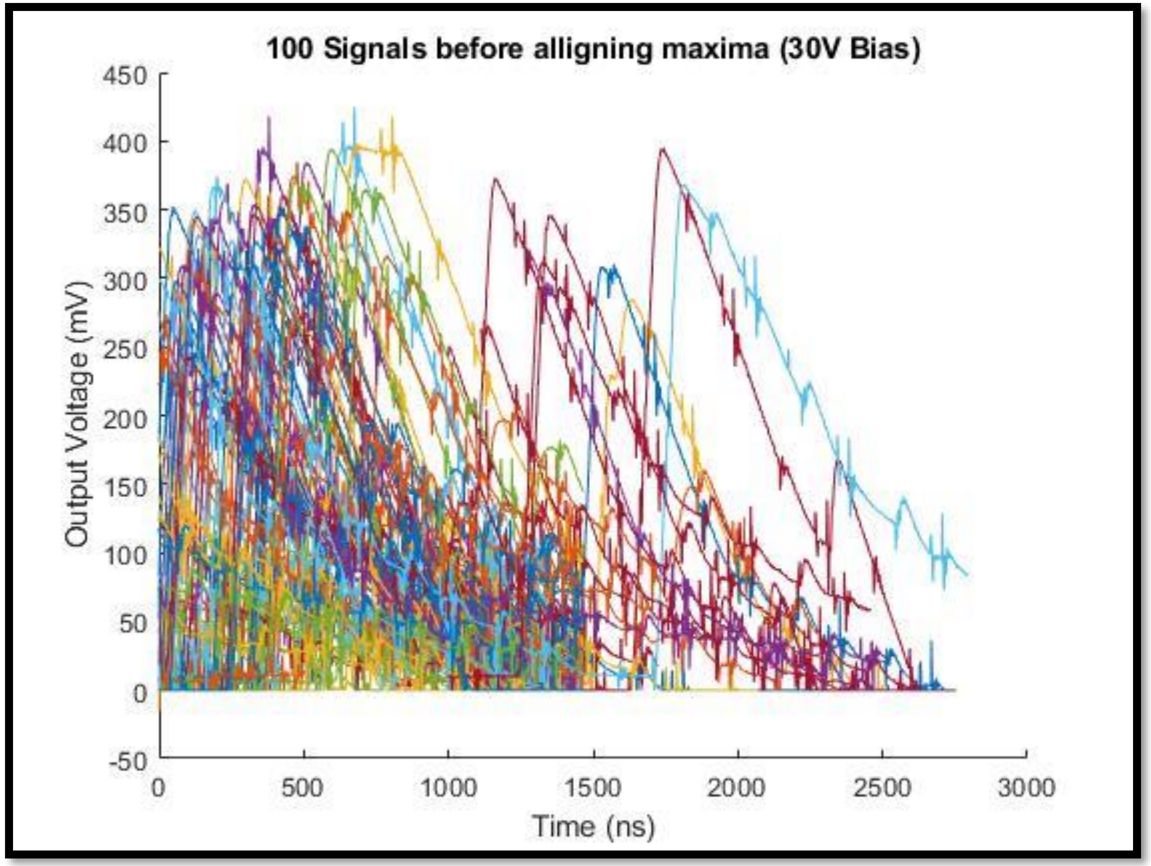


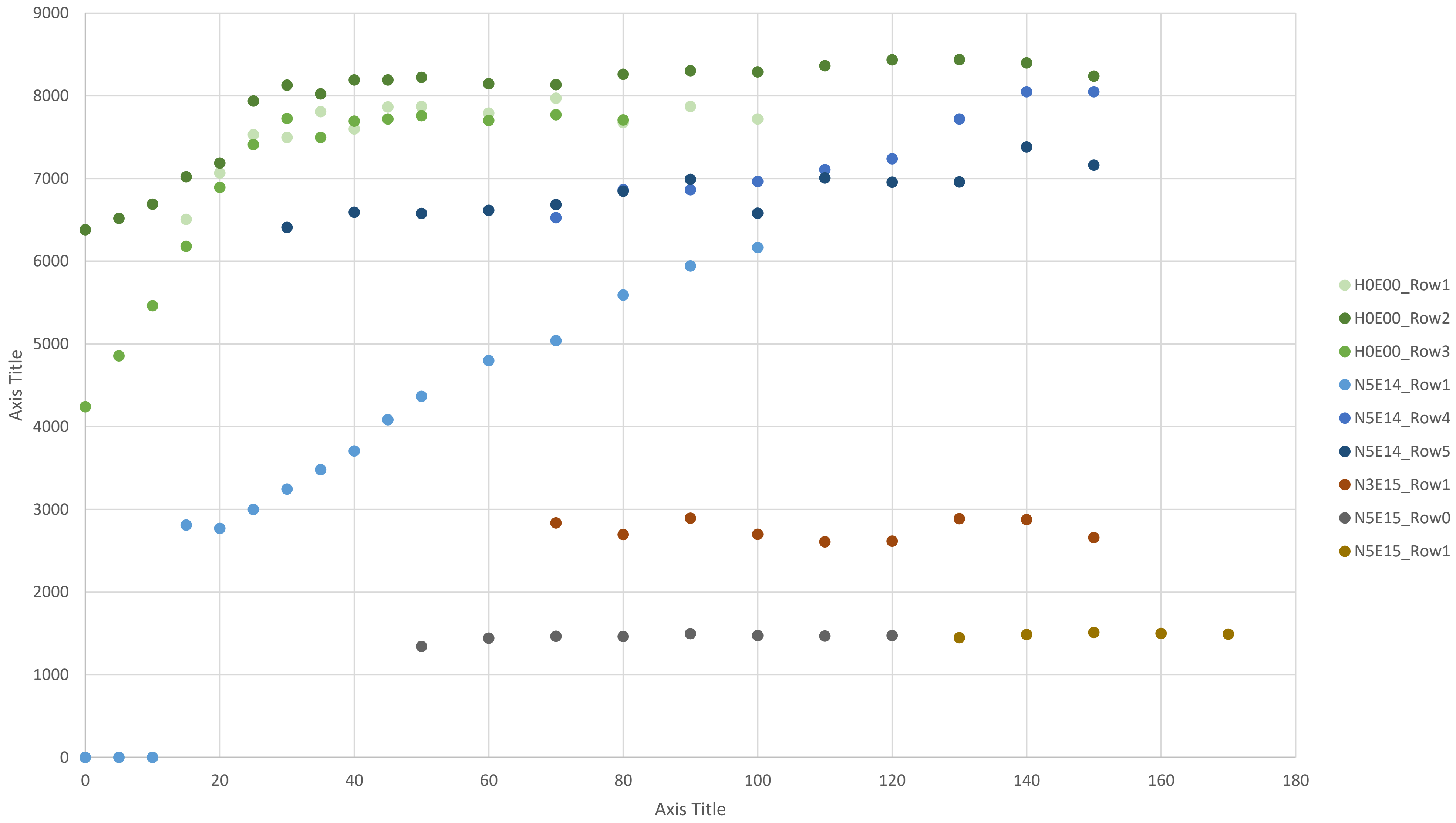
DAC	Use	Value
6	BLR	15
7	VPAB	5
8	VNFB	40
12	VNLogic	1
13	VPLoad	24
14	VNSF	15
15	VP	50
16	VPAB	60

PMT removal

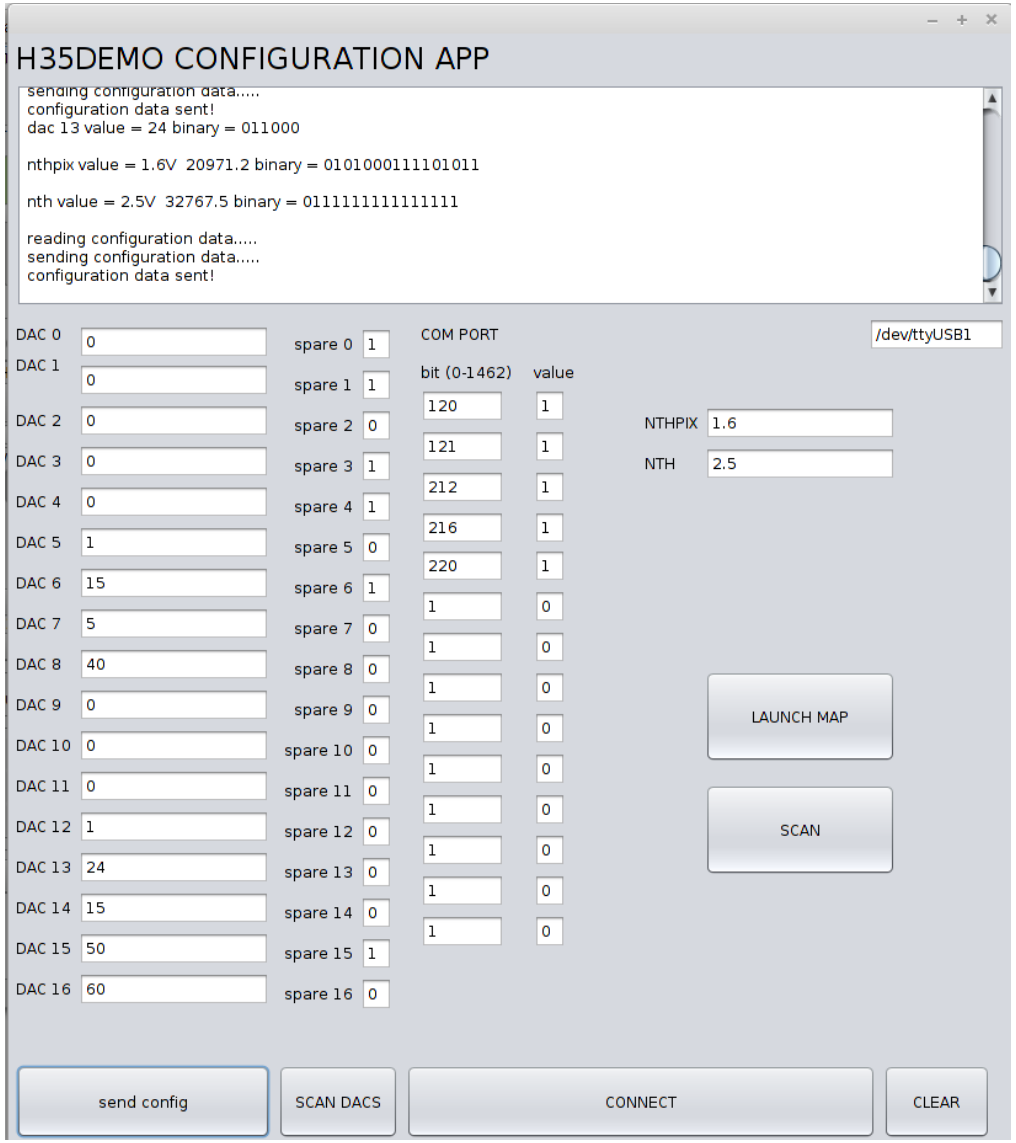
It was chosen to trigger on the analogue output after the following was observed:

- The PMT would trigger when a particle went through an unwanted pixel creating more useless data.
- Good hits were often made unusable by a time delay which caused a section of the waveform to be lost outside of the trigger window




9000
8000
7000
6000
5000
4000
3000
2000
1000
0
Axis Title
0
20
40
60
80
100
120
140
160
180
Axis Title
H0E00_Row1
H0E00_Row2
H0E00_Row3
N5E14_Row1
N5E14_Row4
N5E14_Row5
N3E15_Row1
N5E15_Row0
N5E15_Row1

Pk-Pk [CH3]:
23.4 mV
Min 13.300
Max 215.400
Mean 27.742
Std 11.4436
N 1000
20 mV/div 20 mV/div 20 mV/div 20 mV/div
1 Acq/s
0.010 V 1093 ns
500 ns/div 641 MS/s Calib



H35DEMO CONFIGURATION APP
sending configuration data.....
configuration data sent!
dac 13 value = 24 binary = 011000
nthpix value = 1.6V 20971.2 binary = 0101000111101011
nth value = 2.5V 32767.5 binary = 0111111111111111
reading configuration data.....
sending configuration data.....
configuration data sent!
DAC 0 0
DAC 1 0
DAC 2 0
DAC 3 0
DAC 4 0
DAC 5 1
DAC 6 15
DAC 7 5
DAC 8 40
DAC 9 0
DAC 10 0
DAC 11 0
DAC 12 1
DAC 13 24
DAC 14 15
DAC 15 50
DAC 16 60
spare 0 1
spare 1 1
spare 2 0
spare 3 1
spare 4 1
spare 5 0
spare 6 1
spare 7 0
spare 8 0
spare 9 0
spare 10 0
spare 11 0
spare 12 0
spare 13 0
spare 14 0
spare 15 1
spare 16 0
COM PORT
/dev/ttyUSB1
bit (0-1462)
value
120 1
121 1
212 1
216 1
220 1
NTHPIX 1.6
NTH 2.5
LAUNCH MAP
SCAN
send config
SCAN DACS
CONNECT
CLEAR

Finding output voltage – charge collected conversion factor

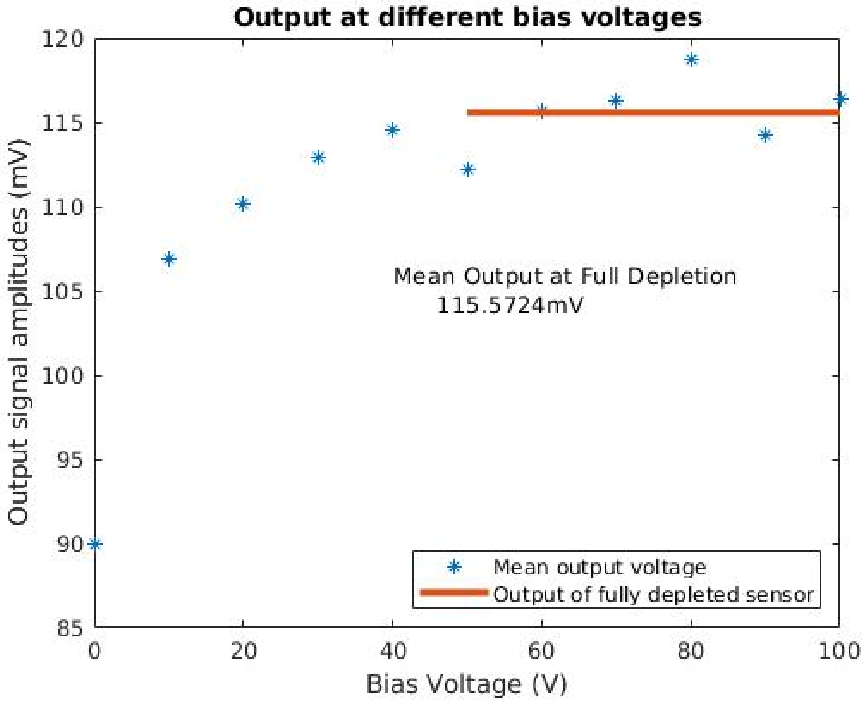
The injection circuit does not use the sensing junction of the sensor and therefore the charge collected should not depend on the bias voltage used.

<u>For Sr90 however:</u>

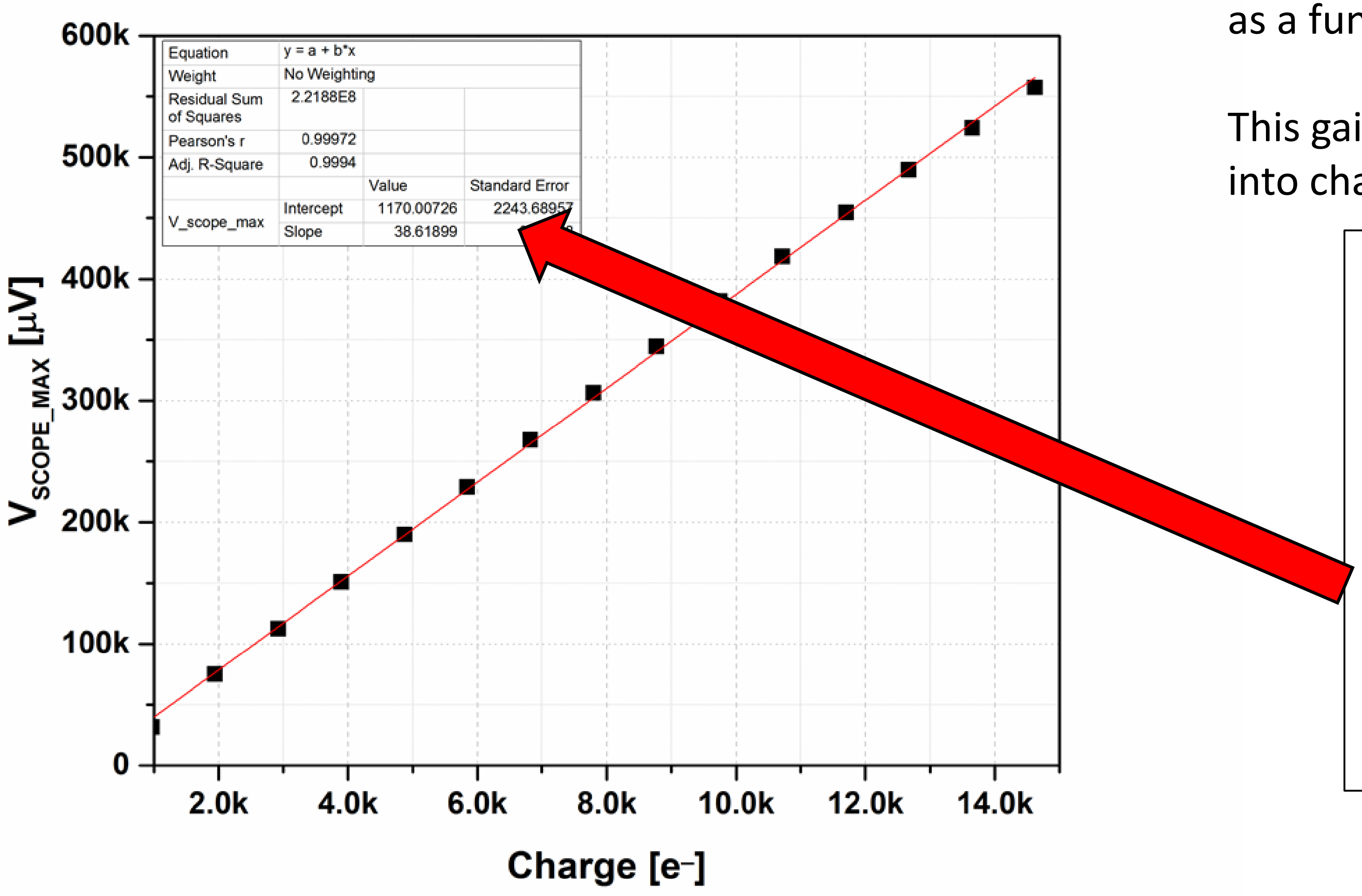
This is what we should expect:

- Sensor reaches a bias voltage where it is fully depleted.

- From eTCT measurements we know the depletion width at these bias voltages



Finding output voltage – charge collected conversion factor



This is a plot from a cadence simulation in which the simulation gives the voltage measured by the scope as a function of the charge collected by the sensor.

This gain will be used to convert all voltage outputs into charge collected.

Where:

$$Q_{detector} = Charge\ in\ pixel$$

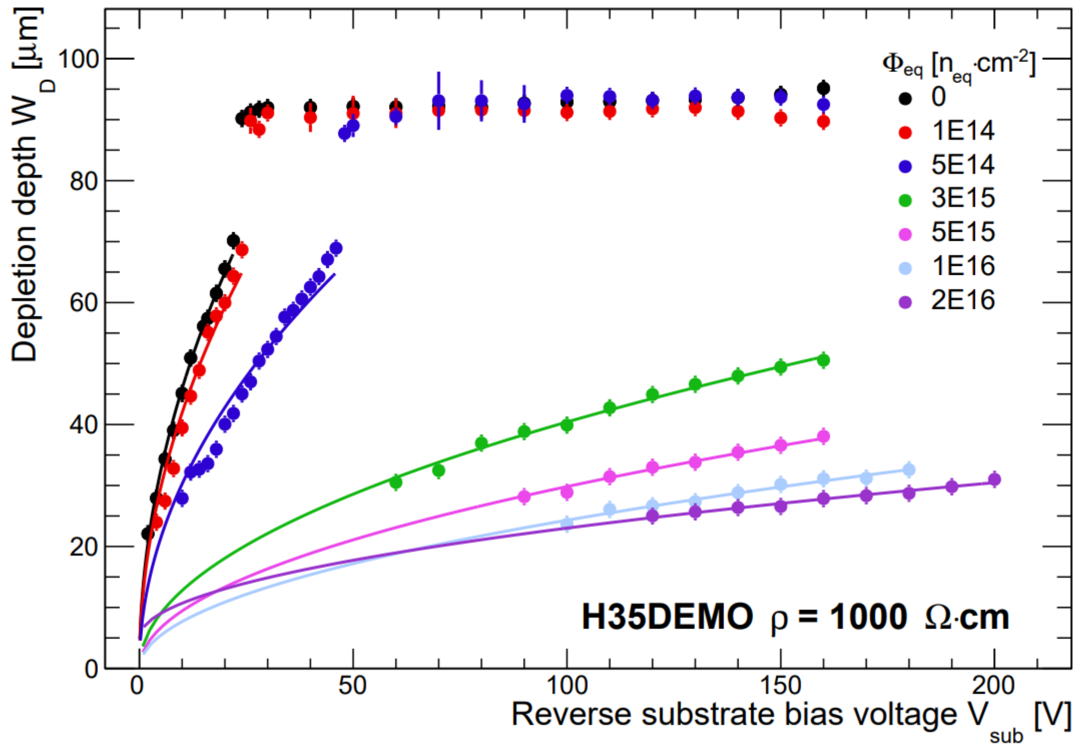
$$C_{detector} = Capacitance\ of\ pixel = 442\ fF$$

$$V_{nw} = voltage\ change\ in\ nwell$$

$$G_{CSA} = gain\ of\ amplifier\ =\ 38.619\frac{\mu V}{e^-}$$

$$e_{detector} = amount\ of\ electrons\ collected$$

Fe55 X-ray Attenuation



M.Franks:
E-TCT characterization of a thinned, backside biased, irradiated HV-CMOS pixel test structure

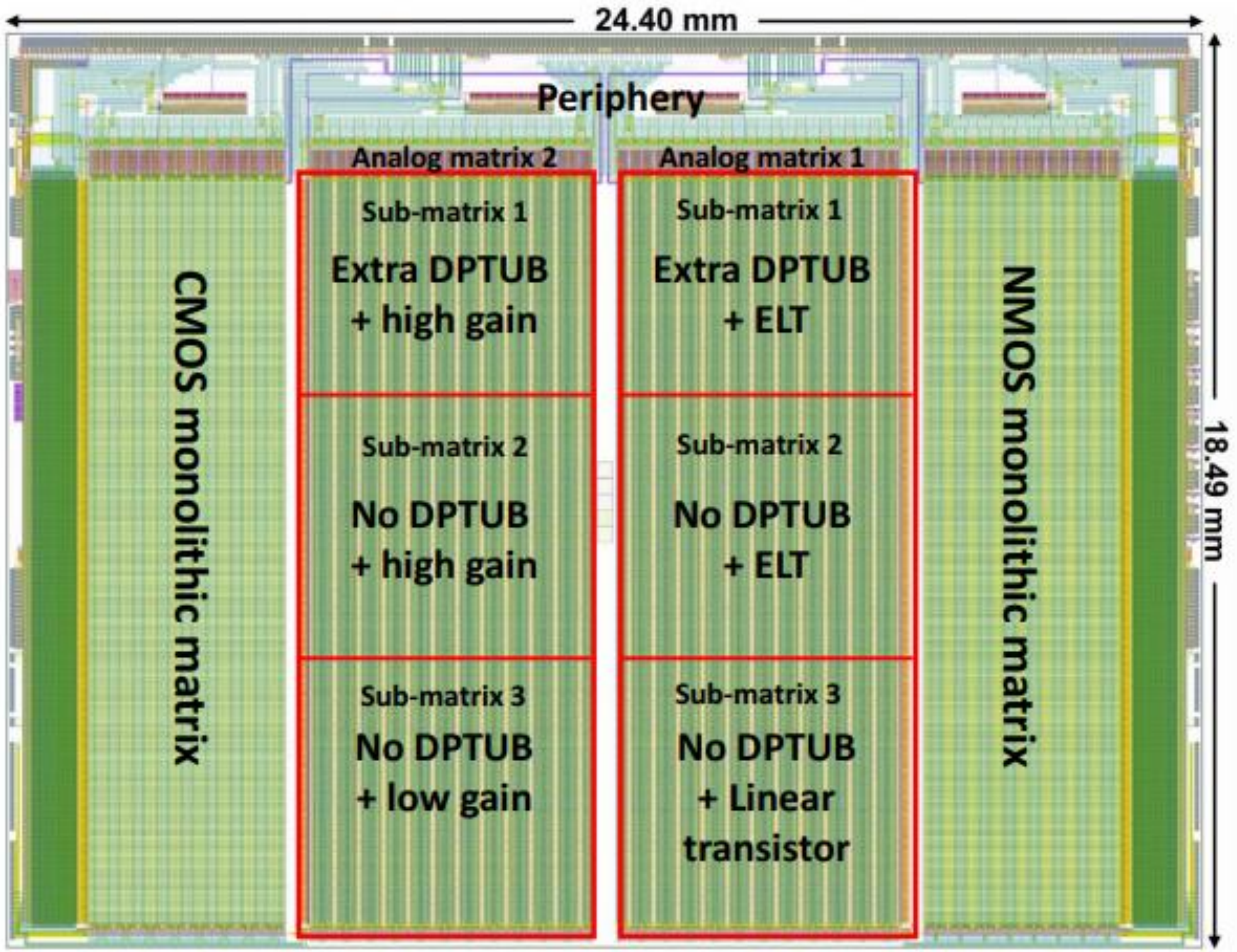
X-ray energy from Fe55 will give a constant energy response.

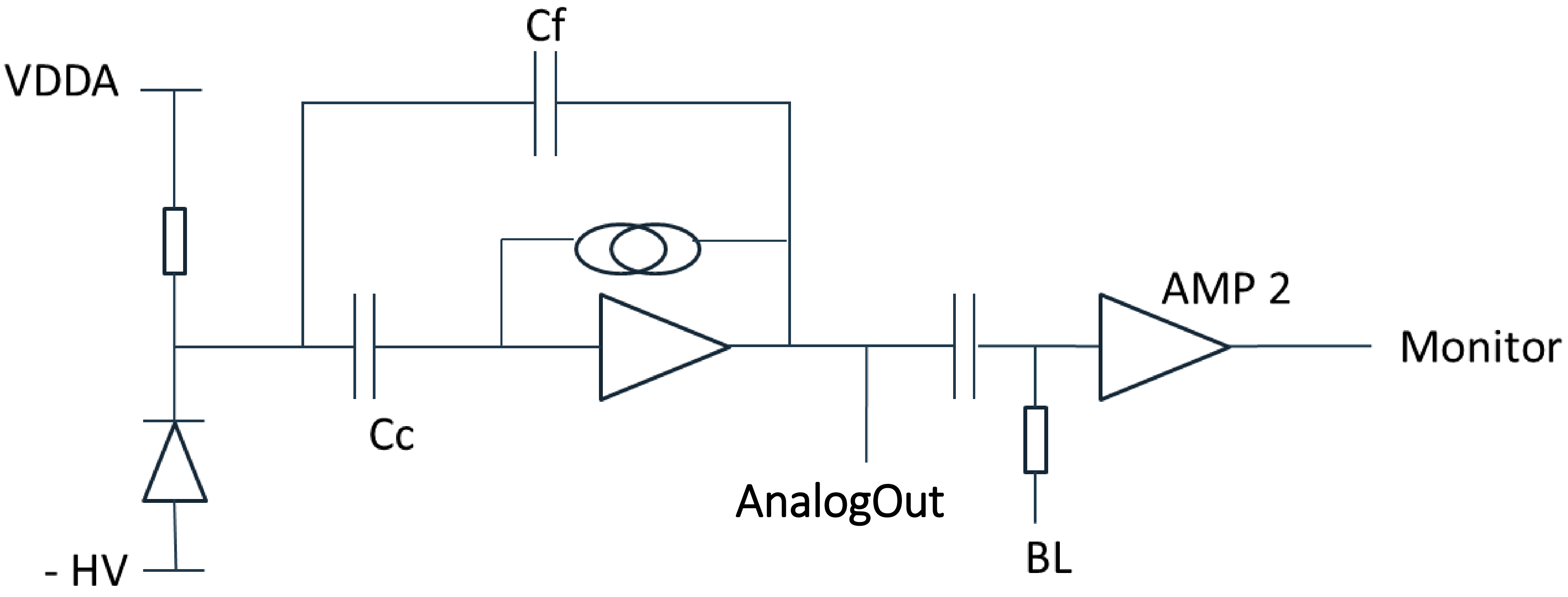
$$Linear\ attenuation \qquad E = E_0\, e^{-\mu x}$$

$$\mu = \sim 147 \frac{cm^2}{g} \times 2.329 \frac{d}{cm^3} = 340\ cm^{-1}$$

$$\frac{E}{E_0} = e^{-340 \times 0.01\ cm} = 0.3 = \sim 3\%\ energy\ remaining$$

97% of energy is deposited into sensor when fully depleted


24.40 mm
Periphery
Analog matrix 2
Analog matrix 1
Sub-matrix 1
Extra DPTUB
+ high gain
Sub-matrix 1
Extra DPTUB
+ ELT
Sub-matrix 2
No DPTUB
+ high gain
Sub-matrix 2
No DPTUB
+ ELT
Sub-matrix 3
No DPTUB
+ low gain
Sub-matrix 3
No DPTUB
+ Linear
transistor
CMOS monolithic matrix
NMOS monolithic matrix
18.49 mm


Cf
VDDA
AMP 2
Monitor
Cc
AnalogOut
BL
- HV