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Charge collection efficiency of a thinned, backside biased, neutron irradiated High Voltage-CMOS active matrix

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Monolithic High Voltage-CMOS (HV-CMOS) sensors are emerging as a prime candidate for tracking systems in future physics experiments. They are designed to be suitable for these challenging environments by integrating the sensing diode and readout ASIC in a single layer of silicon allowing for high bias voltages and using high resistivity substrates. This results in thin detectors with fast charge collection and high radiation tolerance.

The H35DEMO is a demonstrator sensor ASIC in the 0.35 µm HV-CMOS process from AMS and manufactured in a few substrate resistivities between 20 Ω·cm and 1 kΩ·cm. It features four active matrices with 50 µm × 250 µm pixels and different readout electronics flavours. We have thinned a 1 kΩ·cm wafer of H35DEMOs to 100 µm and processed it to allow backside biasing. We have irradiated several of these samples with neutrons up to fluences of 2E16 neq/cm2 to study their radiation tolerance.

In this work, we report initial Charge Collection Efficiency (CCE) measurements of thinned and backside biased H35DEMOs before and after neutron irradiation. For this study, we have used one active matrix of pixels with in-pixel amplification and a Strontium 90 radioactive source.

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