Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

TCAD simulation studies of Fully Depleted Monolithic Active Microstrip Sensors (FD-MAMS) for the ARCADIA project

Lorenzo de Cilladi on behalf of the ARCADIA collaboration

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lorenzo.decilladi@unito.it – ARCADIA FD-MAMS
Fully Depleted Monolithic Active Microstrip Sensors (FD-MAMS)

• Feasibility in a commercial fabrication process
• New and cost-effective solution for tracking and timing
• Particle, nuclear, space, medical applications

• Synopsys Sentaurus TCAD 3D simulations
  • Sensor electrical characteristics
  • Signal formation
• Inter-strip region wide enough to host monolithic integrated CMOS electronics
The idea: CMOS monolithic strips sensors

• Microstrips: up to now hybrid
• High spatial resolution, simpler readout, lower power density

• Recent proposals: pixel matrix with strip readout
• Our proposal: strip-shaped CMOS monolithic sensor
  • Upcoming engineering run: 1.2 cm strip length with 25µm and 10µm pitch
• Reduce complexity of detector assembly (no 1-by-1 strip bonding)
ARCADIA sensor

- LFoudny commercial 110nm CMOS process
Depletion

- Collection n-well
- P-well
- Resistive path between collection n-wells
- Undepleted
- Depletion region border
- Fully depleted
- N-wells are isolated
- Sensor is fully depleted

ARCADIA TCAD simulation

Depletion voltage

Graph:

- $I_{well, unbalanced}$
- $V_{dpl}$

Current [A] vs. $|V_{back}|$ [V]

- $10^{-9}$
- $10^{-11}$
- $10^{-13}$
- $10^{-15}$

0 5 10 15 20 25

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Punch through

\[ V_{\text{back}} > V_{\text{pt}} + 4 \text{ V} \]

\( \text{Depletion voltage} \)

\( \text{Punch through voltage} \)
SiO$_2$ and surface damage

Surface damage model: AIDA 2020 D7.4 report

ARCADIA TCAD simulation

With dose

Capacitance [fF/μm]

\( C_{\text{sens}} \)

- dose = 0
- no SiO$_2$ layer

With SiO$_2$

No SiO$_2$

Dose [Mrad]

10$^{-1}$

10$^{0}$

10$^{1}$

10$^{2}$

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Sensor capacitance

Depletion voltage

Punch through voltage
Sensor capacitance

- Expectation: small wells for minimum capacitance
- Confirmed for n-wells
- Smallest p-well is not necessarily best option, especially at larger pitches
Operating ranges

ARCADIA TCAD simulation

- no dpw
- with dpw
- $V_{pt}$
- $V_{dpi}$

Voltage [V]

Gap size [μm]

Smaller (deep) p-well
Transient simulations

Reduced simulation domain

Central incidence

Edge incidence

Particle
Electric field and potential, signals
Charge collection time

Small (deep) p-wells

Higher operating voltage

Stronger electric field

Faster and more uniform charge collection

• Optimised geometry $\rightarrow$ 95% charge collection in
  • $\sim$ 1.6 ns (with deep p-well)
  • $\sim$ 1.2 ns (without deep p-well)
Charge collection time

- Vertical line: max gap size for CMOS electronics integration between adjacent strips
Enhancements for fast timing

- Larger V\textsubscript{Nwell}

0.8V (default)
Enhancements for fast timing

Larger Vnwell

ARCADIA TCAD simulation
- no dpw
- with dpw
- Vpf
- Vdp

0.8V (default)
Heavy ion nuclei

- 95% collection time raises by 300-400ps over a factor 100 increase in LET
- Never > 2 ns with 50μm thick sensors

Geant4: https://github.com/mcentis/muonOnSilicon
Charge sharing

300μm thick sensors

Central incidence

Cluster size [strips]

Linear Energy Transfer [10^-5 pC/μm]

Central incidence

Edge incidence
Conclusions

• Selected 10 µm pitch fully depleted MAMS

<table>
<thead>
<tr>
<th>Version 1</th>
<th>Optimised for fast timing</th>
<th>With deep p-wells</th>
</tr>
</thead>
<tbody>
<tr>
<td>Version 2</td>
<td>Optimised for fast timing</td>
<td>Without deep p-wells</td>
</tr>
<tr>
<td>Version 3</td>
<td>Large deep p-well for potential inter-strip integrated CMOS electronics</td>
<td></td>
</tr>
</tbody>
</table>

• Operation in full depletion
• Minimum capacitance
  • 0.33fF/µm (0.8V, DC coupling)
  • 0.2 fF/µm (3V, AC coupling)
• First samples available from May 2021

Details on ARCADIA simulations:
• arXiv:2101.09088
• arXiv:2011:09723