Advanced **R**eadout **C**MOS **A**rchitectures with **D**epleted **I**ntegrated sensor **A**rrays

TCAD simulation studies of Fully Depleted Monolithic Active Microstrip Sensors (FD-MAMS) for the ARCADIA project

Lorenzo de Cilladi on behalf of the ARCADIA collaboration

16/02/2021

16th Trento Workshop on Advanced Silicon Radiation Detectors

Fully Depleted Monolithic Active Microstrip Sensors (FD-MAMS)

- Feasibility in a commercial fabrication process
- New and cost-effective solution for tracking and timing
- Particle, nuclear, space, medical applications

- Synopsys Sentaurus TCAD 3D simulations
  - Sensor electrical characteristics
  - Signal formation
- Inter-strip region wide enough to host monolithic integrated CMOS electronics

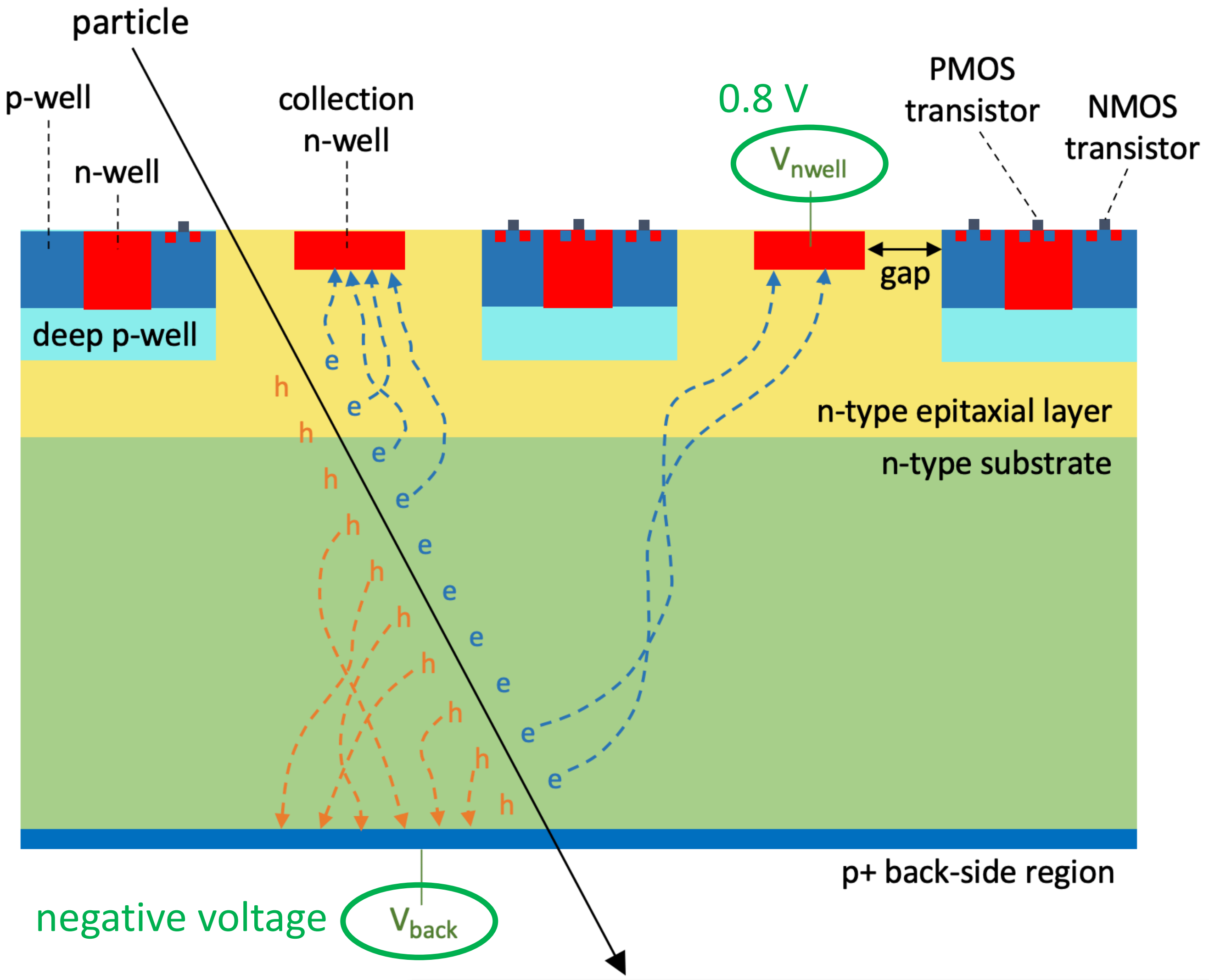
The idea: CMOS monolithic strips sensors

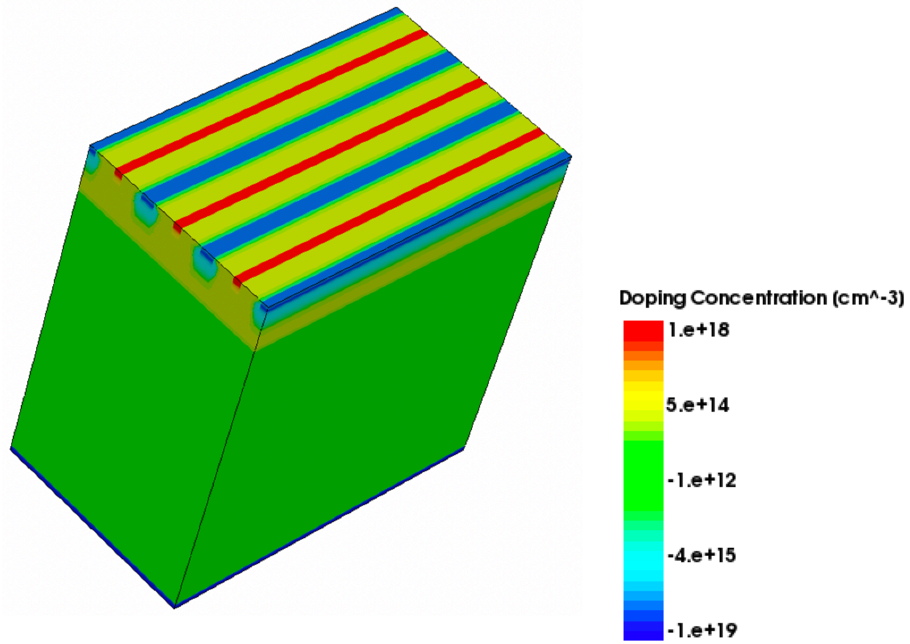
- Microstrips: up to now hybrid
- High spatial resolution, simpler readout, lower power density

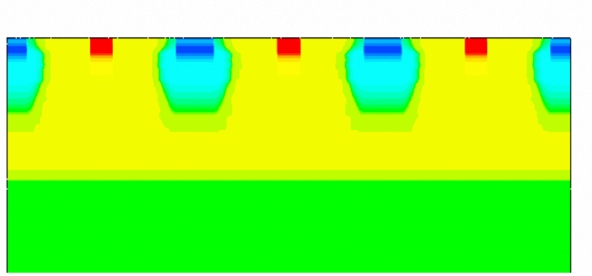
- Recent proposals: pixel matrix with strip readout
- Our proposal: strip-shaped CMOS monolithic sensor
  - Upcoming engineering run: **1.2 cm strip length** with **25μm and 10μm pitch**
- Reduce complexity of detector assembly (no 1-by-1 strip bonding)

ARCADIA sensor

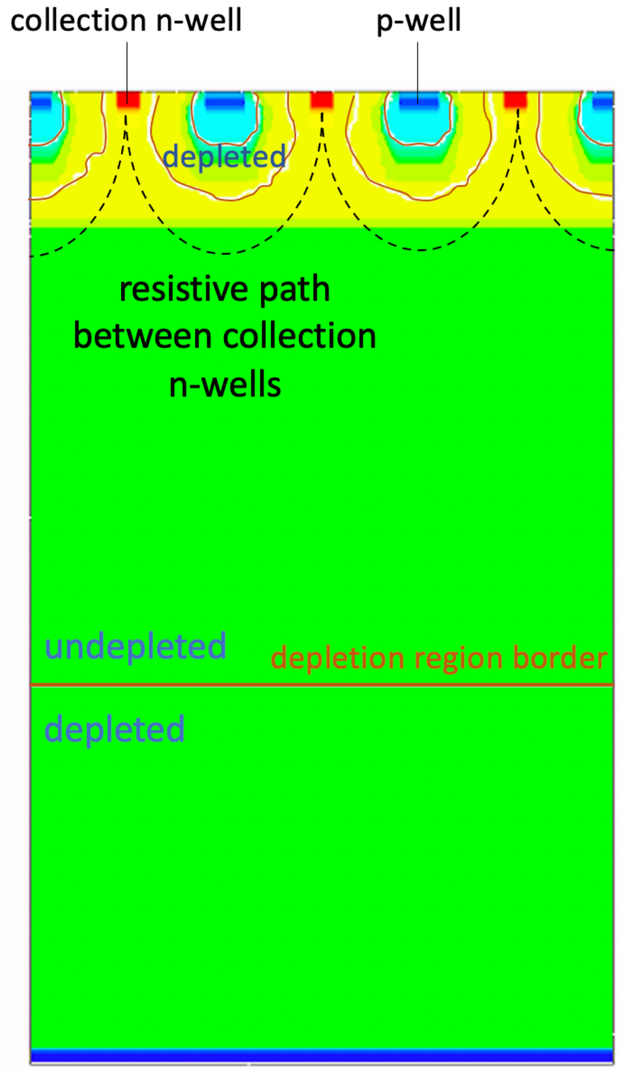
- LFoundry commercial 110nm CMOS process

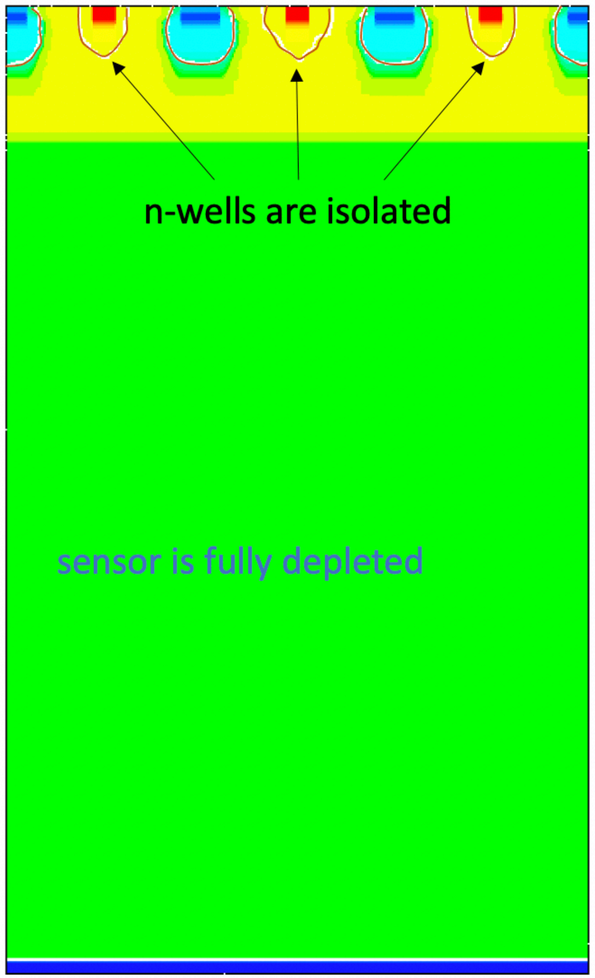


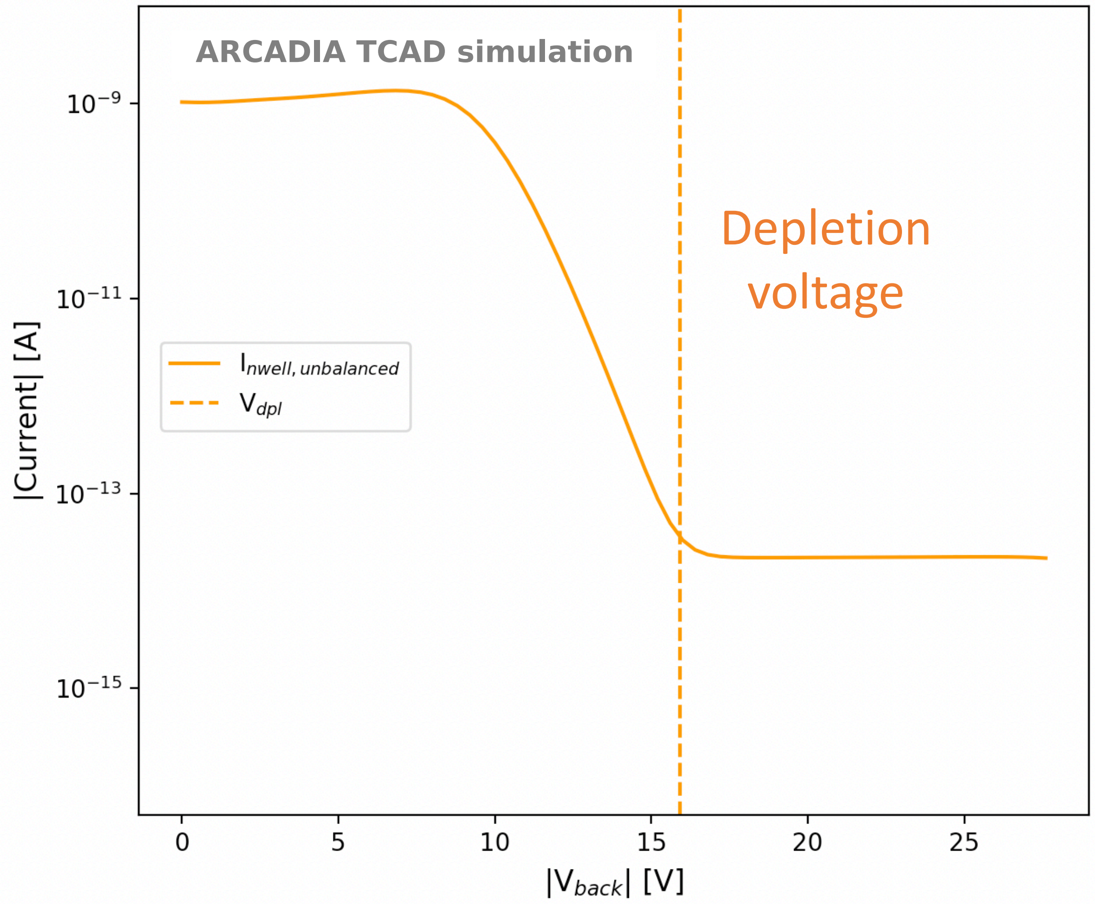




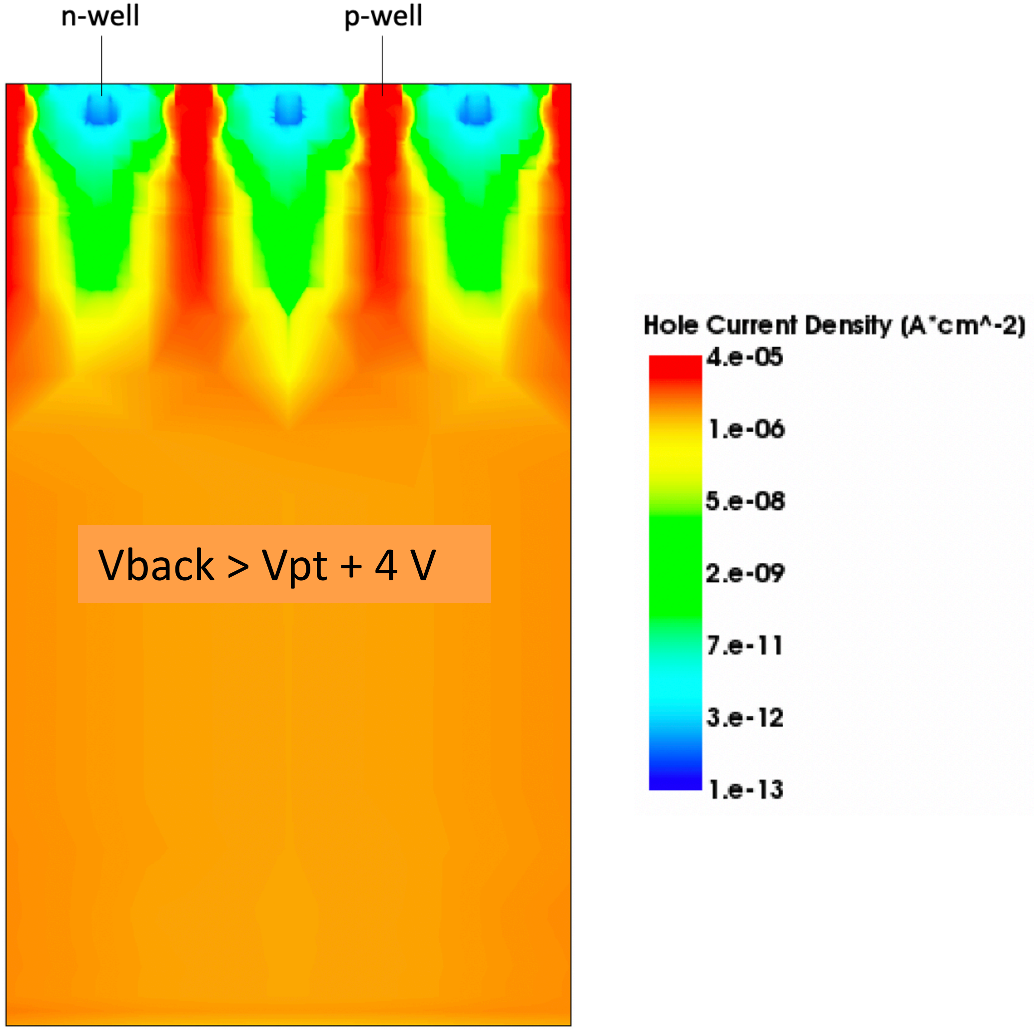
Depletion

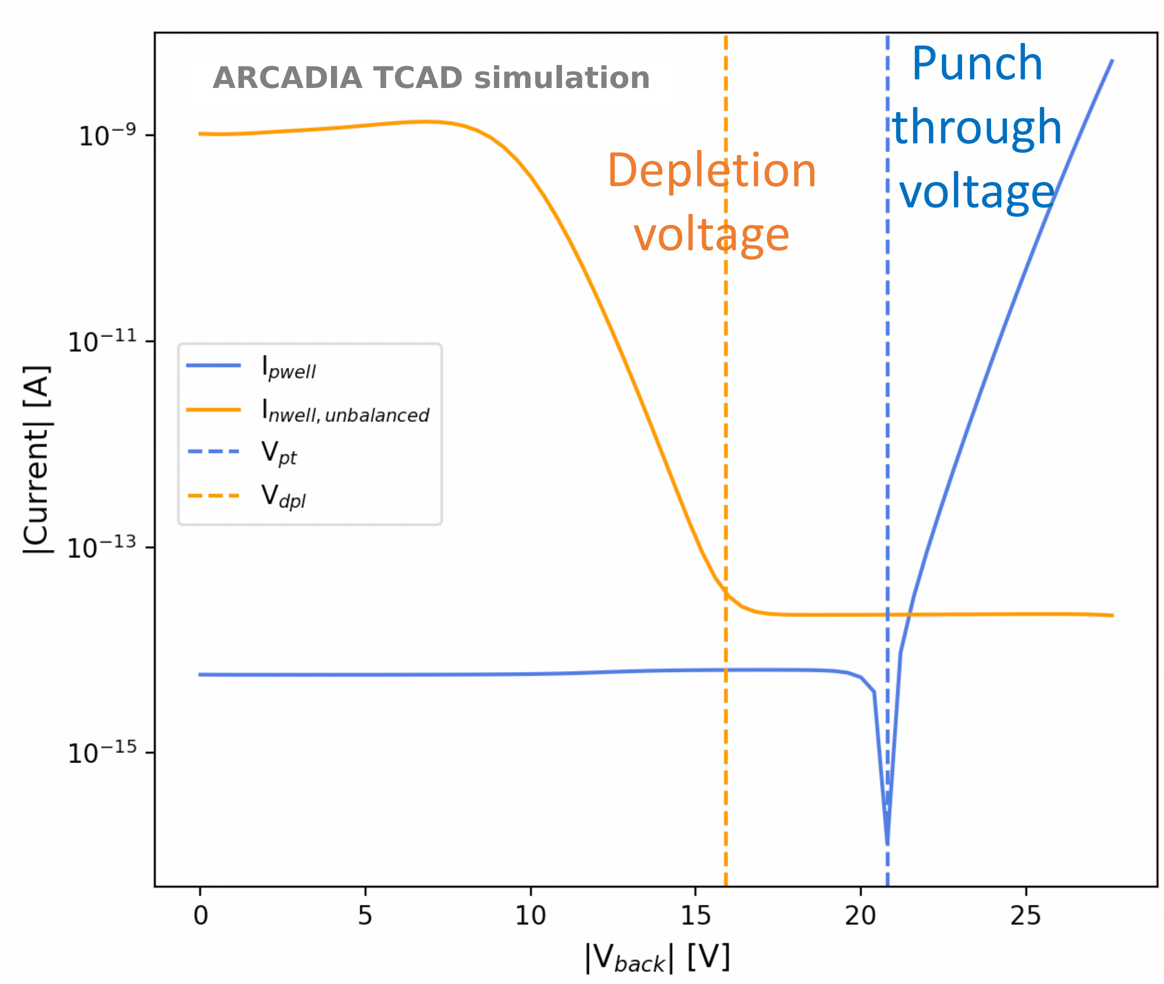

collection n-well
p-well
depleted
resistive path
between collection
n-wells
undepleted
depletion region border
depleted


n-wells are isolated
sensor is fully depleted


ARCADIA TCAD simulation
Depletion
voltage
$I_{nwell, unbalanced}$
V_{dpl}
|Current| [A]
10^{-9}
10^{-11}
10^{-13}
10^{-15}
0
5
10
15
20
25
$|V_{back}|$ [V]

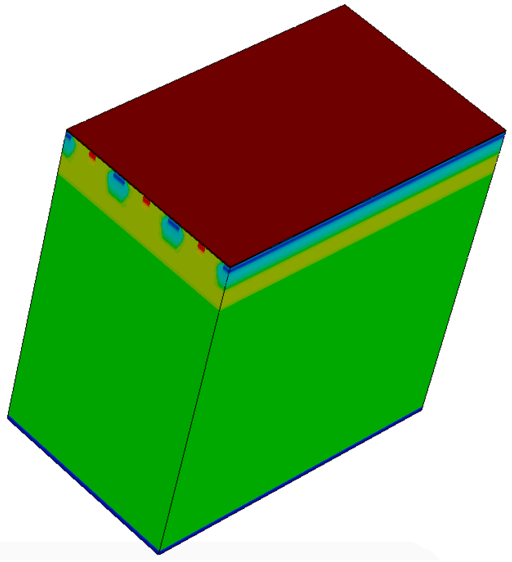
Punch through

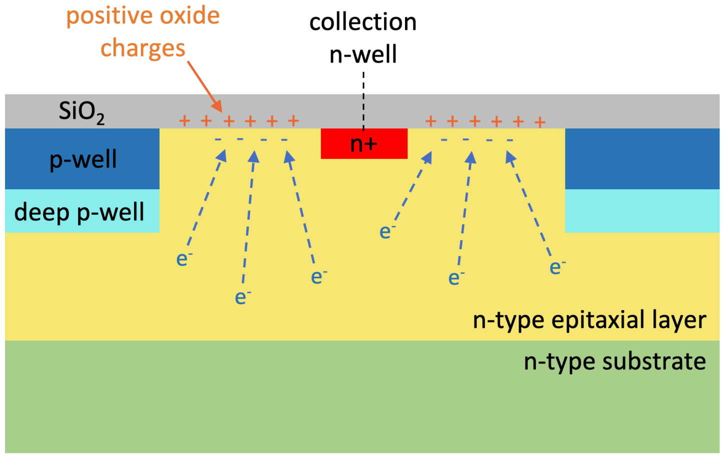


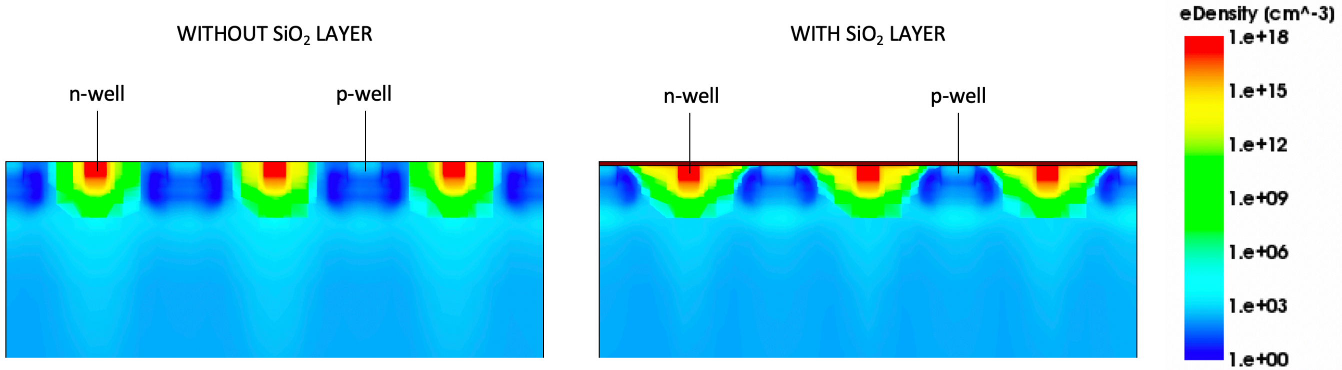


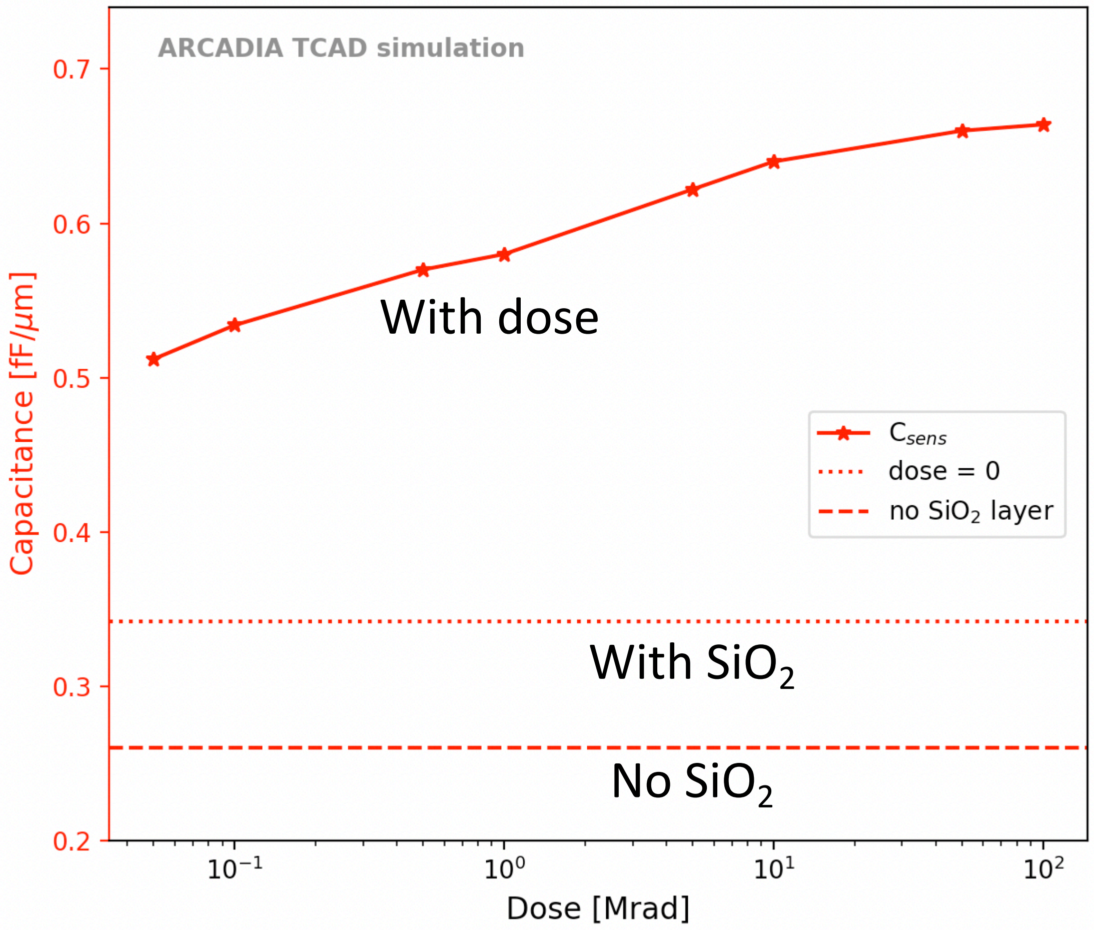
Surface damage model: AIDA 2020 D7.4 report

SiO_2 and surface damage

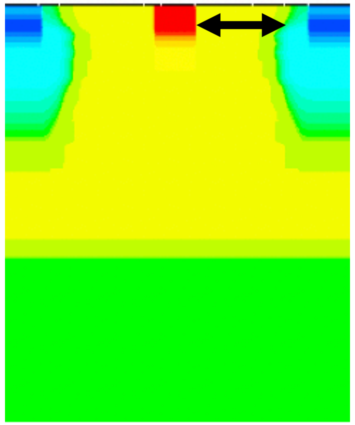


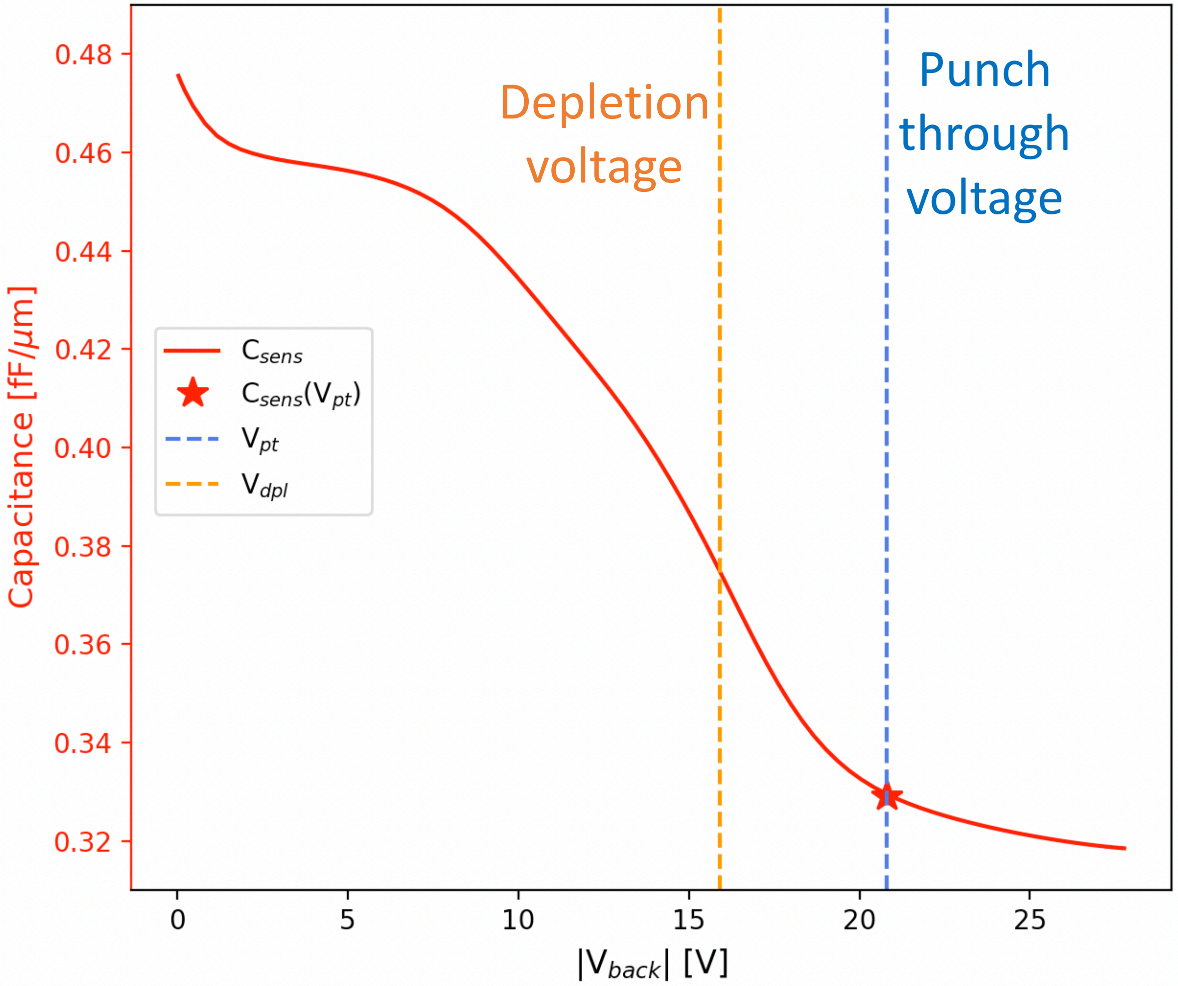




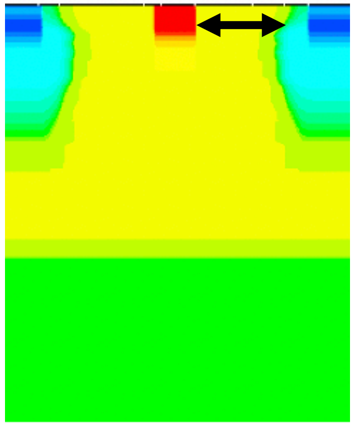


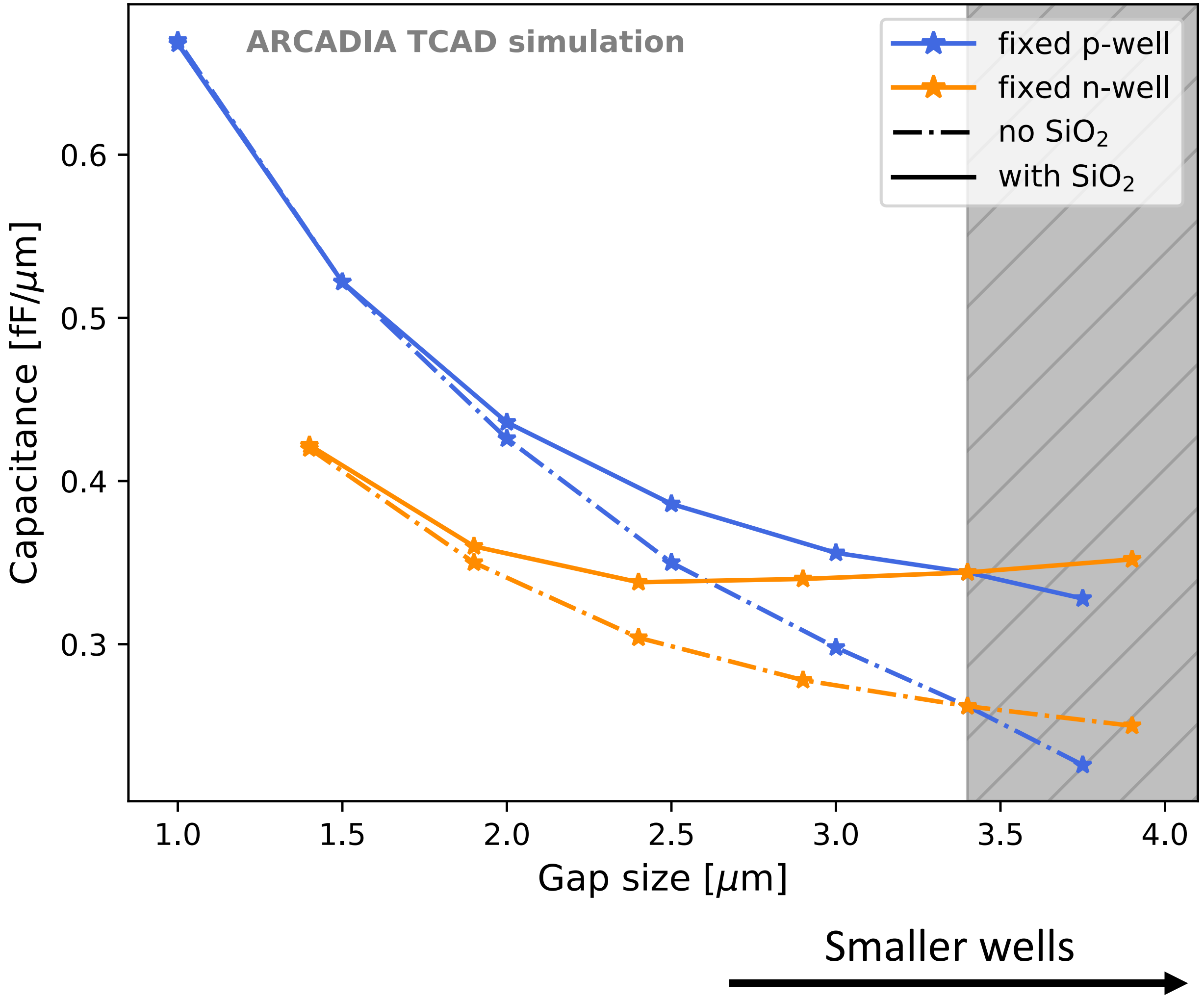
Sensor capacitance





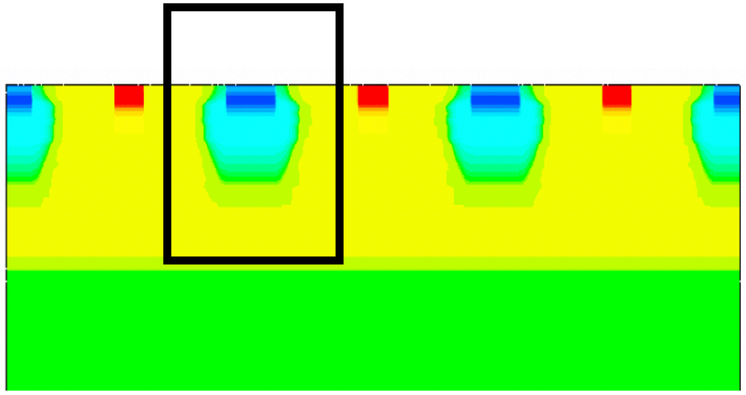
Sensor capacitance

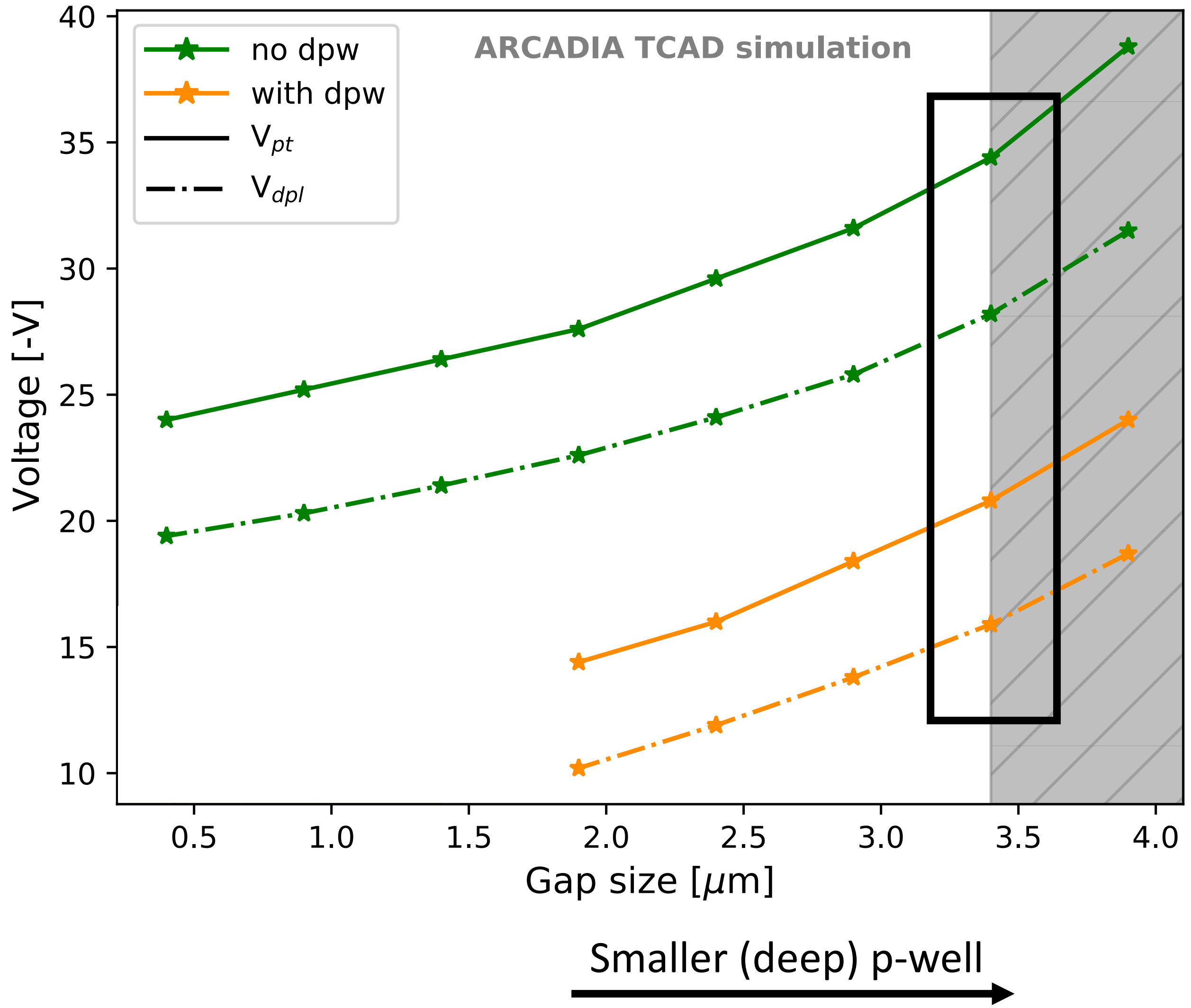




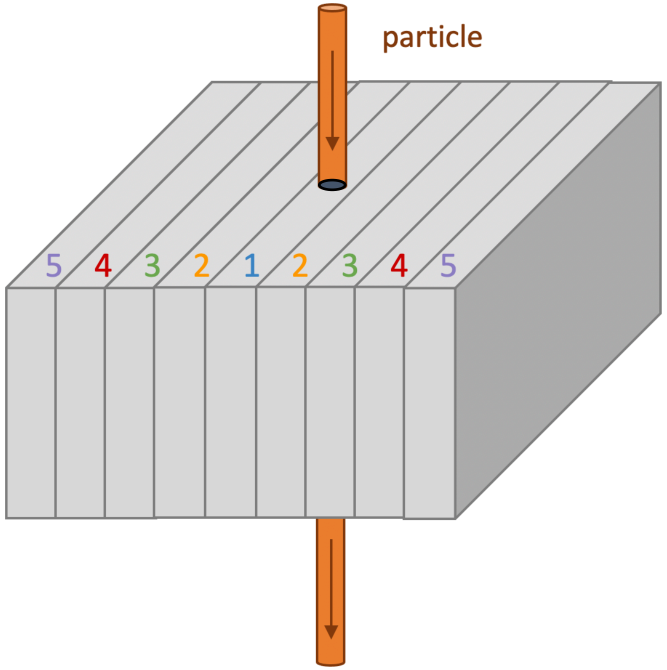
- Expectation: small wells for minimum capacitance
- Confirmed for n-wells
- Smallest p-well is not necessarily best option, especially at larger pitches

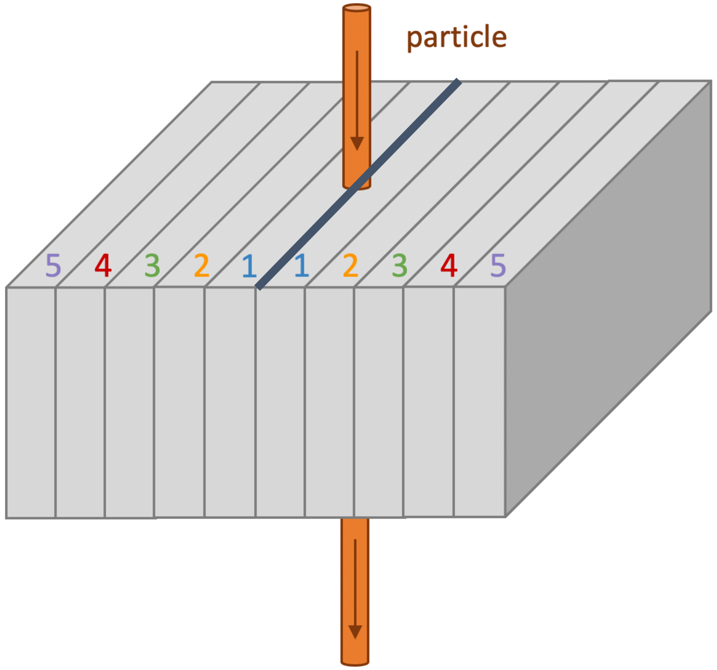
Operating ranges



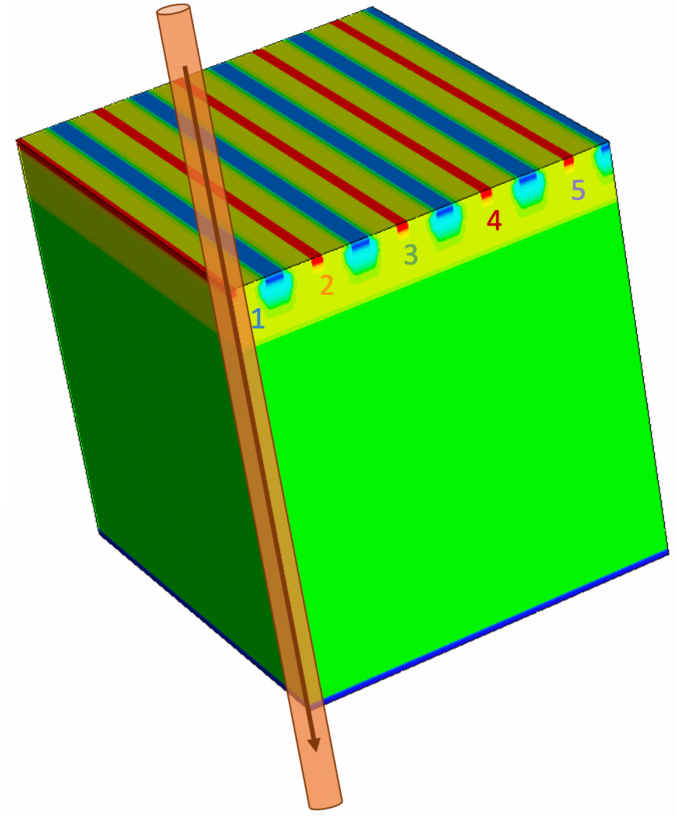


Transient simulations

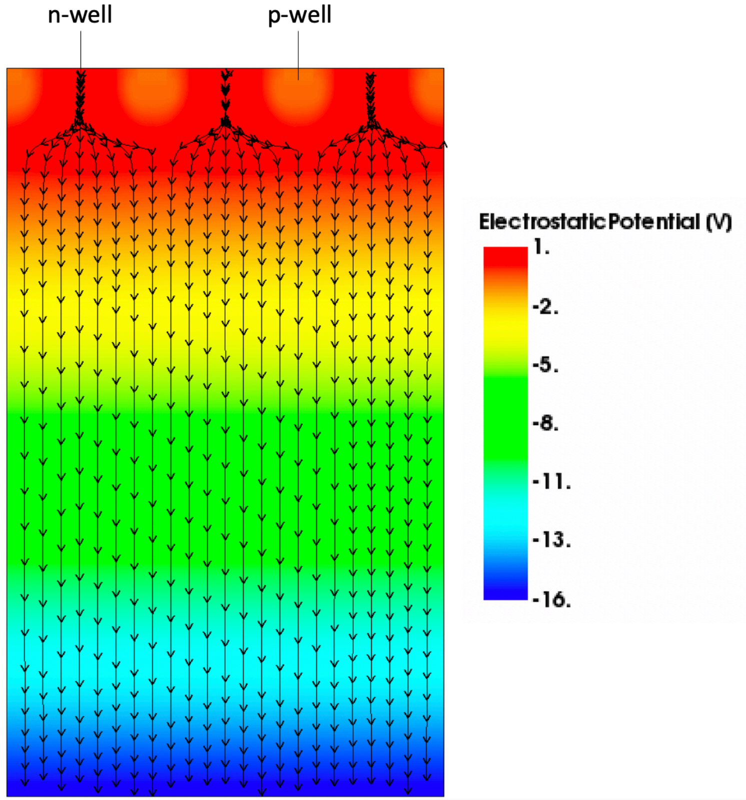


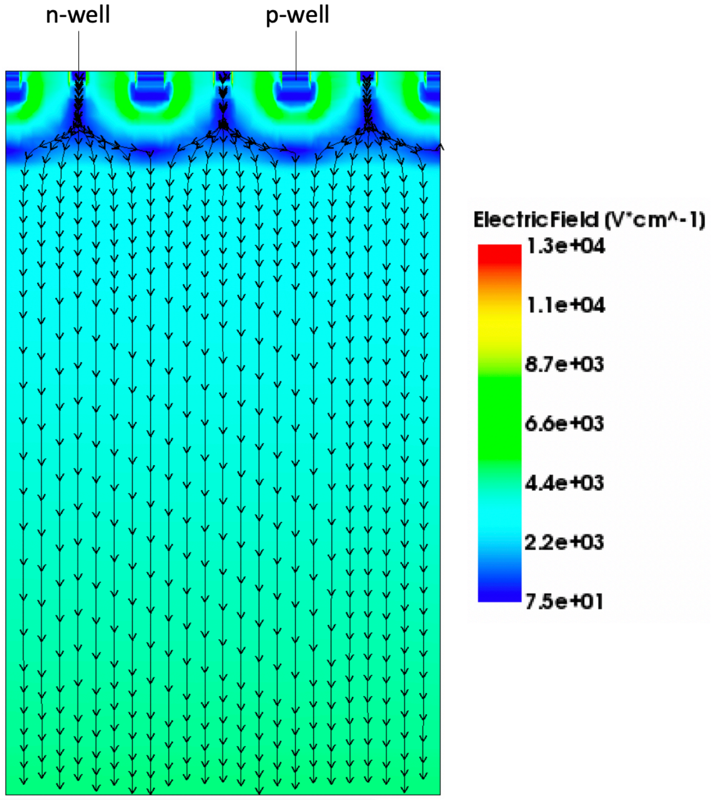


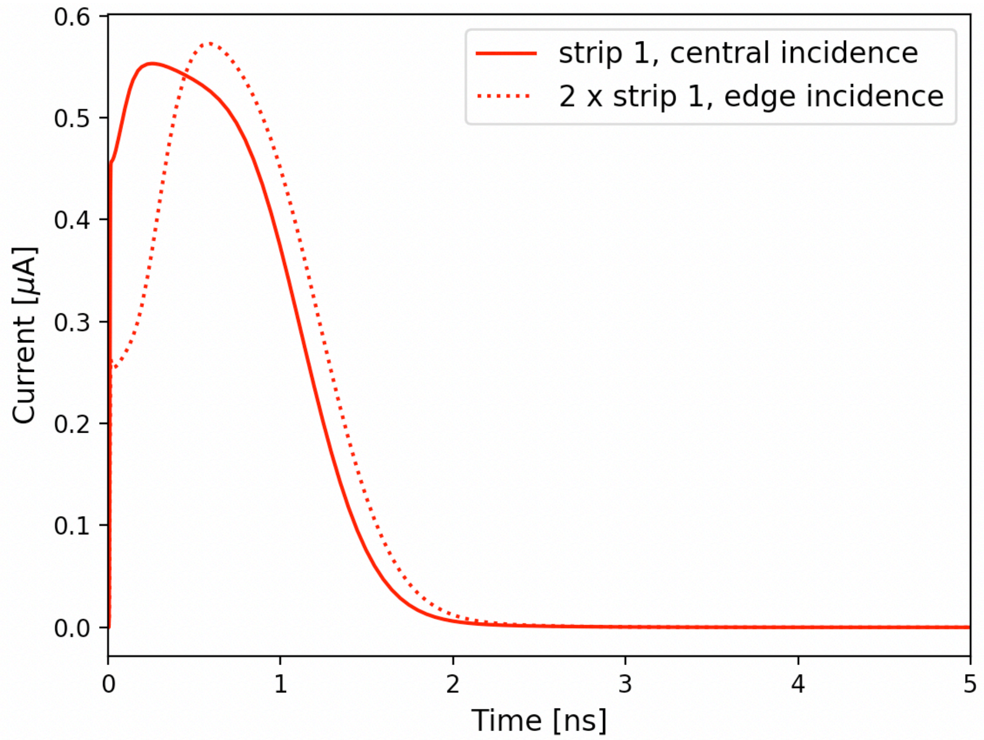
Reduced simulation domain



Electric field and potential, signals







Charge collection time

Small (deep) p-wells

↓

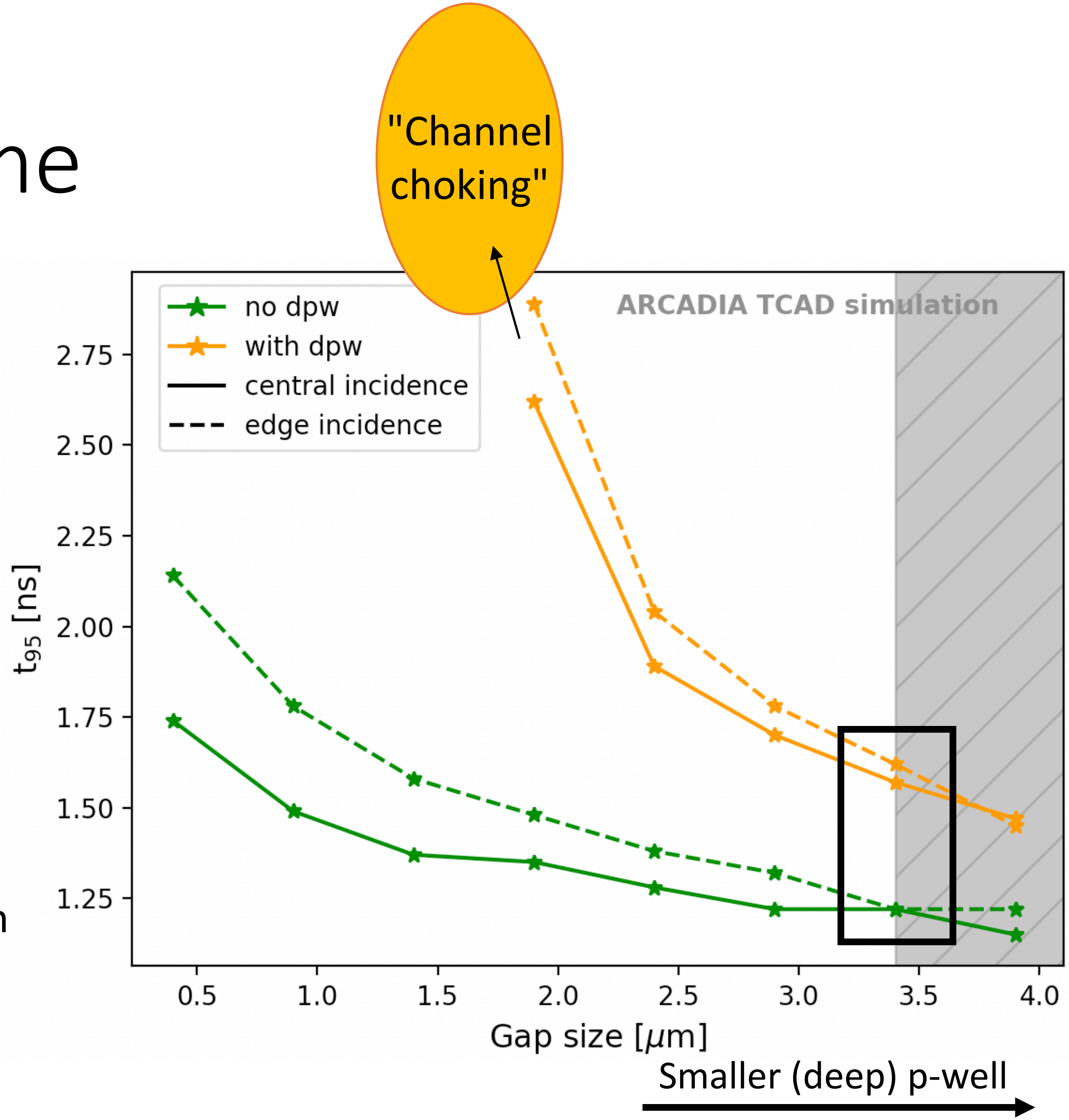
Higher operating voltage

↓

Stronger electric field

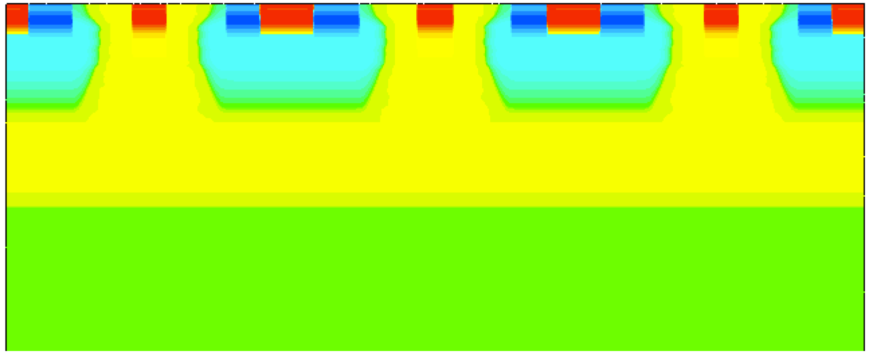
↓

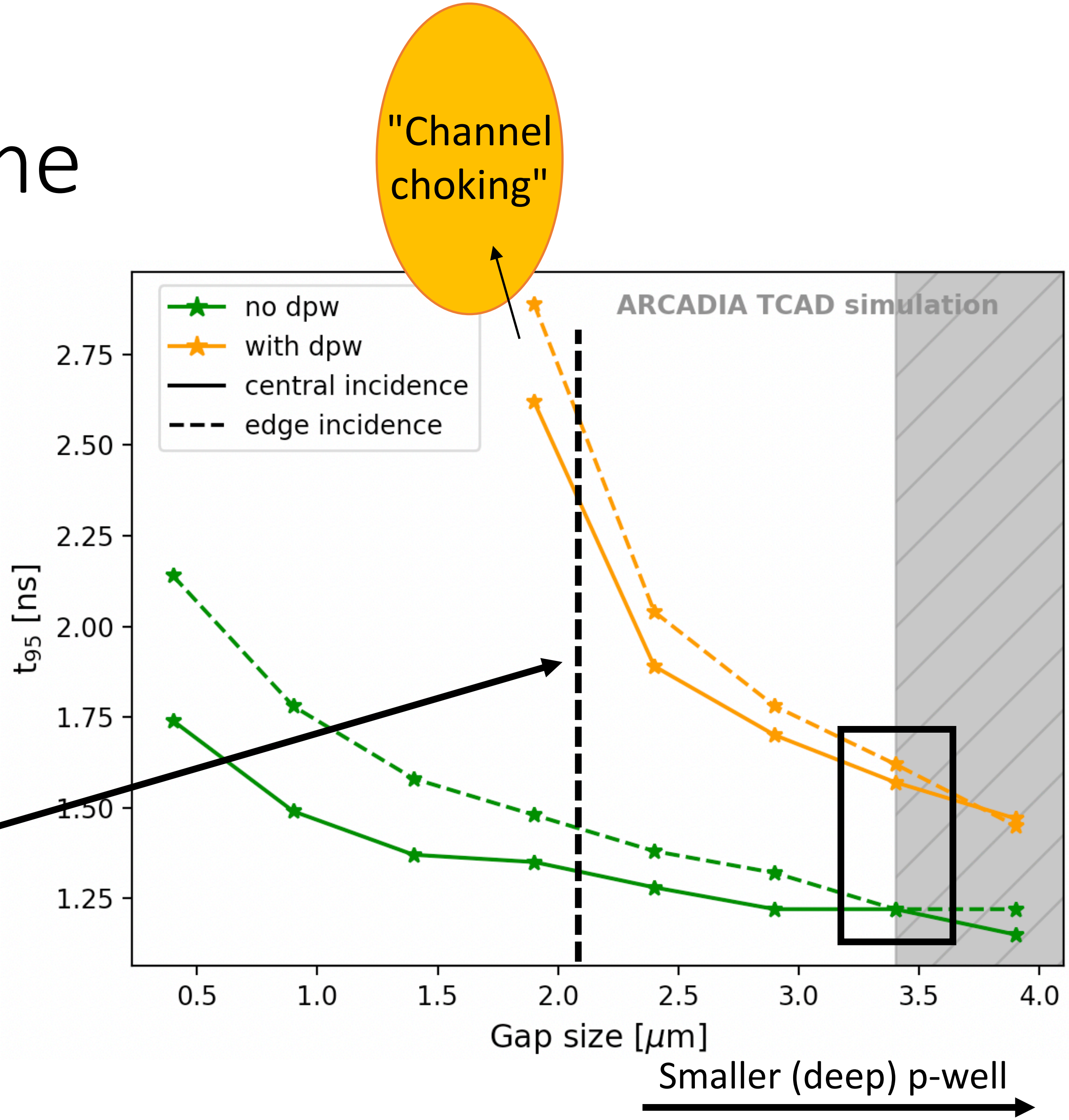
Faster and more uniform charge collection



- Optimised geometry → 95% charge collection in
  - ~ 1.6 ns (with deep p-well)
  - ~ 1.2 ns (without deep p-well)

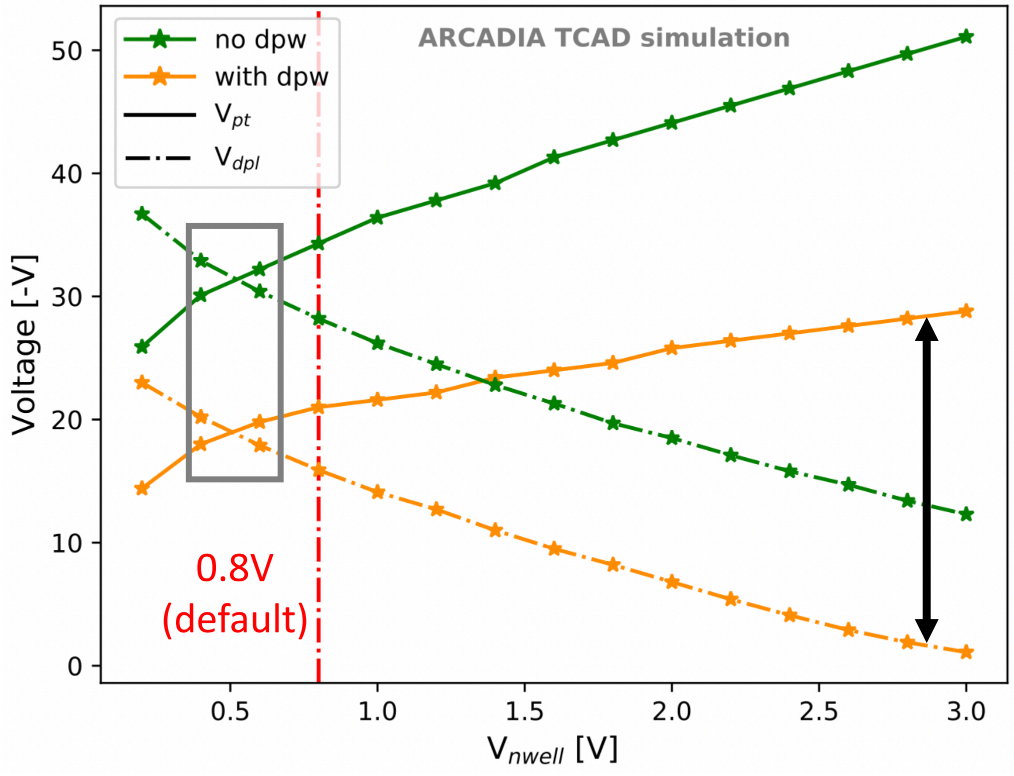
Charge collection time

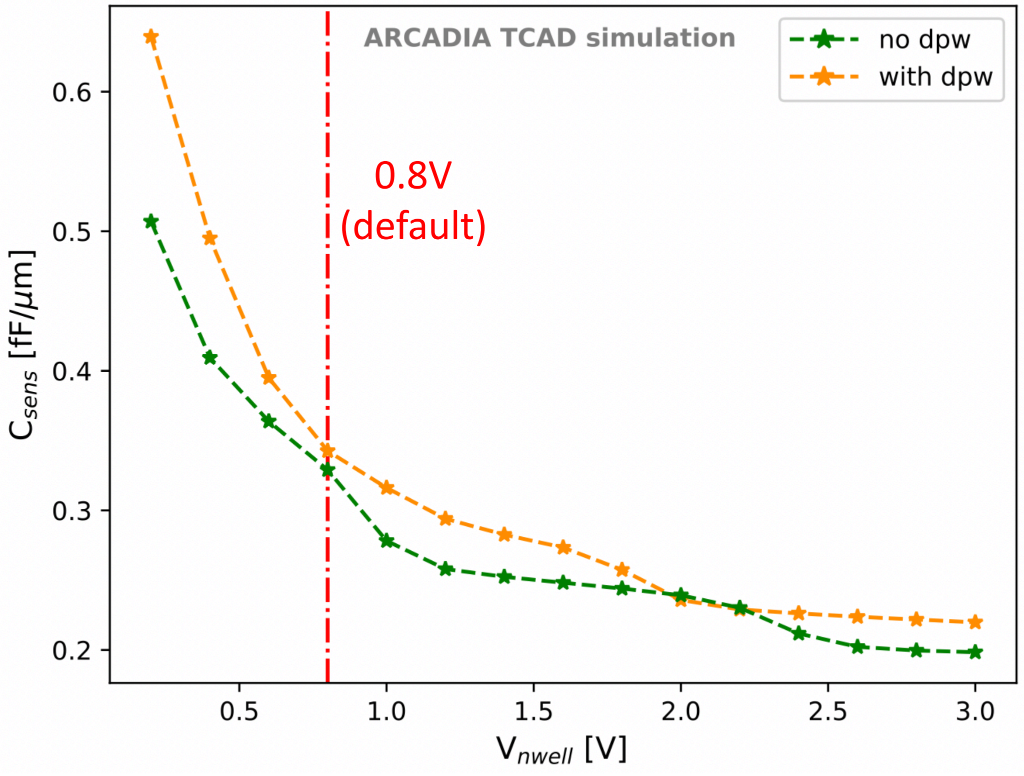




- Vertical line: max gap size for CMOS electronics integration between adjacent strips

Enhancements for fast timing

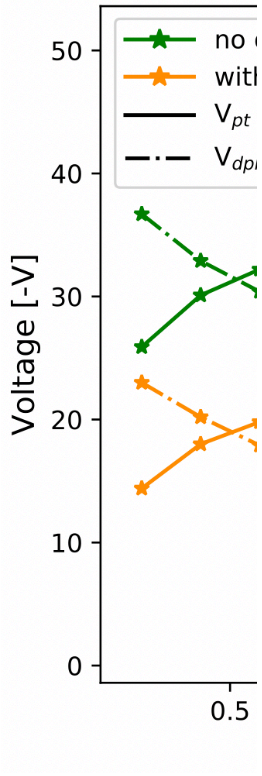


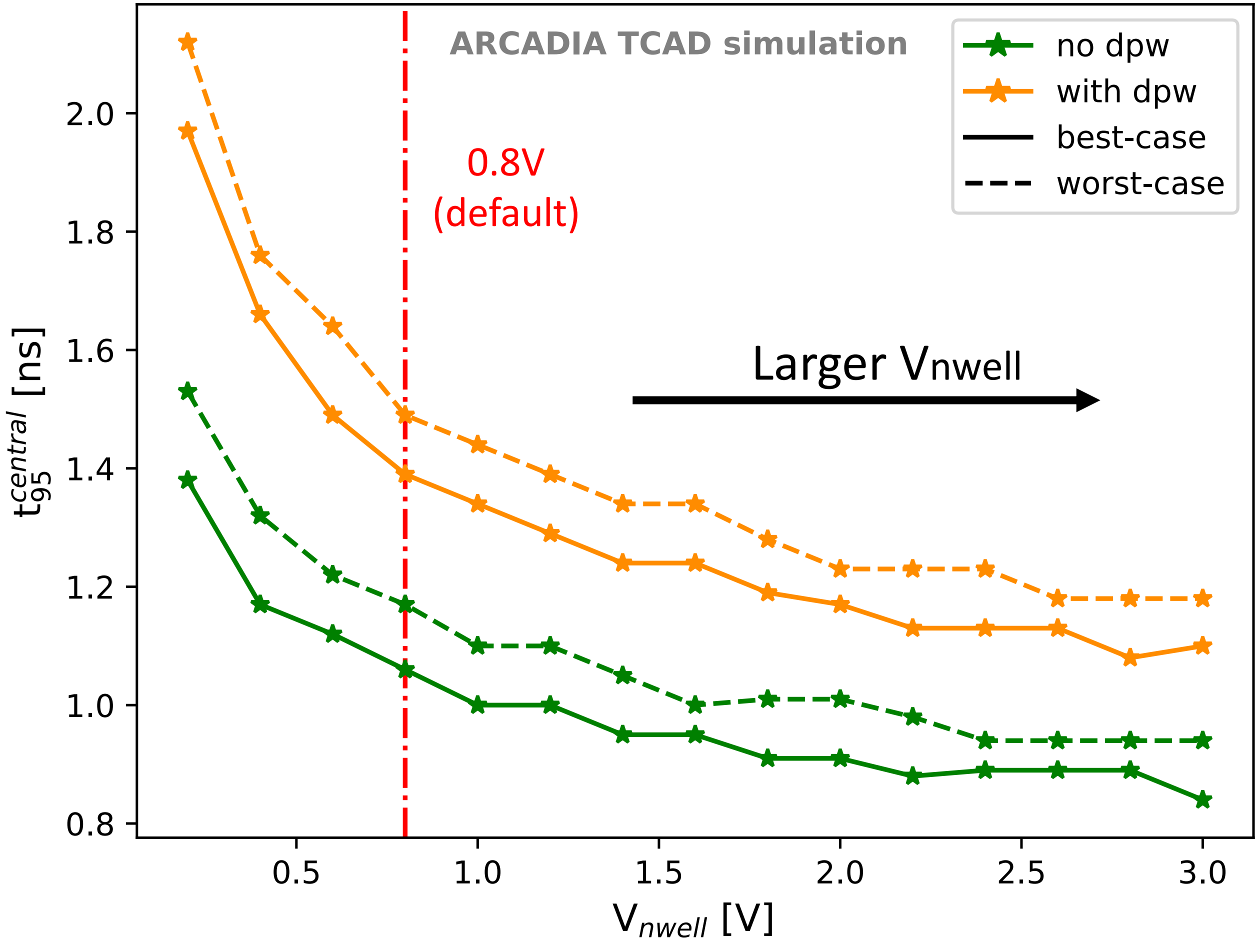


Larger Vnwell

Larger Vnwell

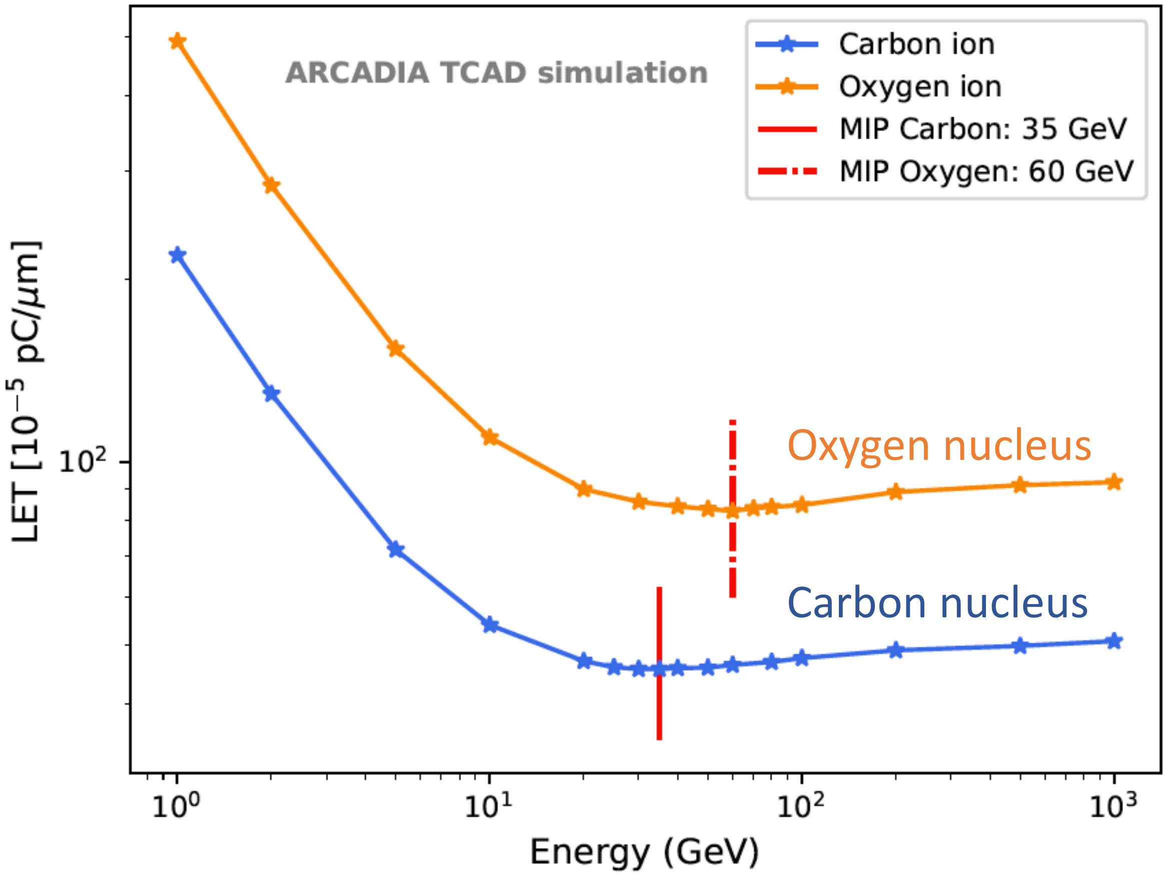
Enhancements for fast timing

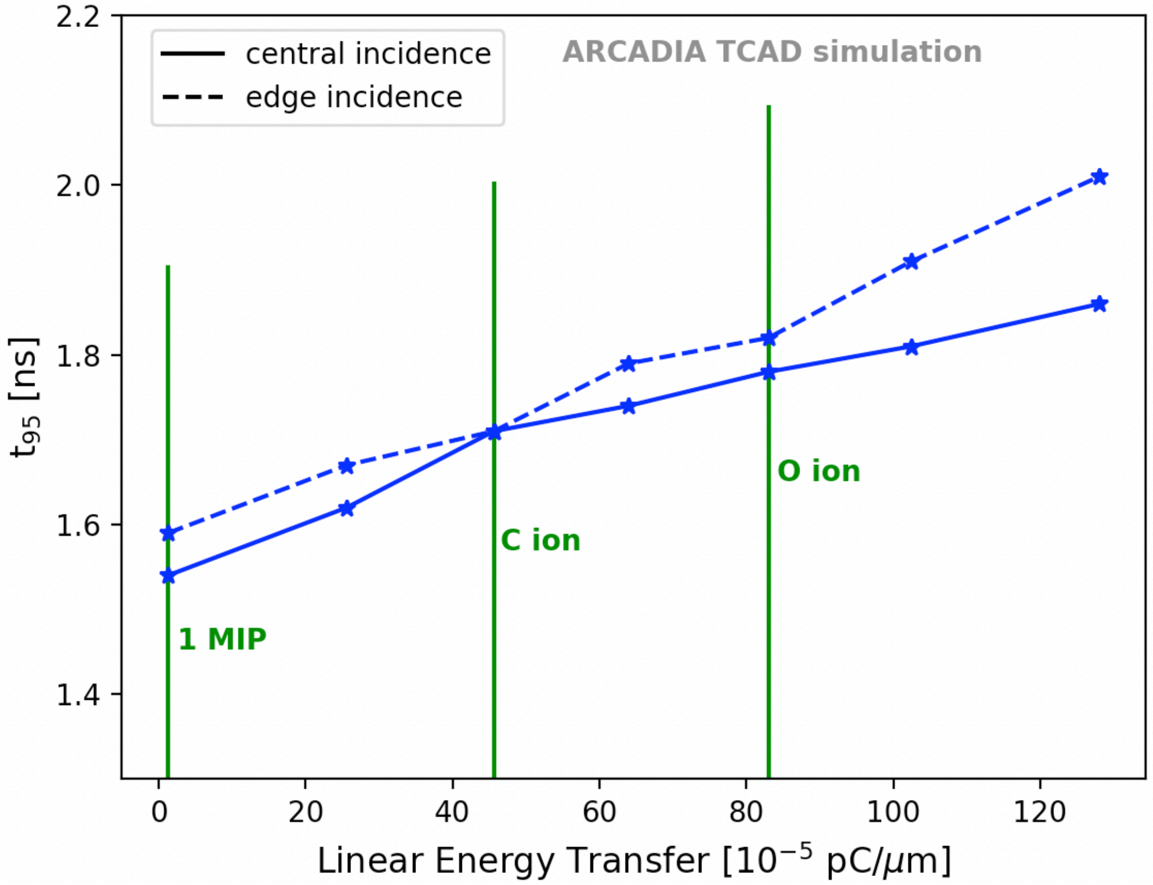




Heavy ion nuclei

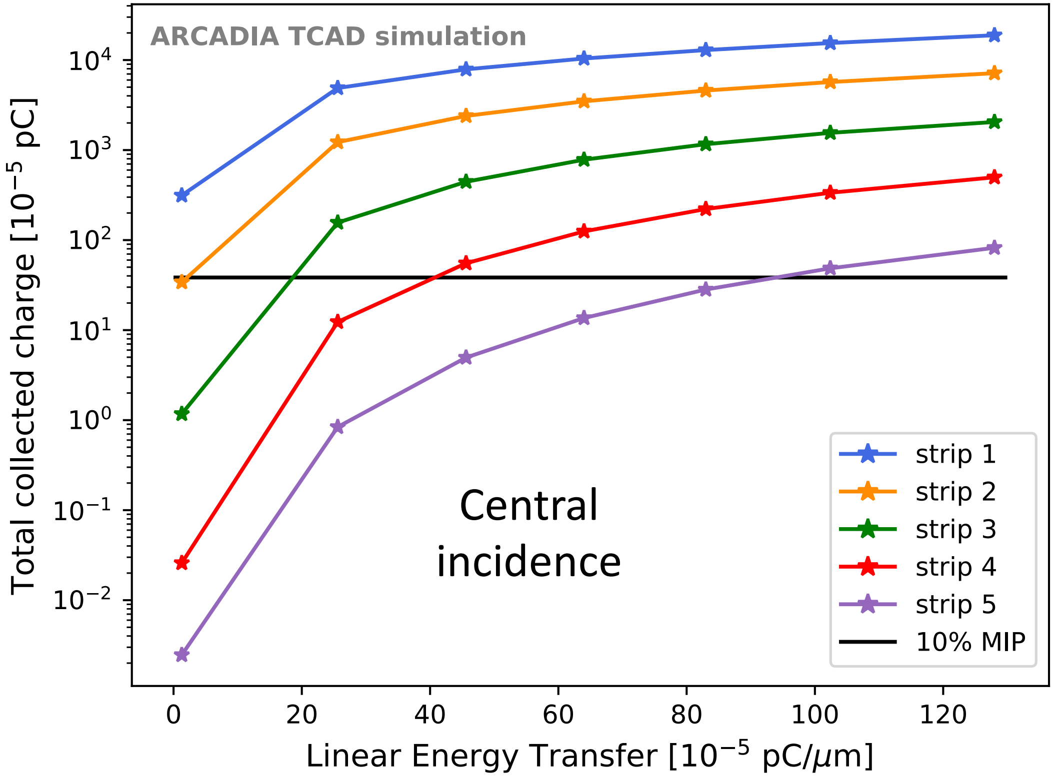
- 95% collection time raises by 300-400ps over a factor 100 increase in LET
- Never > 2 ns with 50μm thick sensors



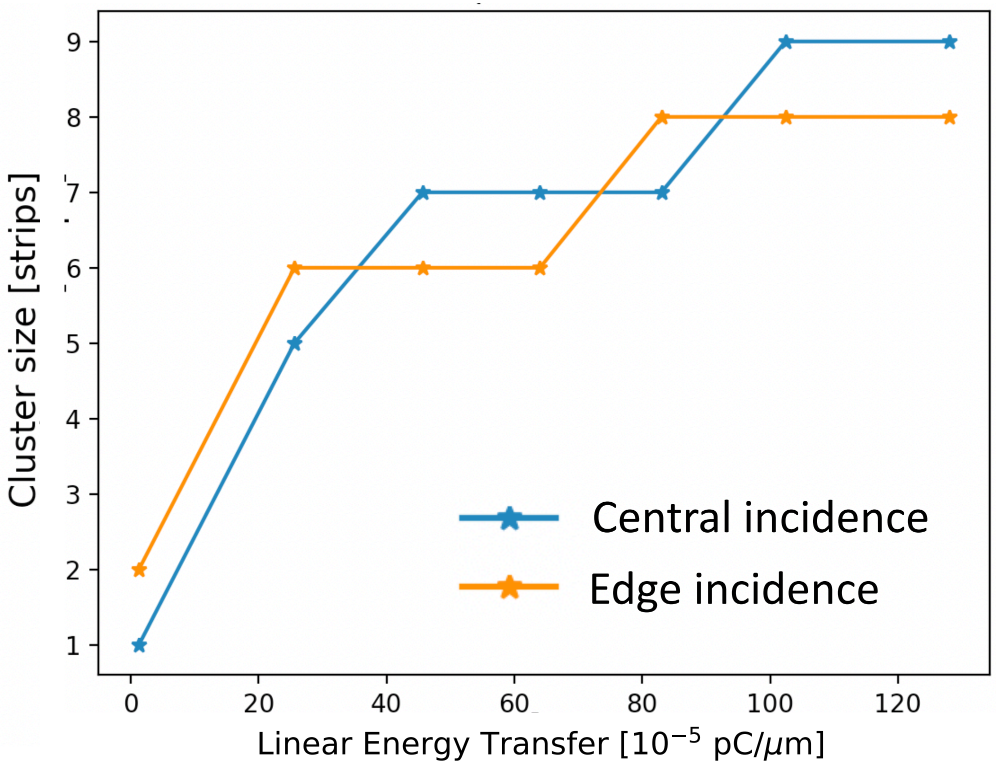


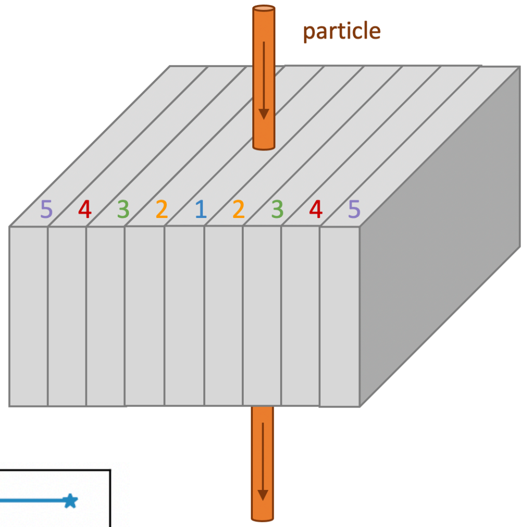
Geant4: https://github.com/mcentis/muonOnSilicon

Charge sharing

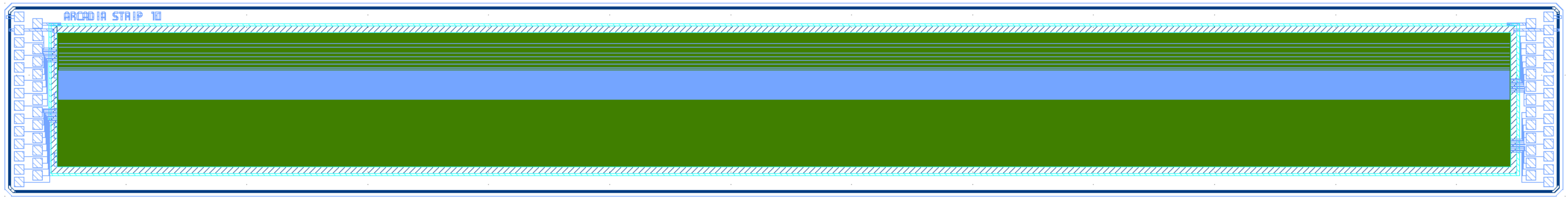


300μm thick sensors





Conclusions



- Selected 10 μm pitch fully depleted MAMS

Version 1	Optimised for fast timing	With deep p-wells
Version 2	Optimised for fast timing	Without deep p-wells
Version 3	Large deep p-well for potential inter-strip integrated CMOS electronics	

- Operation in full depletion
- Minimum capacitance
  - 0.33fF/μm (0.8V, DC coupling)
  - 0.2 fF/μm (3V, AC coupling)
- First samples available from May 2021

Details on ARCADIA simulations:

- arXiv:2101.09088
- arXiv:2011:09723