A readout architecture for the HEPD-02 tracker

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17/02/2021

CSES-02 and HEPD

HEPD-02 is a small particle detector that will be part of the China Seismo-Electromagnetic Satellite (CSES), a platform designed to perform precise correlated measurement of EM fields and particle fluxes.
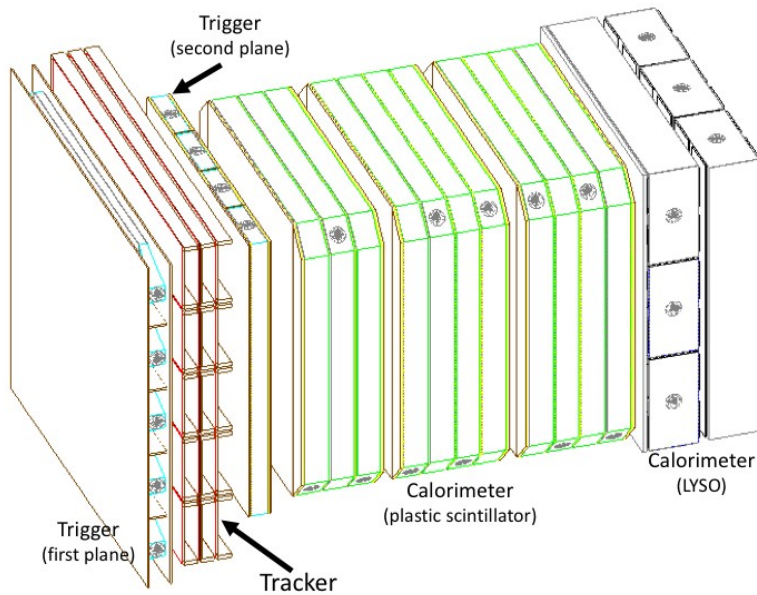
Instruments:
- EM fields detectors (EFD, HPM, SCM)
- Plasma physics (LP, GNSS-RO)
- Particle detectors (HEPD, PAP)

Fields of interest:
- Lithosphere-ionosphere coupling
- Solar Physics (space weather)
- Cosmic ray fluxes
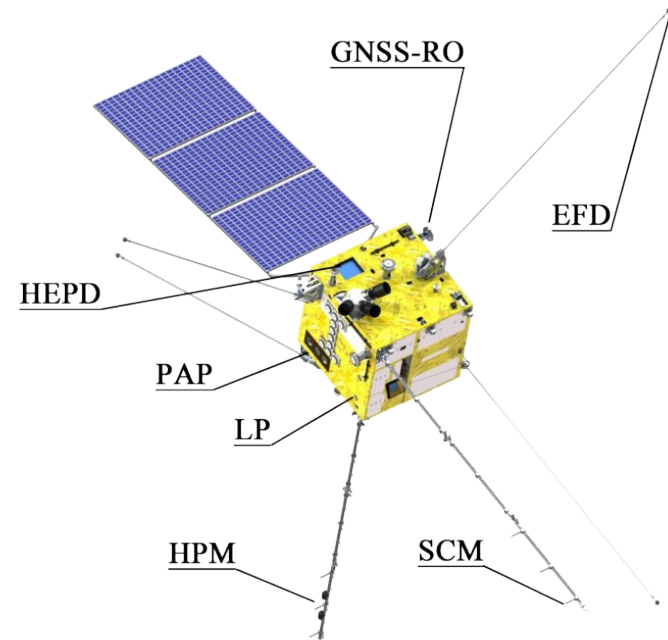
High Energy Particle Detector (HEPD-02) to measure fluxes of trapped particles in the magnetosphere in the 3-150 MeV range for electrons and 30-300 MeV for protons.


- 3-planes detector tracker composed by 150 ALPIDE pixel sensor.

- Two layers of crossed trigger bars.

- 11-tiles plastic scintillator.

- Two layers of LYSO scintillators.

- Surrounded by veto detectors (not shown in fig).

HEPD-02 measures particle energy and direction.

ALPIDE sensor

The ALPIDE sensor is CMOS Monolithic Active Pixel Matrix sensor developed by the ALICE collaboration for the LHC run 2 upgrade.
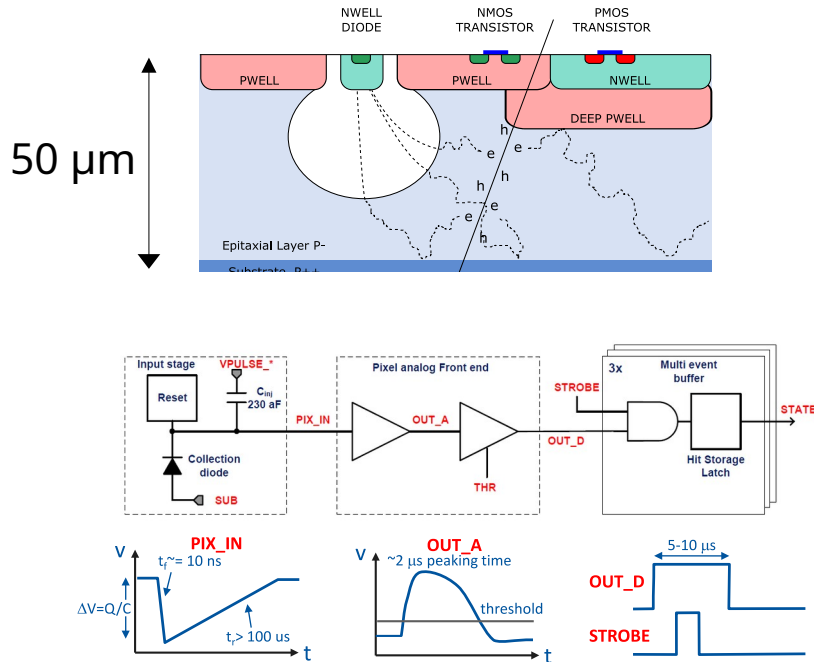
- 15×30 mm^2 sensor composed by a 1024×512 pixels matrix (~28 μm pixel pitch).

- On-pixel readout circuit implanted on the same substrate of the active area.

- Each pixel generates a binary output (hit/no-hit) after a trigger command.

ALPIDE sensor

The ALPIDE sensor is CMOS Monolithic Active Pixel Matrix sensor developed by the ALICE collaboration for the LHC LS2 upgrade.
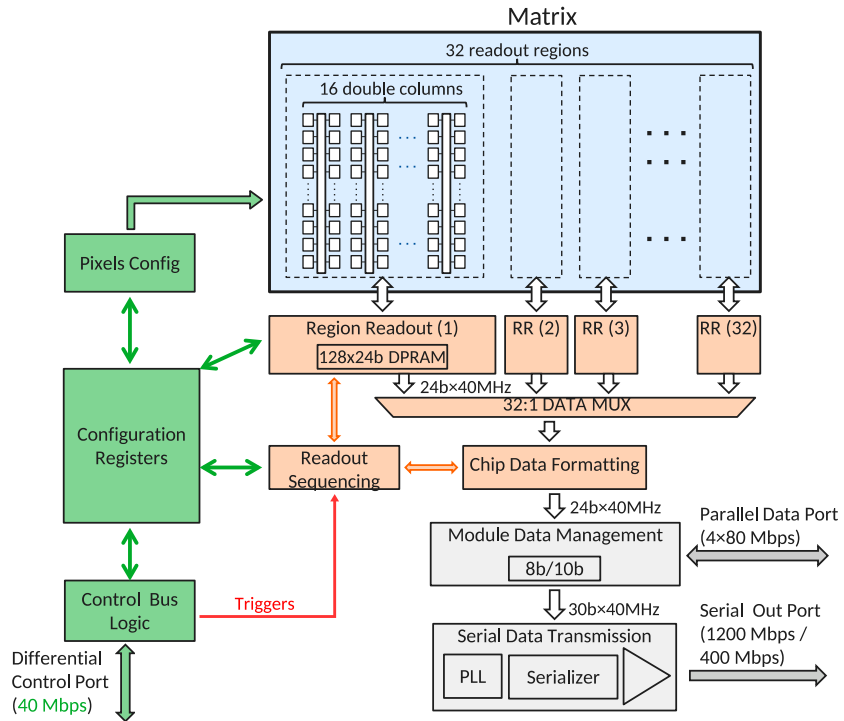
- Readout performed on groups of two columns, with zero suppression and efficient cluster coding.

- Fast readout port (up to ~1.2 Gbps) + Parallel port for local bus (daisy chain configuration 1 master + max 6 slaves).

- Control port offering a slow readout side-channel (~3-5 Mbps raw datarate).
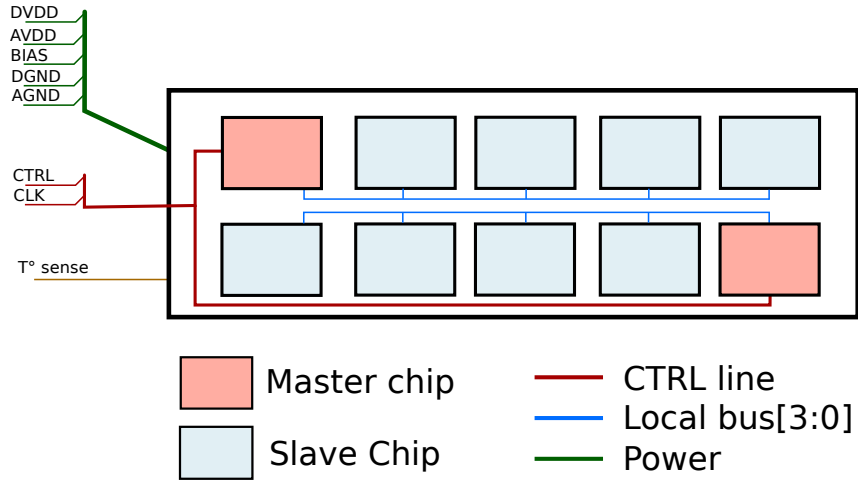
Use of ALPIDE in space

The nominal power consumption of the chip overshoot the HEPD-02 power budget for the tracker.
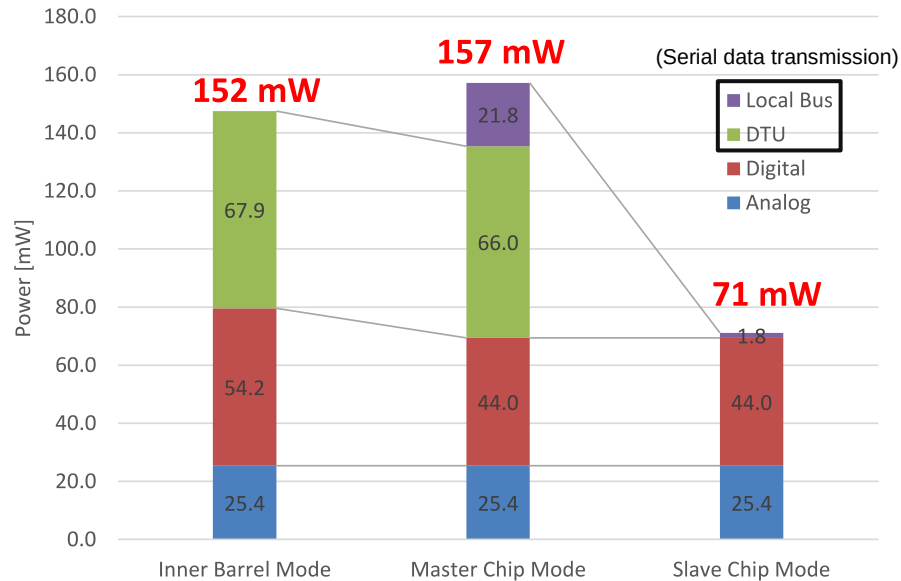
- Higher resolution
- Sparse readout scheme
- Lower noise
- Cost
- Power consumption

Stave structure

The basic unit of the tracking detector is a stave with 10 chips (2 master with 5 slaves each)

DVDD
AVDD
BIAS
DGND
AGND

CTRL
CLK

T° sense

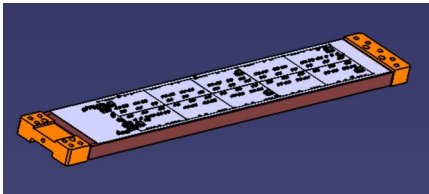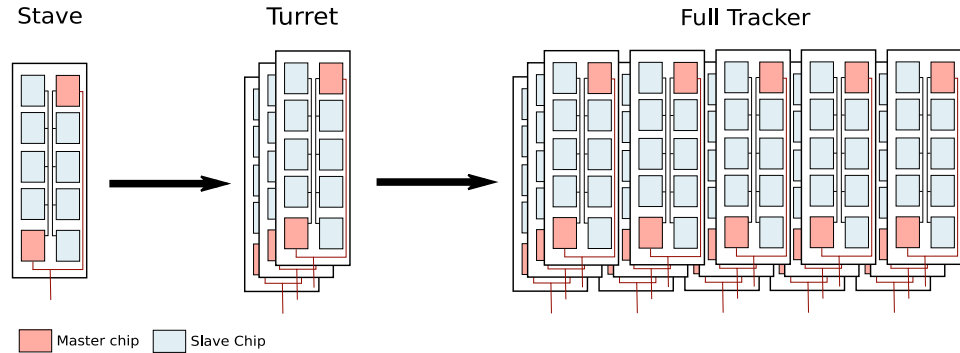| Master chip | CTRL line |
| Slave Chip | Local bus[3:0] |
| | Power |

- The high speed serial line on the two master is not connected.

- The two masters share the same CTRL line, used for the readout of the entire stave.

A single CTRL line shared for the entire stave is acceptable considering the expected event rate: max ~100-200 bytes @ 100Hz typical 1 KHz peak.
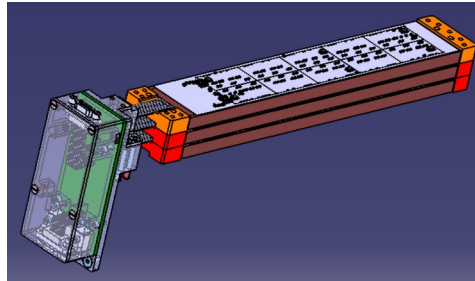
Tracker

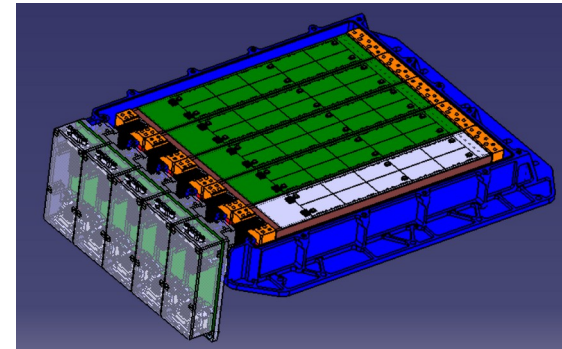The tracker is divided in 5 turrets aligned with the trigger bars.

Each turret is composed by 3 staves formed by a Flexible Printed Circuit (FPC) with 10 chips, mounted on a carbon fiber support.

Stave Turret Full Tracker
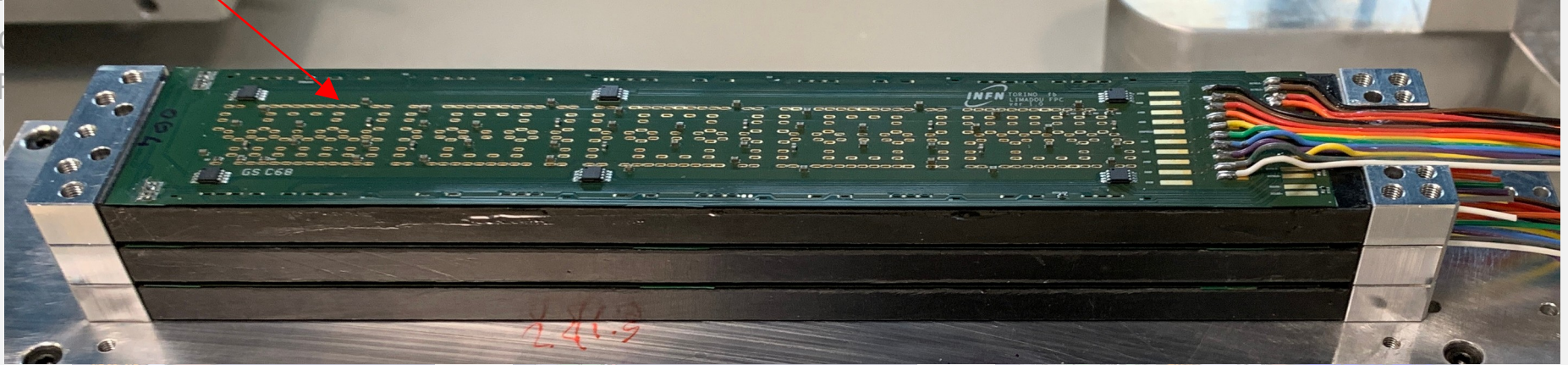
Master chip Slave Chip

Stave

Turret

Tracker

Turret Prototype

The tracker is divided in 5 turrets and ... trigger bars.

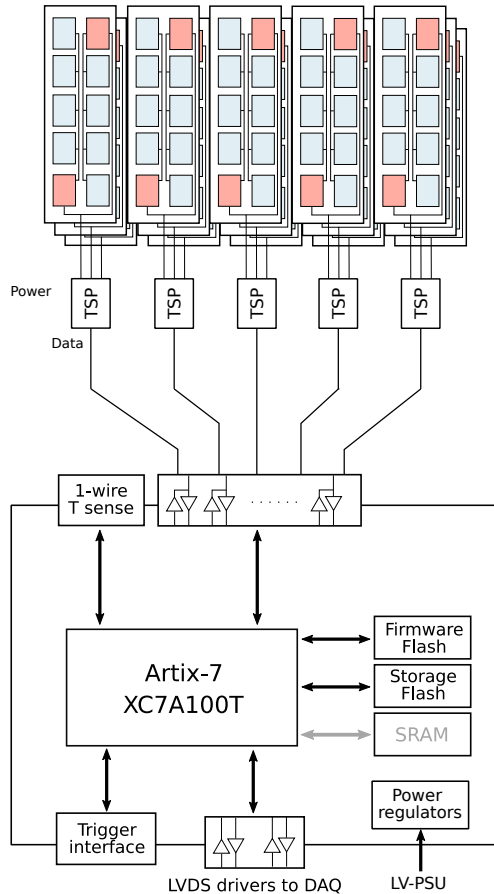Each turret is composed by 3 staves fo...
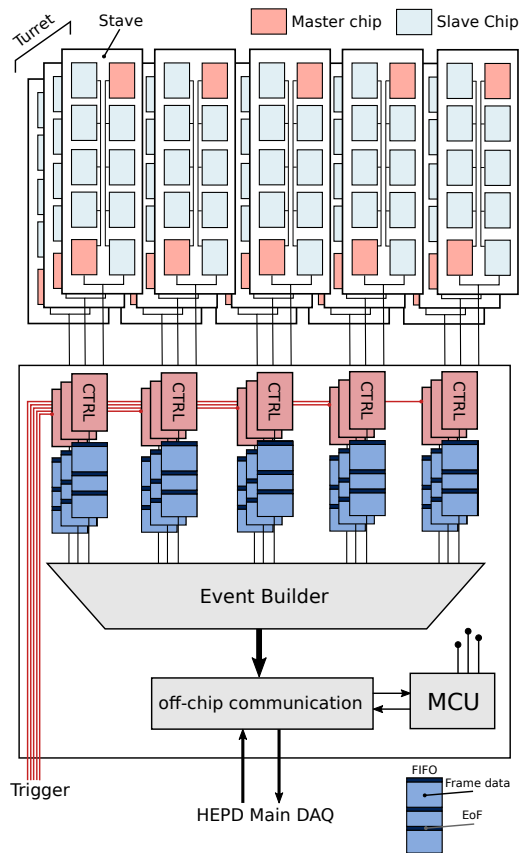
(P...

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Stave

Turret

Tracker

Tracker DAQ Board

The entire tracker is managed and read out by a Tracker DAQ board (schematic and firmware developed in-house).

- Single low-power FPGA.

- 3x differential LVDS Control lines for each tower + 1 clock line for each turret.

- Spacewire connection with HEPD main DAQ (~100 Mhz).

- 5 trigger lines + busy output.

Firmware Implementation

The readout of the tracker is performed in parallel on each stave and employs clock gating to save power.

- 15 readout cores ("CTRL") propagate the trigger to the staves (triggered tower + 2 adjacent) and implement a readout finite state machine.

- Event data is deposited in stave-dedicated FIFOs and is assembled and packaged by an "event builder".

- Each stave is clocked only for the time necessary for the event readout.

Strategy: clock gating

To save power enable the clock to the staves of triggered turrets only for the time necessary for the readout of the event.
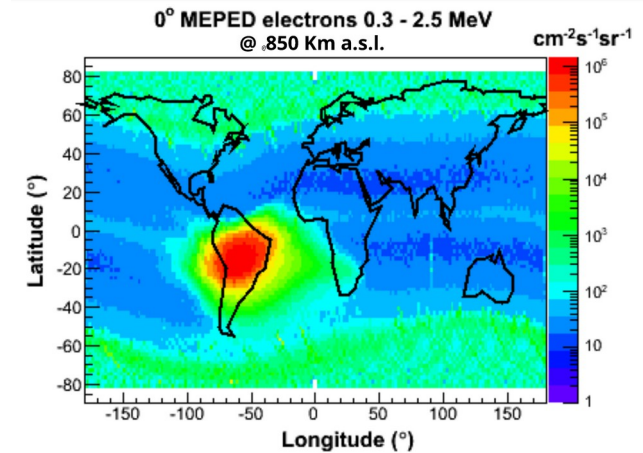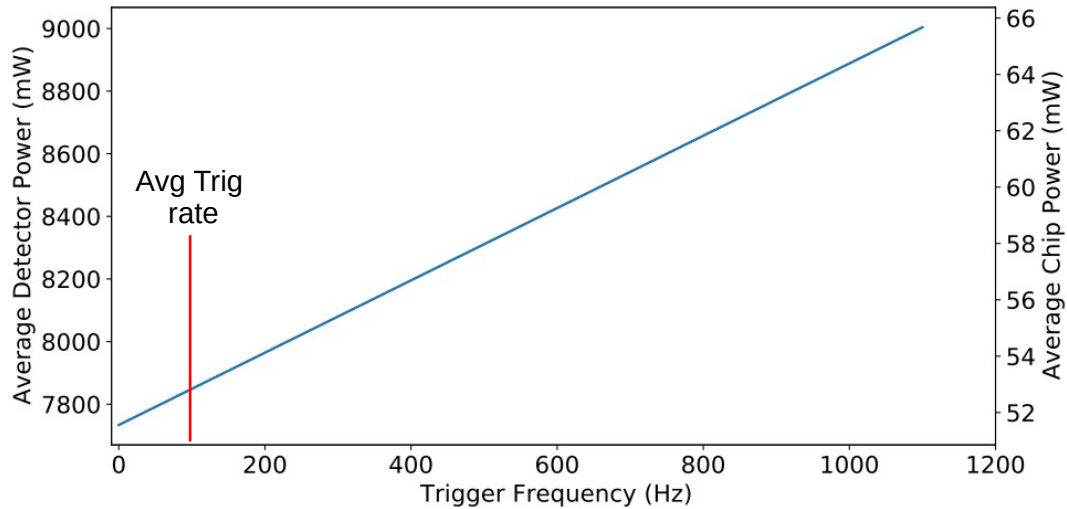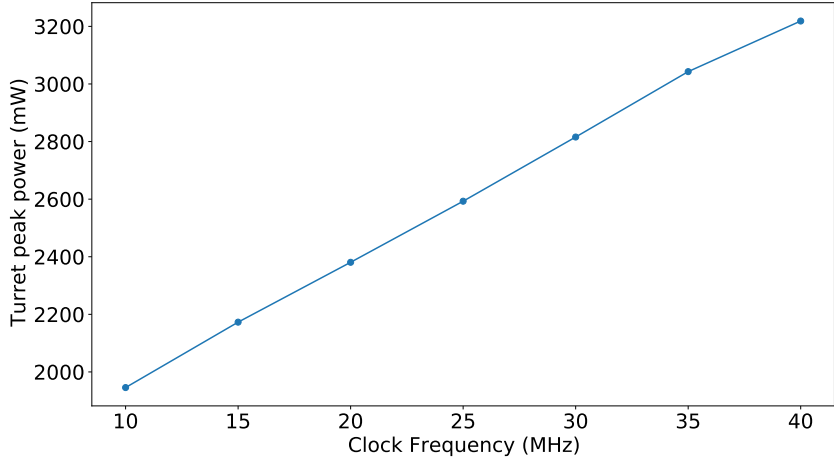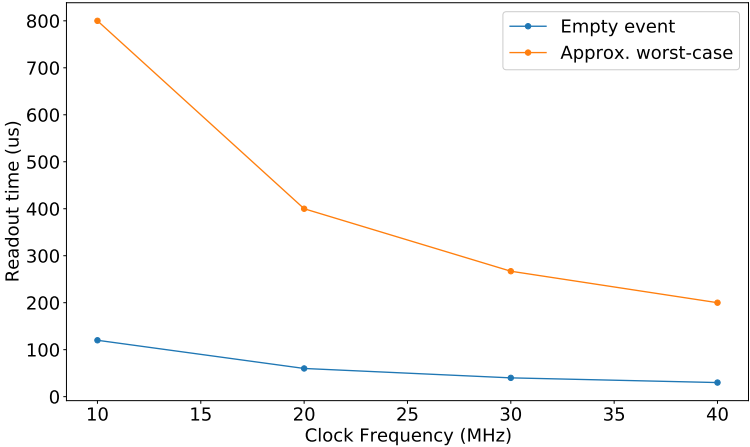

With a typical trigger rate of ~100 Hz (and maximum of 1 KHz) the detector is functionally "off" for most of the time.

Strategy: dynamic frequency scaling

Since the event rate is dependent on coordinates it should be possible to dynamically scale the clock freq:
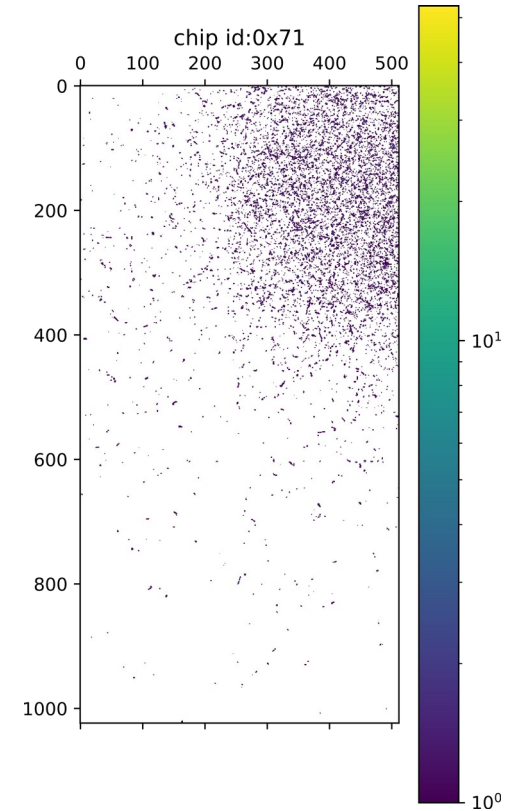
- Lower trigger rate → less data to read and more tolerant to dead time → clock speed can be reduced.

Conclusion

- Implemented a readout solution to fit the mission's power budget (readout scheme, clock gating and frequency scaling)

  - validation of the readout scheme

  - ~50% average power consumption reduction

- Several staves prototypes produced and "mass" production of turrets starting soon.

Acquisition with ^{90}Sr test source

Thank You