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Readout architecture for the HEPD-02 tracker

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The adoption of monolithic active pixel particle detectors in space missions is obstructed by a number of technical challenges involving power dissipation, mechanics and material budget.

This work presents a sparse readout architecture for the 3-layers particle tracker, based of the ALPIDE MAPS chip, under development for the HEPD-02 instrument.

With a total of 150 APIDE chips and the stringent constrains imposed by a space mission, the deployment and readout of such detector requires careful optimizations to limit the power consumption but at the same time maintain useful performances.

Such task is approached with a custom parallel readout architecture, implemented on a single low-power FPGA chip managing the entire tracker.

The envisaged solution can be scaled up to detectors of size and complexity larger than HEPD-02, constituting a viable option for future mid-sized space missions.

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