Contribution ID: **184** Type: **Oral**

Readout architecture for the HEPD-02 tracker

Wednesday 17 February 2021 15:00 (20 minutes)

The adoption of monolithic active pixel particle detectors in space missions is obstructed by a number of technical challenges involving power dissipation, mechanics and material budget.
This work presents a sparse readout architecture for the 3-layers particle tracker, based of the ALPIDE MAPS chip, under development for the HEPD-02 instrument.
With a total of 150 APIDE chips and the stringent constrains imposed by a space mission, the deployment and readout of such detector requires careful optimizations to limit the power consumption but at the same time maintain useful performances.
Such task is approached with a custom parallel readout architecture, implemented on a single low-power FPGA chip managing the entire tracker.
The envisaged solution can be scaled up to detectors of size and complexity larger than HEPD-02, constituting a viable option for future mid-sized space missions.

Primary author: GEBBIA, Giuseppe (Università di Trento)

Co-authors: ZUCCON, Paolo (Universita degli Studi di Trento and INFN (IT)); IUPPA, Roberto (Universita degli Studi di Trento è INFN (IT)); RICCI, Ester (Universita degli Studi di Trento and INFN (IT))

Presenter: GEBBIA, Giuseppe (Università di Trento)

Session Classification: Session 7: Electronics

Track Classification: Electronics