PASSIVE CMOS SENSORS FOR RADIATION-TOLERANT HYBRID PIXEL-DETECTORS

16. TRENTO WORKSHOP

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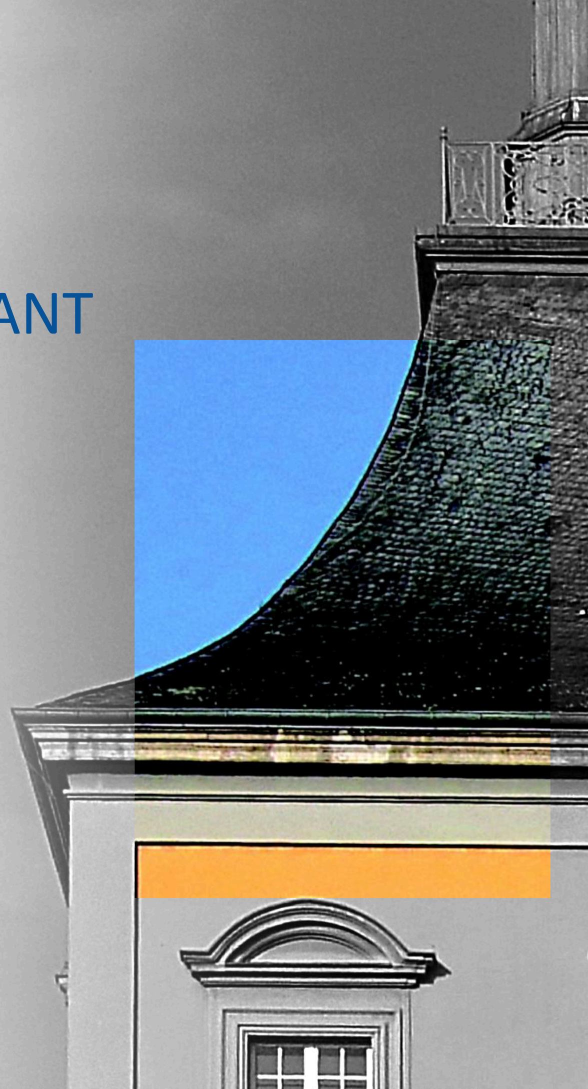
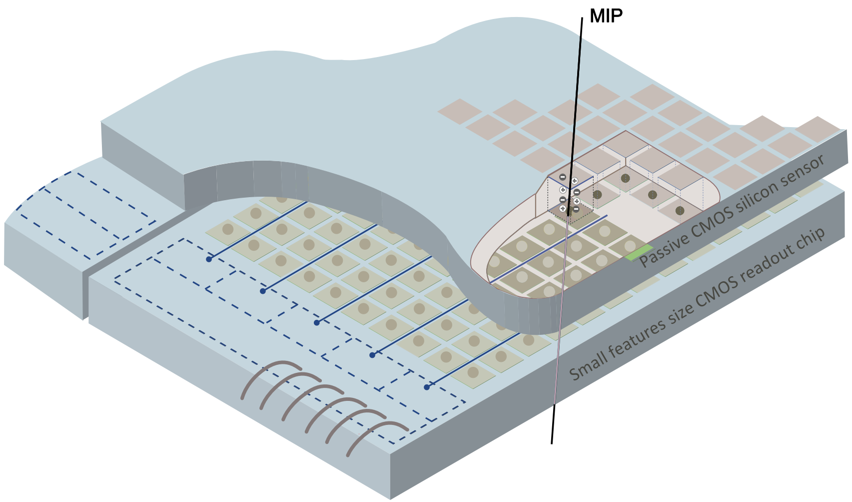


PASSIVE CMOS SENSORS

Use commercial high-voltage/high-resistive CMOS process for planar sensor production, no active components:

- Large wafers (200 mm)
- High production throughput, low costs
- Poly-silicon resistors → connection to a bias grid
- MIM capacitors for AC-coupling → no leakage current into readout
- Many metal layers for redistribution
- Sub-pixel coding feasible?
  https://doi.org/10.1016/j.nima.2020.164524
- Field plates for inter-pixel isolation?

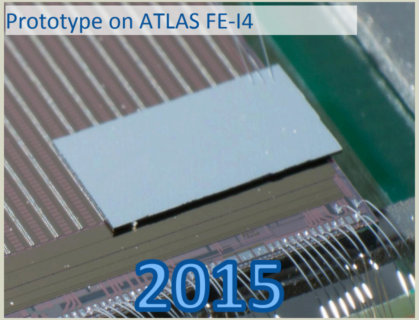


LFoundry 150 nm 1.8V CMOS process http://www.nanoitaly.it/nanoitaly/images/presentazioni/PS_2_1-Fama.pdf
MIM capacitor: 1 fF/μm², 2 fF/μm²
Polysilicon resistor: ~ 2.2 kΩ/□
4 – 6 metal option, thick metal
Back-side processing: thinning and implantation
Lithographic stitching

HISTORY OF PASSIVE CMOS SENSORS USING LFOUNDRY PROCESS

Large pixel prototype

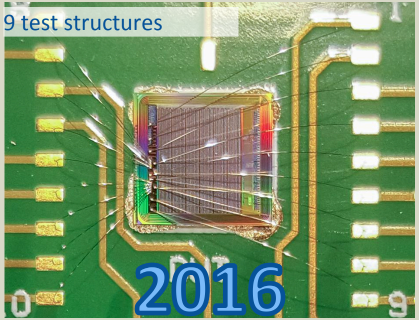
- 50 x 250 um² pixels, ATLAS IBL planar geometry
- Performance comparable to ATLAS IBL sensors after irradiation $> 1 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$
- Investigation of AC-coupling schema, pixel biasing schemes (bias dot vs. resistor biasing)



Prototype on ATLAS FE-I4

Test structures

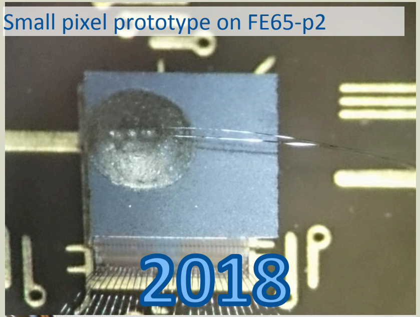
- Many structures produced
- Varying designs: guard rings, pixel isolation, implantation geometries
- Investigations of break down with TID
  → Identified enhanced guard ring structure
- Investigation of sensor capacitances



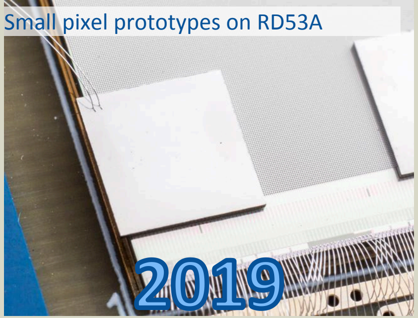
9 test structures

Small pixel prototype

- 50 x 50 um² pixels, ATLAS ITk pixel geometry



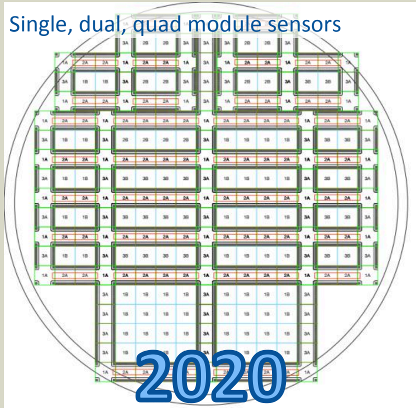
Small pixel prototype on FE65-p2



Small pixel prototypes on RD53A

Full size (quad) sensors

- 50 x 50 um² pixels, 25 x 100 um² pixels
- Full-size ATLAS ITk pixel modules
- Participation in ATLAS ITk pixel sensor market survey
- RD53A and RD53B compatible



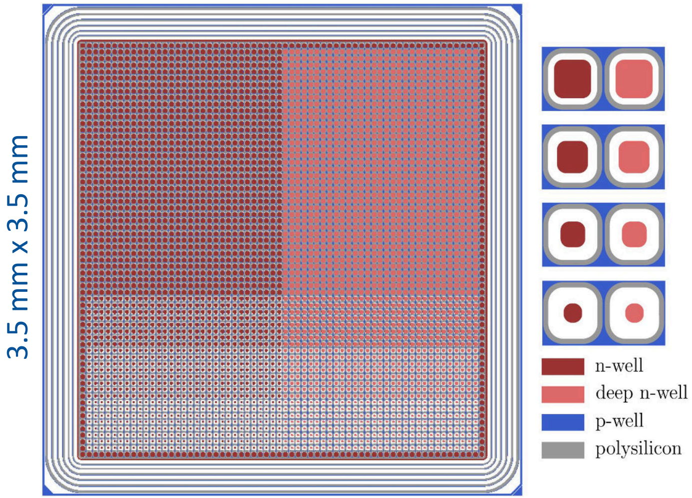
Single, dual, quad module sensors

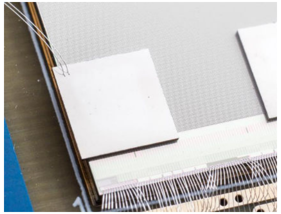
Byproducts of DMAPS efforts

Dedicated submission

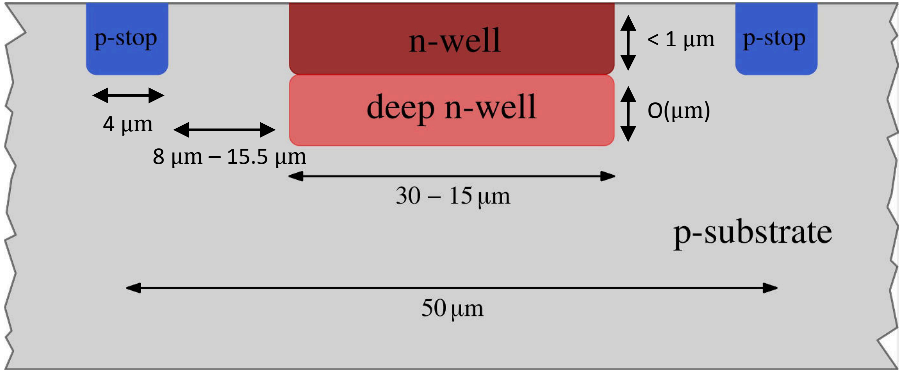
SMALL PIXEL PROTOTYPE

- High resistive 4-5 $\mathrm{k\Omega\ cm}$ p-type CZ wafer
- 50 µm x 50 µm pixels in 64 × 64 matrix
- 100 um thickness, backside implant, etching + metallization @ IBS France
- Bump bonded to RD53A @ IZM Berlin
- DC coupled pixels:
  - No biasing structure
  - Variation of implantation width: 15 µm - 30 µm
  - Variation of n-well depth: n-well (NW) and deep n-well (DNW)
- More info in publication: https://doi.org/10.1016/j.nima.2020.164130
- Irradiated at the Bonn HISKP Irradiation Facility





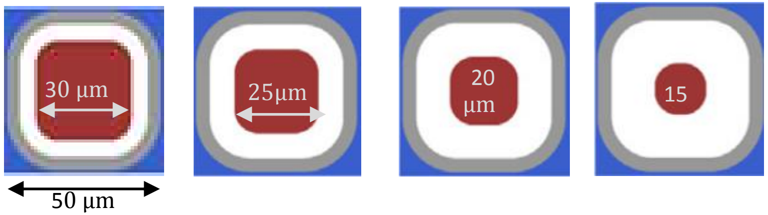
DC pixel

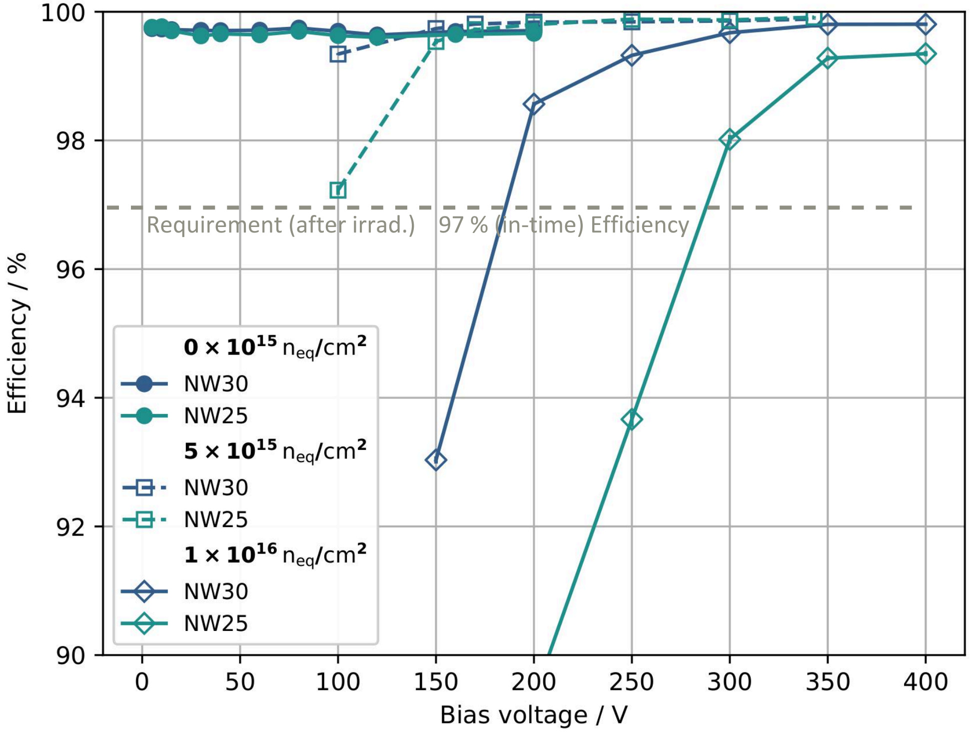


EFFICIENCY MEASUREMENT

- DUT operation conditions:
  - Threshold: ~ 1000 e
  - Noise occupancy: < 10^{-6}
  - Bias voltage < 400 V, otherwise too many noisy pixels
- Before irradiation:
  > 99.5 % at 5 V only
- $5 \times 10^{15}\ n_{eq}/cm^2$:
  > 99 % efficiency (@ 100 V)
- $1 \times 10^{16}\ n_{eq}/cm^2$:
  > 99 % efficiency (@ 400 V)
- Mean efficiency for fifferent fill-factors @ 400 V:

99.8 % | 99.3 % | 99.1 % | 96.8 %



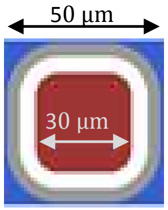


IN-PIXEL EFFICIENCY @ 1 x 10^{16} n_{eq}/cm^2

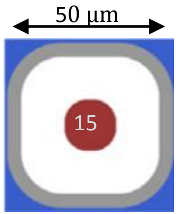
- High bias voltage + large n-implants
  Homogeneous efficiency within pixels
- Flavors with small n-implants:
  Efficiency loss at pixel corners (especially for low bias voltage)

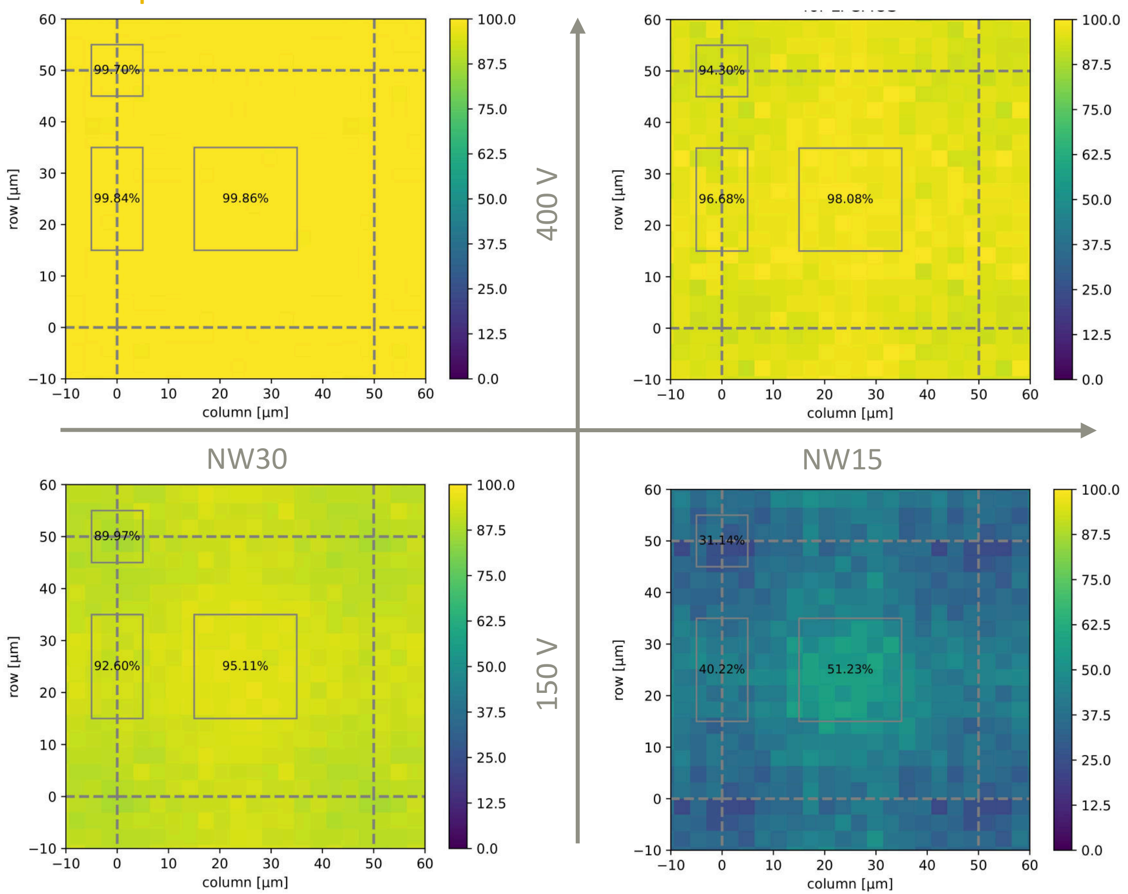
  → Due to low electric field and charge sharing

NW30 (std. design)



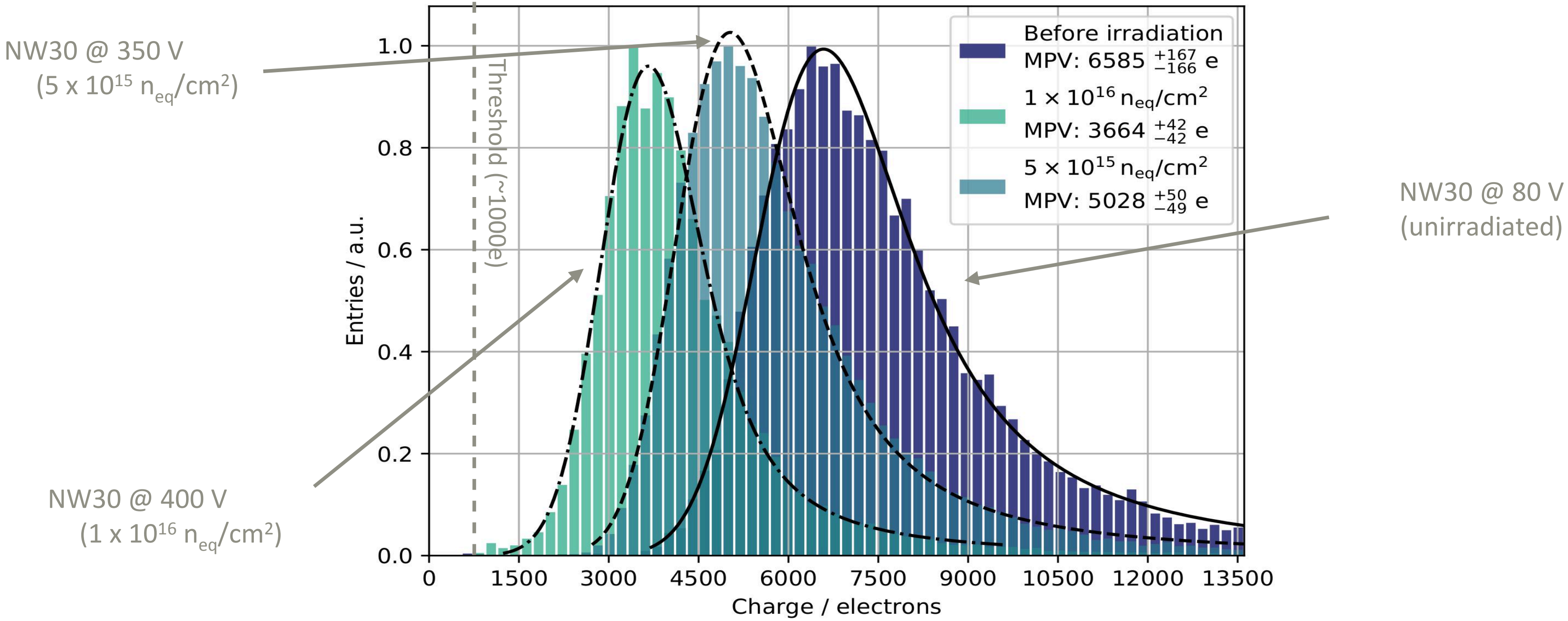
NW15



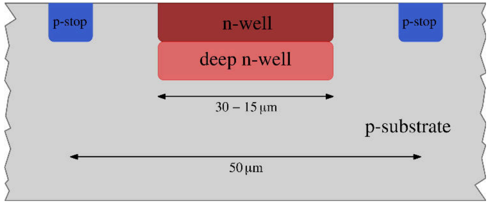


CHARGE: UNIRRADIATED VS IRRADIATED

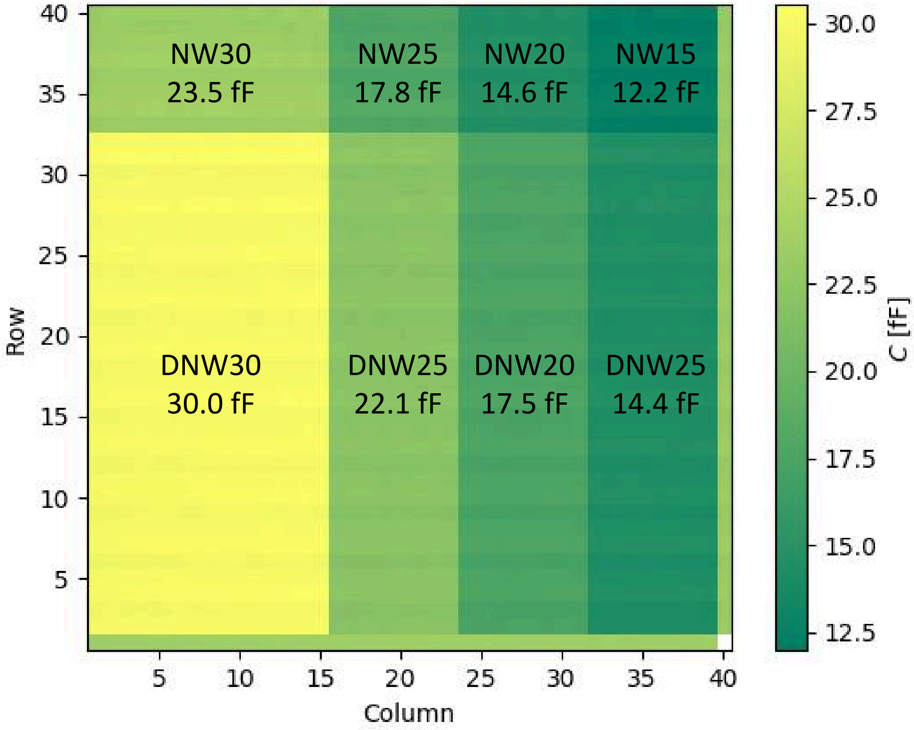
- Single-hit cluster-charge measurements with 5 GeV electrons
- Measured after charge calibration
- Using hit-bus TDC method

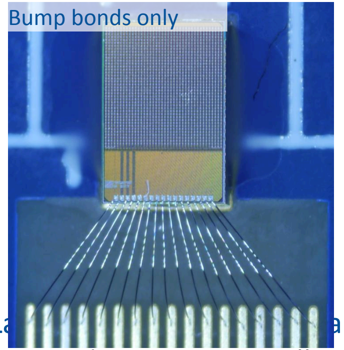


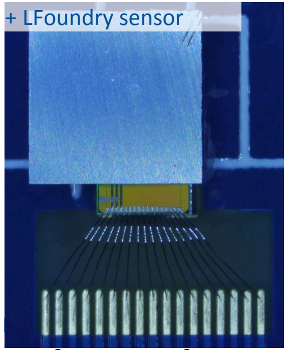
SENSOR INPUT CAPACITANCE



- Capacitance measurement chip in TSMC 65 nm PixCap65:
  - ~ 0.3 fF precision
  - Ability to measure different contributions to input capacitance (inter-pixel, bump bonds, backplane)
- Publication: https://doi.org/10.1088/1748-0221/16/01/P01029



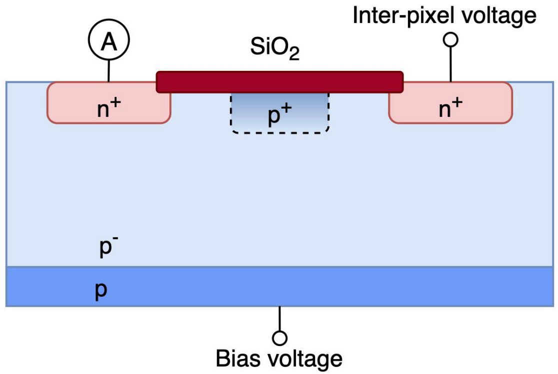


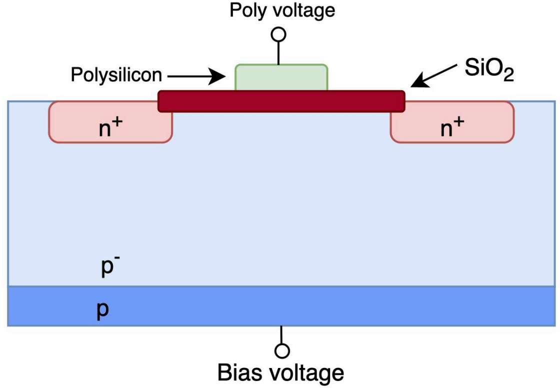


- La … a
  p-stop distance to n-well: 23.5 fF -> 12.2 fF
  -> use no p-stop, but field plates?

INVESTIGATION OF THE INTER-PIXEL RESISTANCE

- P-stop isolation maintains a high inter-pixel resistance after irradiation
  - Advantage: low signal spreading, good spatial resolution
  - But: a dominating source of the detector capacitance
- Idea:
  - Substitute the p-stop by a field plate at inter-pixel regions
  - Electrostatic potential on field plate modifies the conductivity
    - Increase inter-pixel resistance
    - Remove the contribution of p-stop to the pixel capacitance
- Resistance measurement: apply voltage between neighboring pixel n-wells and measure current (voltage << bias voltage)





INVESTIGATION OF THE INTER-PIXEL RESISTANCE

- Test structure in LFoundry 150 nm CMOS, 50 x 50 μm^2 pixel matrix, irradiated with 12 MeV protons @ Bonn HISKP irradiation facility
- Before irradiation: High resistance for all isolation structures ($\sim 10^{13} - 10^{14} \Omega$)
- After irradiation: P-stop: $\sim 10^{11} \Omega$, Field-plate: $\sim 10^{8} - \sim 10^{11} \Omega$ depending on bias

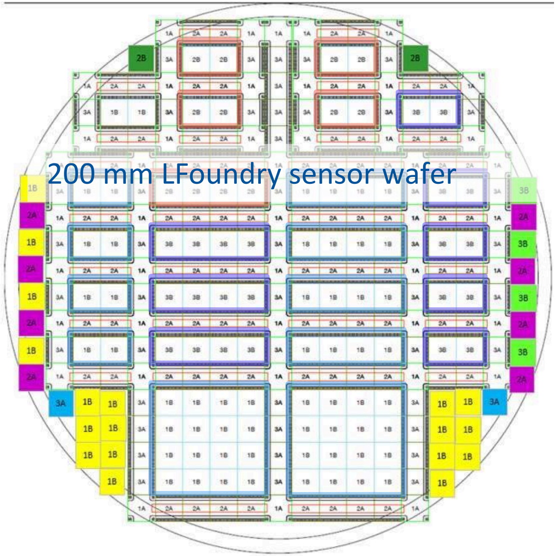
Measurements at 100 V bias

Fluence $[n_{eq}\ cm^{-2}]$	Resistance Field-plate: floating	Resistance Field-plate: 0 V	Resistance Field-plate: -100 V	Resistance with p-stop	T
0	$\sim 5 \times 10^{13} \Omega$	$\sim 2 \times 10^{14} \Omega$	$\sim 2 \times 10^{14} \Omega$	$\sim 1.5 \times 10^{14} \Omega$	293 K
5×10^{14}	$4960 \times 10^{6} \Omega$	$950 \times 10^{6} \Omega$	$130 \times 10^{9} \Omega$	$155 \times 10^{9} \Omega$	258 K
1×10^{15}	$2580 \times 10^{6} \Omega$	$520 \times 10^{6} \Omega$	$160 \times 10^{9} \Omega$	$110 \times 10^{9} \Omega$	258 K
5×10^{15}	$510 \times 10^{6} \Omega$	$130 \times 10^{6} \Omega$	$32 \times 10^{9} \Omega$	$27 \times 10^{9} \Omega$	258 K
1×10^{16}	$260 \times 10^{6} \Omega$	$130 \times 10^{6} \Omega$	$15 \times 10^{9} \Omega$	$16 \times 10^{9} \Omega$	258 K

- Requirement > $10\ M\Omega$ seems feasable?
- Next: measure capacitance for field-plates, X-Ray irradiations, and reproduce results with TCAD

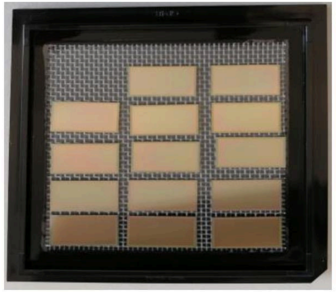
FULL-SIZE PASSIVE CMOS SENSOR SUBMISSION

- Design (mainly by Tianyang Wang)
  - Different sizes for modules:
    - RD53A single and dual chip modules
    - RD53B quad modules
  - Different pixel flavors:
    - 50 x 50 μm^2 and 25 x 100 μm^2
    - AC or DC coupled
  - Not only pixel sensors, also strip sensors:
    See previous talk
- Float-zone wafer material
- Thinning to 150 µm + handling wafer and backside implantation @ LFoundry
- Backside Al-Si metal + UBM + Flip-chip @ IZM Berlin

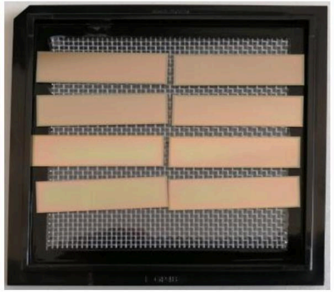


200 mm LFoundry sensor wafer

Single sensor



Double sensor



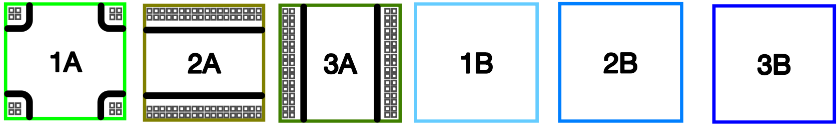
Quad sensor

STITCHING AND BIASING

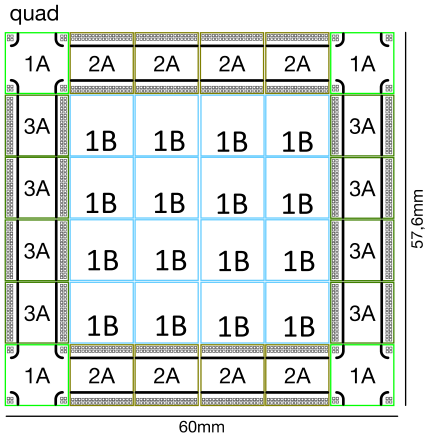
- Sensor size > reticle size → reticle stitching needed
- Different reticles:

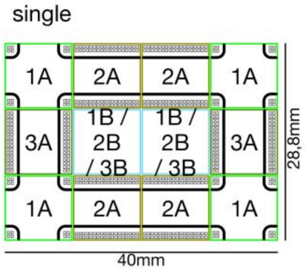
Edge guard ring reticles

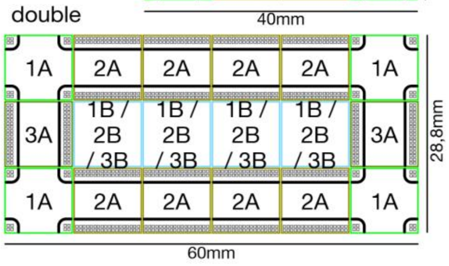
Center pixel reticles



- Repeat them for different designs:



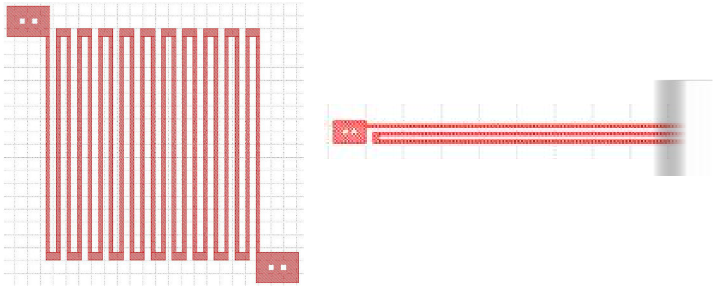




- Resistor biasing for all pixel flavors, likely benefitial to prevent cross talk
- Bias resistor: > 2 MΩ

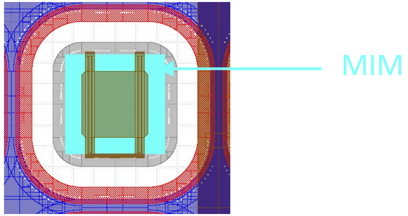
50 µm x 50 µm

25 µm x 100 µm



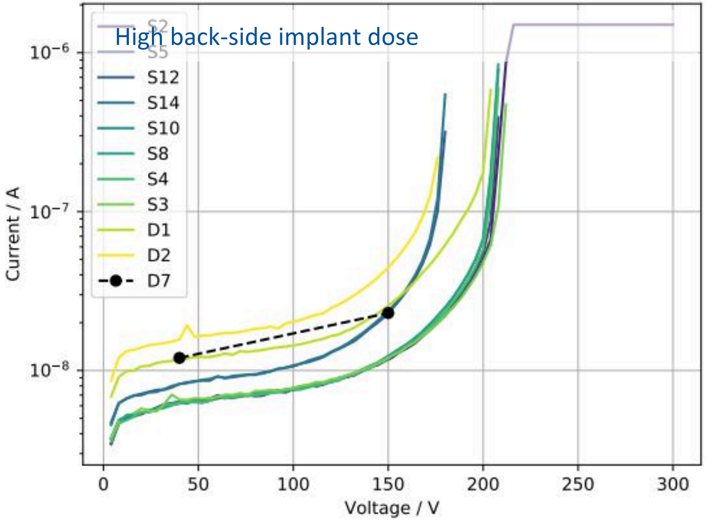
- AC coupled pixels:
  Using MIM capacitor in each pixel (0.56 pF)

50 µm x 50 µm

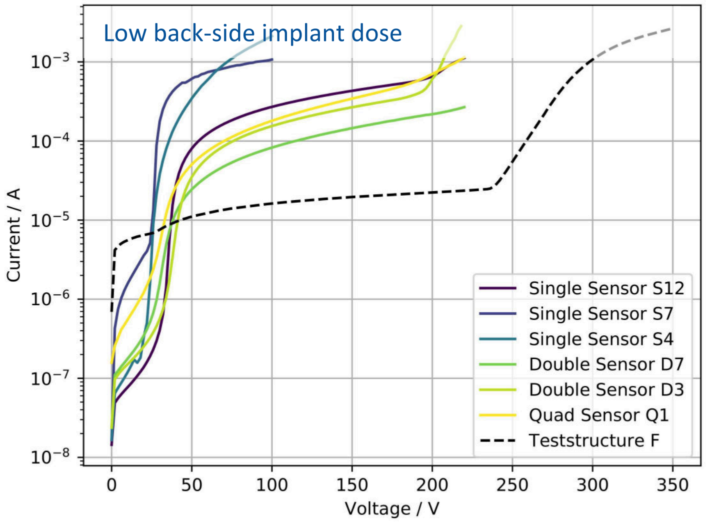


IV CURVES AND BACKSIDE PROCESSING

- Sensor requirements before irradiation ATLAS ITk:
  - V_{dep} ~ 30V (< 100V, for 150 um) ✔
  - I_{leak} < 0.75 μA/cm² @ 80V (V_{dep} + 50 V) ✔
  - V_{break} ~ 180-200 V (> V_{dep} + 70 V) ✔
- → Sensors fulfill specifications



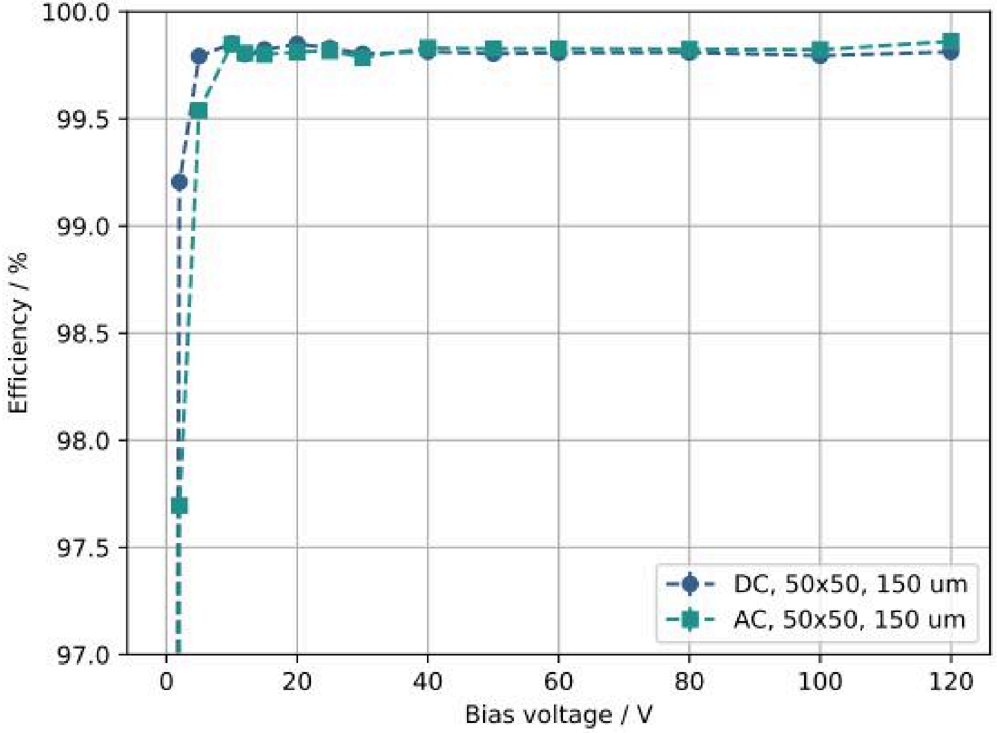
- Full-size submission: changed backside processing vendor to simplify potential production for ATLAS ITk
- All first-batch devices showed high current at full depletion (V_{dep} ~ 30 V), due to inadequate interface from bulk to backside metal
- Increase of implant dose solved issue



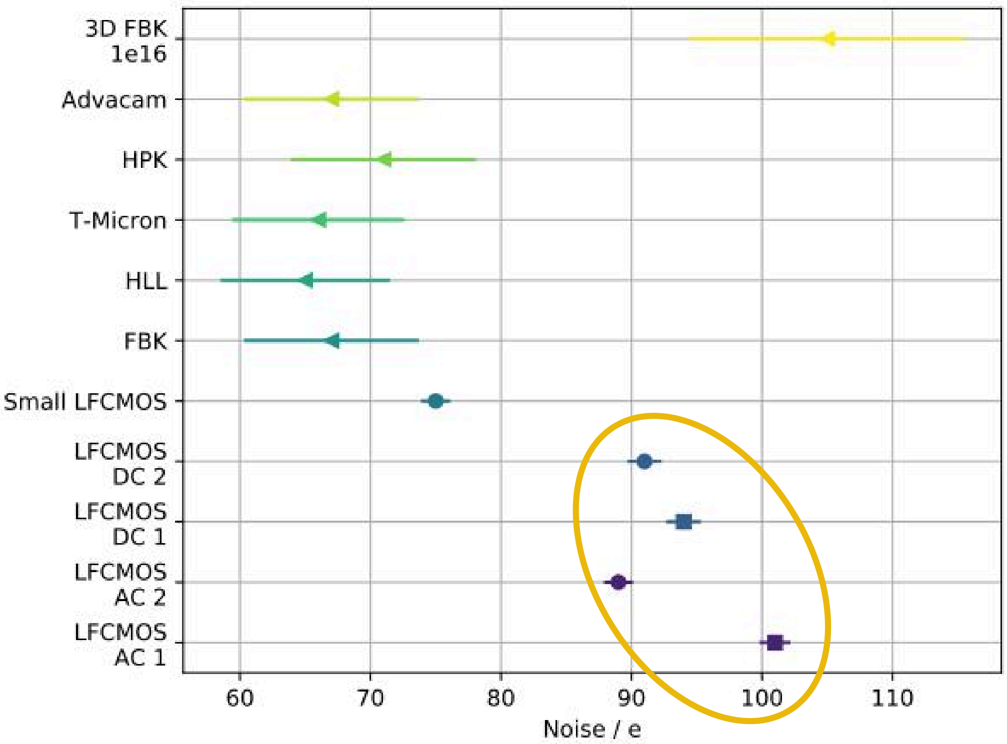
EFFICIENCY MEASUREMENT

- Detection efficiency measured @ DESY test beam in December 2020:
  - Perpenticular beam
  - 5 GeV electrons
  - 5 - 7 kHz trigger rate
- DUT conditions:
  - Linear FE of RD53A
  - Threshold: 1200 e
  - Noise occupancy: < 10^{-6}
  - 50 x 50 μm^2 pixel design
  - High BS implant dose
- Efficiency of both, DC and AC design above requirement (97%)
  - At 80 V (V_{dep} + 50 V):
    99.85 % efficiency
  - For V > V_{dep}:
    No difference between AC and DC

Efficiency of 150 um full-size passive CMOS sensor



NOISE COMPARISON



- Pure FE (LIN) noise: 60-65 e
- Other sensors:
  - Dual-chip module measurement (> 2 samples per vendor)
  - Larger error due to unkown charge calibration: assume 10 % uncertainty
- Only 50x50 μm^2 sensors measured, yet
- Noise of LFoundry sensors comparable to other sensors
- Likely slightly larger sensor capacitance than other sensor designs
- Capacitance to be measured

SUMMARY

- 100 µm, 50 x 50 µm² prototype:
  - Detection efficiency > 99% @ 1 x 10^{16} n_{eq}/cm^2 with RD53A
  - Large capacitance reduction possible for small fill-factor designs
- Inter-pixel isolation with field plates:
  - Sufficient inter-pixel resistance reached (> 10 MΩ)
  - Even at 1 x 10^{16} n_{eq}/cm^2
  - Capacitance benefits to be measured...
- 150 µm, full-size sensor of dedicated submission:
  - Sensors fullfill requirements (ATLAS ITk)
  - Irradiated devices cool down, to be measured after irradiation...
  - Next: build a quad module with RD53B