PASSIVE CMOS SENSORS FOR RADIATION-TOLERANT HYBRID PIXEL-DETECTORS

16. TRENTO WORKSHOP

Malte Backhaus\textsuperscript{a}, Yannick Dieter\textsuperscript{b}, Jochen Dingfelder\textsuperscript{b}, Tomasz Hemperek\textsuperscript{b}, Fabian Hügging\textsuperscript{b}, Hans Krüger\textsuperscript{b}, Anna Macchiolo\textsuperscript{c}, Daniel Münstermann\textsuperscript{d}, David-Leon Pohl\textsuperscript{b}, Tianyang Wang\textsuperscript{b}, Norbert Wermes\textsuperscript{b}, Pascal Wolf\textsuperscript{b}, Sinuo Zhang\textsuperscript{b}

\textsuperscript{a}. ETH Zürich
\textsuperscript{b}. Physikalisches Institut der Universität Bonn
\textsuperscript{c}. Physik-Institut der Universität Zürich
\textsuperscript{d}. Physics Department, Lancaster University
PASSIVE CMOS SENSORS

Use commercial high-voltage/high-resistive CMOS process for planar sensor production, no active components:

- **Large wafers** (200 mm)
- **High production throughput, low costs**
- **Poly-silicon resistors** → connection to a bias grid
- **MIM capacitors** for AC-coupling → no leakage current into readout
- **Many metal layers** for redistribution
- **Sub-pixel coding feasible?**
  
  [Link](https://doi.org/10.1016/j.nima.2020.164524)
- **Field plates for inter-pixel isolation?**

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**LFoundry 150 nm 1.8V CMOS process**

[http://www.nanoitaly.it/nanoitaly/images/presentazioni/PS_2_1-Fama.pdf](http://www.nanoitaly.it/nanoitaly/images/presentazioni/PS_2_1-Fama.pdf)

- MIM capacitor: 1 fF/µm², 2 fF/µm²
- Polysilicon resistor: ~ 2.2 kΩ/□
- 4 – 6 metal option, thick metal
- Back-side processing: thinning and implantation
- Lithographic stitching
**HISTORY OF PASSIVE CMOS SENSORS USING LFOUNDRY PROCESS**

**Large pixel prototype**
- 50 x 250 µm² pixels, ATLAS IBL planar geometry
- Performance comparable to ATLAS IBL sensors after irradiation > $1 \cdot 10^{15}\text{n}_{eq}/\text{cm}^2$
- Investigation of AC-coupling schema, pixel biasing schemes (bias dot vs. resistor biasing)

**Test structures**
- Many structures produced
- Varying designs: guard rings, pixel isolation, implantation geometries
- Investigations of break down with TID → Identified enhanced guard ring structure
- Investigation of sensor capacitances

**Small pixel prototype**
- 50 x 50 µm² pixels, ATLAS ITk pixel geometry

**Full size (quad) sensors**
- 50 x 50 µm² pixels, 25 x 100 µm² pixels
- Full-size ATLAS ITk pixel modules
- Participation in ATLAS ITk pixel sensor market survey
- RD53A and RD53B compatible

**Byproducts of DMAPS efforts**
- Large pixel prototype
- Test structures
- Small pixel prototypes on RD53A
- Full size (quad) sensors

**Dedicated submission**
- Single, dual, quad module sensors

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**SMALL PIXEL PROTOTYPE**

- High resistive 4-5 kΩ cm p-type CZ wafer
- 50 µm x 50 µm pixels in 64 × 64 matrix
- 100 µm thickness, backside implant, etching + metallization @ IBS France
- Bump bonded to RD53A @ IZM Berlin
- DC coupled pixels:
  - No biasing structure
  - Variation of implantation width: 15 µm - 30 µm
  - Variation of n-well depth: n-well (NW) and deep n-well (DNW)
- Irradiated at the Bonn HISKP Irradiation Facility
EFFICIENCY MEASUREMENT

- DUT operation conditions:
  - Threshold: \(~ 1000\) e
  - Noise occupancy: \(< 10^{-6}\)
  - Bias voltage \(< 400\) V, otherwise too many noisy pixels
- Before irradiation:
  > 99.5 % at 5 V only
- \(5 \times 10^{15} n_{eq}/cm^2\):
  > 99 % efficiency (@ 100 V)
- \(1 \times 10^{16} n_{eq}/cm^2\):
  > 99 % efficiency (@ 400 V)
- Mean efficiency for different fill-factors @ 400 V:
High bias voltage + large n-implants
Homogeneous efficiency within pixels

Flavors with small n-implants:
Efficiency loss at pixel corners (especially for low bias voltage)

→ Due to low electric field and charge sharing

IN-PIXEL EFFICIENCY @ 1 x 10^{16} n_{eq}/cm^2
CHARGE: UNIRRADIATED VS IRRADIATED

- Single-hit cluster-charge measurements with 5 GeV electrons
- Measured after charge calibration
- Using hit-bus TDC method

NW30 @ 350 V
(5 x 10^{15} \text{n}_{eq}/\text{cm}^2)

NW30 @ 80 V
(unirradiated)

NW30 @ 400 V
(1 x 10^{16} \text{n}_{eq}/\text{cm}^2)
SENSOR INPUT CAPACITANCE

- Capacitance measurement chip in TSMC 65 nm PixCap65:
  - ~ 0.3 fF precision
  - Ability to measure different contributions to input capacitance (inter-pixel, bump bonds, backplane)
- Publication: [https://doi.org/10.1088/1748-0221/16/01/P01029](https://doi.org/10.1088/1748-0221/16/01/P01029)

- Large reduction of capacitance when reducing p-stop distance to n-well: 23.5 fF -> 12.2 fF
- -> use no p-stop, but field plates?
INVESTIGATION OF THE INTER-PIXEL RESISTANCE

- **P-stop isolation** maintains a high inter-pixel resistance after irradiation
  - Advantage: low signal spreading, good spatial resolution
  - But: a dominating source of the detector capacitance

- **Idea:**
  - Substitute the p-stop by a field plate at inter-pixel regions
  - Electrostatic potential on field plate modifies the conductivity
    - Increase inter-pixel resistance
    - Remove the contribution of p-stop to the pixel capacitance

- Resistance measurement: apply voltage between neighboring pixel n-wells and measure current (voltage << bias voltage)
INVESTIGATION OF THE INTER-PIXEL RESISTANCE

- Test structure in LFoundry 150 nm CMOS, 50 x 50 µm² pixel matrix, irradiated with 12 MeV protons @ Bonn HISKP irradiation facility
- Before irradiation: High resistance for all isolation structures ($\sim 10^{13} - 10^{14} \Omega$)
- After irradiation: P-stop: $\sim 10^{11} \Omega$, Field-plate: $\sim 10^8 - \sim 10^{11} \Omega$ depending on bias

Measurements at 100 V bias

<table>
<thead>
<tr>
<th>Fluence [n$_{eq}$ cm$^{-2}$]</th>
<th>Resistance Field-plate: floating</th>
<th>Resistance Field-plate: 0 V</th>
<th>Resistance Field-plate: -100 V</th>
<th>Resistance with p-stop</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$\sim 5 \times 10^{13} \Omega$</td>
<td>$\sim 2 \times 10^{14} \Omega$</td>
<td>$\sim 2 \times 10^{14} \Omega$</td>
<td>$\sim 1.5 \times 10^{14} \Omega$</td>
<td>293 K</td>
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<td>$5 \times 10^{14}$</td>
<td>$4960 \times 10^6 \Omega$</td>
<td>$950 \times 10^6 \Omega$</td>
<td>$130 \times 10^9 \Omega$</td>
<td>$155 \times 10^9 \Omega$</td>
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<td>$1 \times 10^{15}$</td>
<td>$2580 \times 10^6 \Omega$</td>
<td>$520 \times 10^6 \Omega$</td>
<td>$160 \times 10^9 \Omega$</td>
<td>$110 \times 10^9 \Omega$</td>
<td>258 K</td>
</tr>
<tr>
<td>$5 \times 10^{15}$</td>
<td>$510 \times 10^6 \Omega$</td>
<td>$130 \times 10^6 \Omega$</td>
<td>$32 \times 10^9 \Omega$</td>
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<td>258 K</td>
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<td>$130 \times 10^6 \Omega$</td>
<td>$15 \times 10^9 \Omega$</td>
<td>$16 \times 10^9 \Omega$</td>
<td>258 K</td>
</tr>
</tbody>
</table>

- Requirement > 10 MΩ seems feasable?
- Next: measure capacitance for field-plates, X-Ray irradiations, and reproduce results with TCAD
FULL-SIZE PASSIVE CMOS SENSOR SUBMISSION

- Design (mainly by Tianyang Wang)
  - Different sizes for modules:
    - RD53A single and dual chip modules
    - RD53B quad modules
  - Different pixel flavors:
    - 50 x 50 \( \mu \text{m}^2 \) and 25 x 100 \( \mu \text{m}^2 \)
    - AC or DC coupled
  - Not only pixel sensors, also strip sensors: See previous talk
- Float-zone wafer material
- Thinning to 150 \( \mu \text{m} \) + handling wafer and backside implantation @ LFoundry
- Backside Al-Si metal + UBM + Flip-chip @ IZM Berlin
STITCHING AND BIASING

- Sensor size > reticle size \(\Rightarrow\) reticle stitching needed
- Different reticles:

  - **Edge guard ring reticles**
  - **Center pixel reticles**

- Repeat them for different designs:

- Resistor biasing for all pixel flavors, likely beneficial to prevent cross talk
- Bias resistor: > 2 MΩ

- AC coupled pixels:
  - Using MIM capacitor in each pixel (0.56 pF)
IV CURVES AND BACKSIDE PROCESSING

- **Sensor requirements** before irradiation ATLAS ITk:
  - \( V_{\text{dep}} \sim 30\,\text{V} \) (<100V, for 150 um)
  - \( I_{\text{leak}} < 0.75 \, \text{µA/cm}^2 \) @ 80V (\( V_{\text{dep}} + 50 \, \text{V} \))
  - \( V_{\text{break}} \sim 180-200 \, \text{V} \) (> \( V_{\text{dep}} + 70 \, \text{V} \))
  - → Sensors fulfill specifications

- **Full-size submission**: changed backside processing vendor to simplify potential production for ATLAS ITk

- All first-batch devices showed high current at full depletion (\( V_{\text{dep}} \sim 30\,\text{V} \)), due to inadequate interface from bulk to backside metal

- Increase of implant dose solved issue

![Graph of IV curves and backside processing](image.png)
Efficiency Measurement

- Detection efficiency measured @ DESY test beam in December 2020:
  - Perpendicular beam
  - 5 GeV electrons
  - 5 - 7 kHz trigger rate
- DUT conditions:
  - Linear FE of RD53A
  - Threshold: 1200 e
  - Noise occupancy: < 10^{-6}
  - 50 x 50 µm² pixel design
  - High BS implant dose
- Efficiency of both, DC and AC design above requirement (97%)
  - At 80 V (V_{dep} + 50 V): 99.85 % efficiency
  - For V > V_{dep}:
    No difference between AC and DC
NOISE COMPARISON

- Pure FE (LIN) noise: 60-65 e
- Other sensors:
  - Dual-chip module measurement (> 2 samples per vendor)
  - Larger error due to unknown charge calibration: assume 10% uncertainty
- Only 50x50 µm^2 sensors measured, yet
- Noise of LFoundry sensors comparable to other sensors
- Likely slightly larger sensor capacitance than other sensor designs
- Capacitance to be measured

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SUMMARY

- 100 µm, 50 x 50 µm² prototype:
  - Detection efficiency > 99% @ $1 \times 10^{16} n_{eq}/cm^2$ with RD53A
  - Large capacitance reduction possible for small fill-factor designs

- Inter-pixel isolation with field plates:
  - Sufficient inter-pixel resistance reached (> 10 MΩ)
  - Even at $1 \times 10^{16} n_{eq}/cm^2$
  - Capacitance benefits to be measured...

- 150 µm, full-size sensor of dedicated submission:
  - Sensors fulfill requirements (ATLAS ITk)
  - Irradiated devices cool down, to be measured after irradiation...
  - Next: build a quad module with RD53B