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Integrated Time-based Signal Processing Circuits for Harsh Radiation Environments

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RADSAGA Final Conference and Industrial event

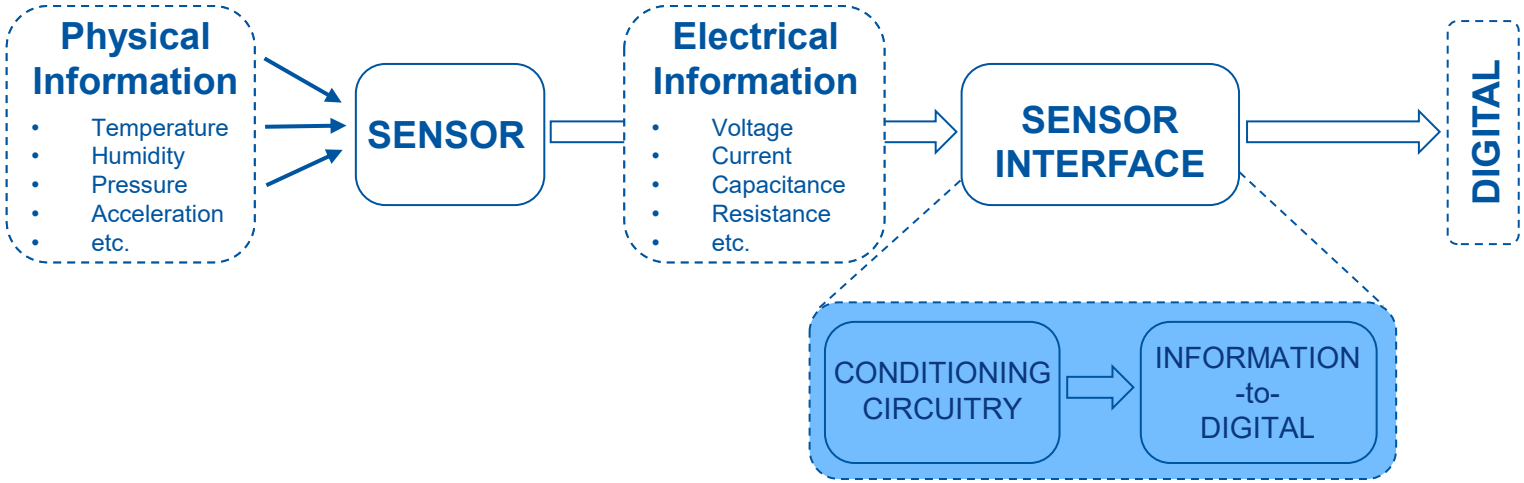
Arijit Karmakar, RADSAGA ESR 6, Work Package #2

RADiation and Reliability Challenges for Electronics used in Space, Aviation, Ground and Accelerators (RADSAGA) is a project funded by the European Commission under the Horizon2020 Framework Program under the Grant Agreement 721624. RADSAGA began in Mars 2017 and will run for 5 years.

Presentation outline

- Research Objectives
- Radiation Effects on Integrated Circuits
- Basics of Time-Domain Signal Processing
- Performance of Time-domain Circuits under Ionizing Radiation
- Rad-hard Time-based $\Delta\Sigma$ Capacitance-to-Digital Convertor
- Rad-hard Multi-Order $\Delta\Sigma$ Time-to-Digital Convertor
- Conclusion

Research Objectives



Design Challenges in sub-90 nm Technology

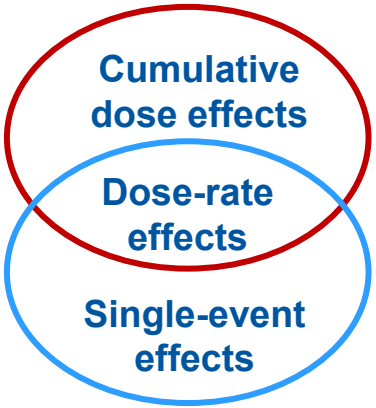
Radiation Tolerance

- Total Ionising Dose
- Single Event Effect
- …

System Performance

- Signal-to-noise Ratio (SNR)
- Dynamic Range
- …

Radiation Effects on Integrated Circuits



Cumulative dose effects

- Total Ionizing Dose (**TID**)
- Displacement Damage

Single-event effects

- Single-bit upset (**SBU**)
- Multiple-bit upset (**MBU**)

→ Single-event upset (**SEU**)

- Single-event functional interrupt (**SEFI**)

→ **Soft error** Non-destructive

- Single-event latchup (**SEL**)
- Single-event gate rupture/burnout (**SEGR/SEB**)

→ **Hard error** Destructive

Radiation Effects on Integrated Circuits

CMOS Scaling: TID ↓ SEE ↑

Decision steps to design Radiation-hardened interfaces

Device technology to counter TID

(65nm CMOS Technology)

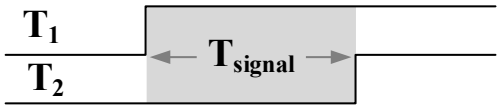
→

Signal processing technique (voltage/time) to counter SEE

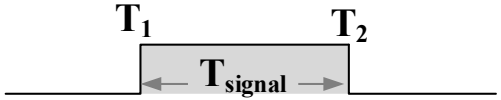
(Time-Domain)

Basics of Time-Domain Signal Processing

- 'T_{signal}' is time difference or interval between two time events.



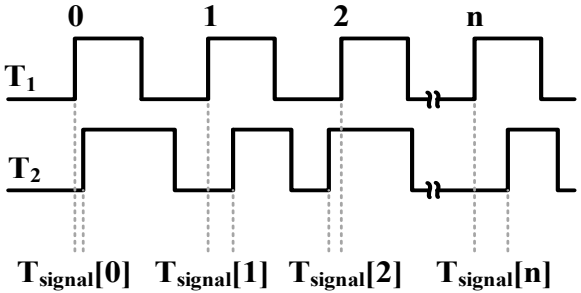
$$T_{signal} = T_2 - T_1$$

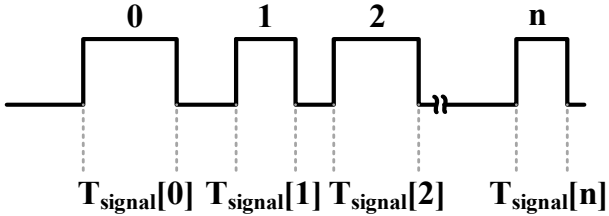


Bipolar information

Unipolar information

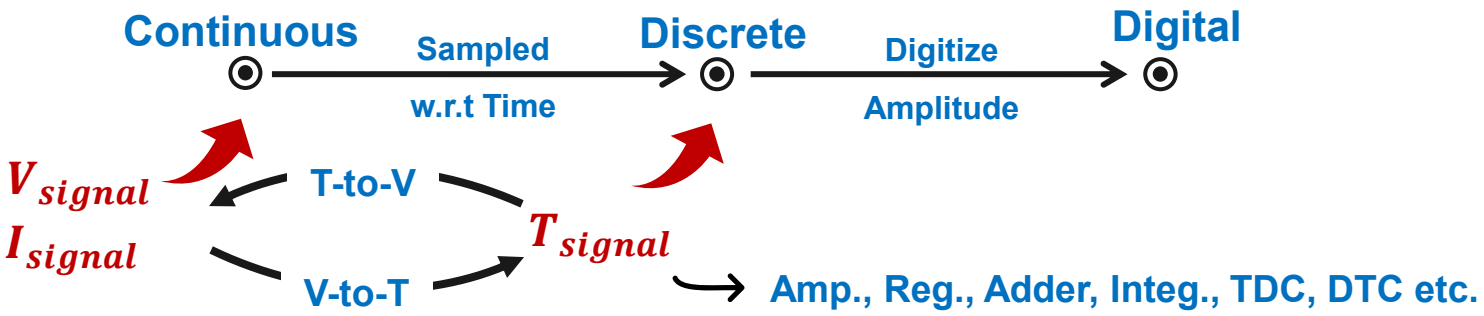
- Inherently always sampled with respect to Time. i.e, discrete-time.





Basics of Time-Domain Signal Processing

Signal Processing Flow



Advantages of Time-domain Signal Processing:

- Pseudo-digital circuits built using digital gates.
- Scaling friendly and inherited noise immunity of digital circuits.

Performance of Time-domain Circuits under Ionizing Radiation

Total Ionizing Dose (TID)

- **Cause:** change in Vth, leakage current
- **Effect:** Variation in reference time-delays or frequencies.

Prevention method:

- No well-known circuit techniques !!
- Use scaled CMOS technologies.
- Wider (W>1 um) device sizes and enclosed gate layout

Correction method:

- Calibration using PLLs or DLLs
  - → Foreground calibration for low dose rate
  - → Background calibration for high dose rate

Time-domain ~ Voltage-domain

Single Event Effect (SEE)

- **Cause:** SET, SEU.
- **Effect:** Transient in time-domain signal, bit-flip or change in logic.

Prevention method:

- Using low bandwidth implementation
- High impedances at sensitive nodes.

Correction method:

- Triple modular redundancy
- Digitally assisted calibration to correct logics

Time-domain > Voltage-domain

Rad-hard Time-domain ΔΣ Capacitance-to-Digital Convertor

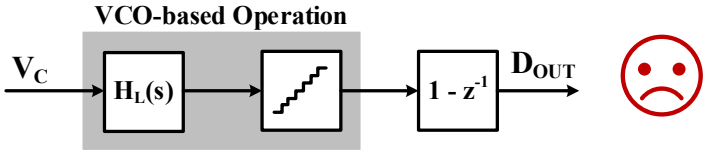
Prior- art

Capacitance Sensors Applications: Pressure, humidity, flow, displacement, acceleration etc…

Energy efficiency (SAR Type) ⇄ **Resolution (ΔΣ Type)**

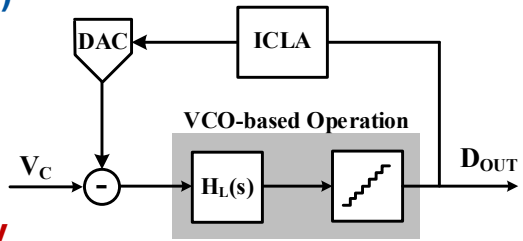
Time-domain ΔΣ → **OTAs** ✗ **VCO/ TD Integ.** ✓ **Power Efficient**

Hybrid Techniques (Time-domain +Voltage-domain)



Open-loop Operation
[Sanyal, JSSC'17]

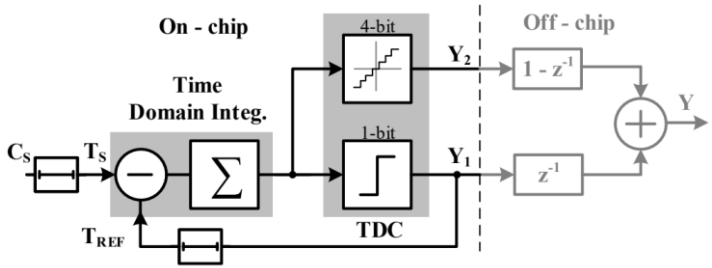
Non-linearity



Closed-loop Operation
[Tang, JSSC'20]

Rad-hard Time-domain ΔΣ Capacitance-to-Digital Convertor

Architecture overview



$C_S \in [0, C_{FS}]$ $T_S \in [T_o, T_{FS}]$ $T_{REF} = T_o$, when $Y_1 = 0$

T_{FS}, when $Y_1 = 1$

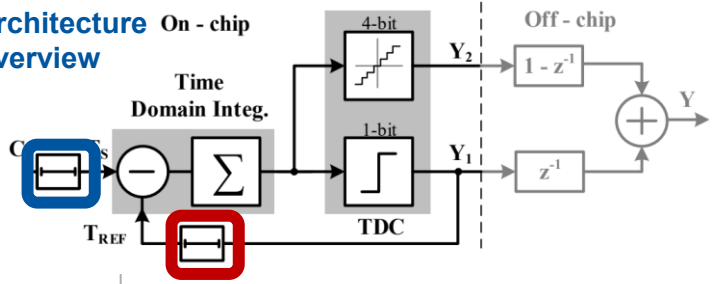
$$Y = C_S z^{-1} + Q_2 z^{-0.5}(1 - z^{-1})$$

- TID mitigation
  - DLL based calibration
  - Wider devices
- SEE mitigation
  - TMR/ majority voter
  - Bubble Error correction

Rad-hard Time-domain ΔΣ Capacitance-to-Digital Convertor

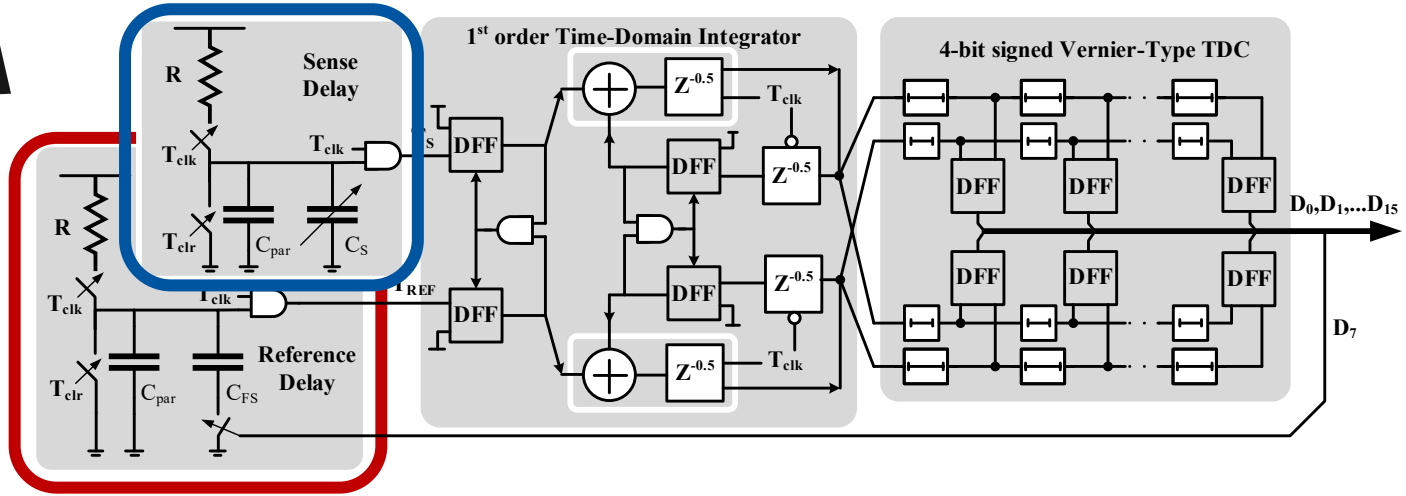
Circuit Implementations

Architecture overview



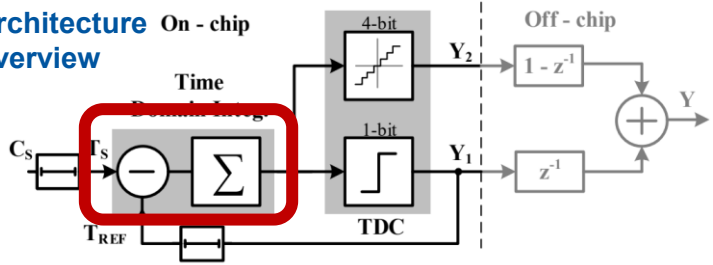
$$T_S = k_R(C_S + C_{par}), \quad T_{REF} = k_R(C_{FS} + C_{par})$$

where, $k_R = Rln\frac{V_{DD}}{V_{DD} - V_{TH}}$

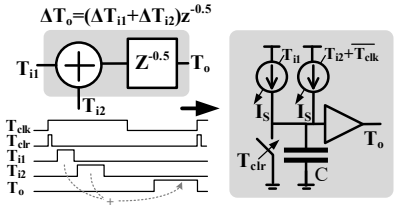


Rad-hard Time-domain ΔΣ Capacitance-to-Digital Convertor

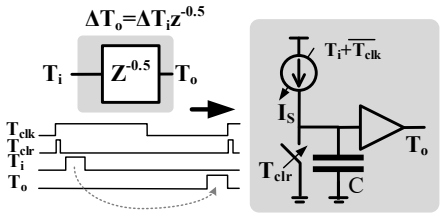
Architecture overview



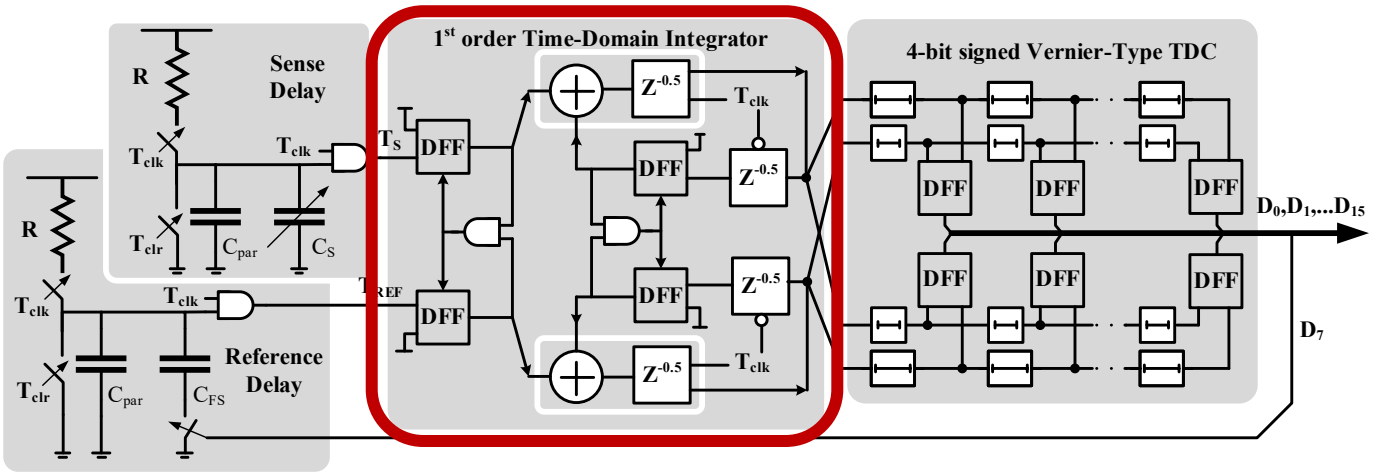
Circuit Implementations



Time-Domain Adder



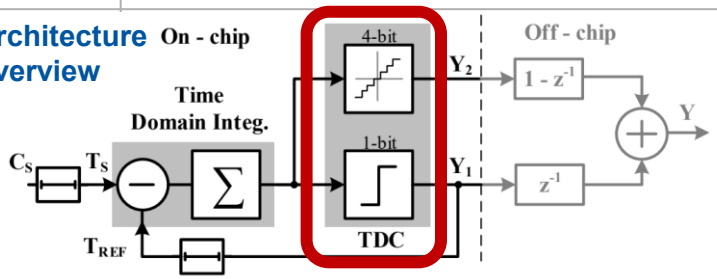
Time-Domain Register

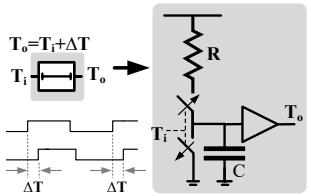


Rad-hard Time-domain ΔΣ Capacitance-to-Digital Convertor

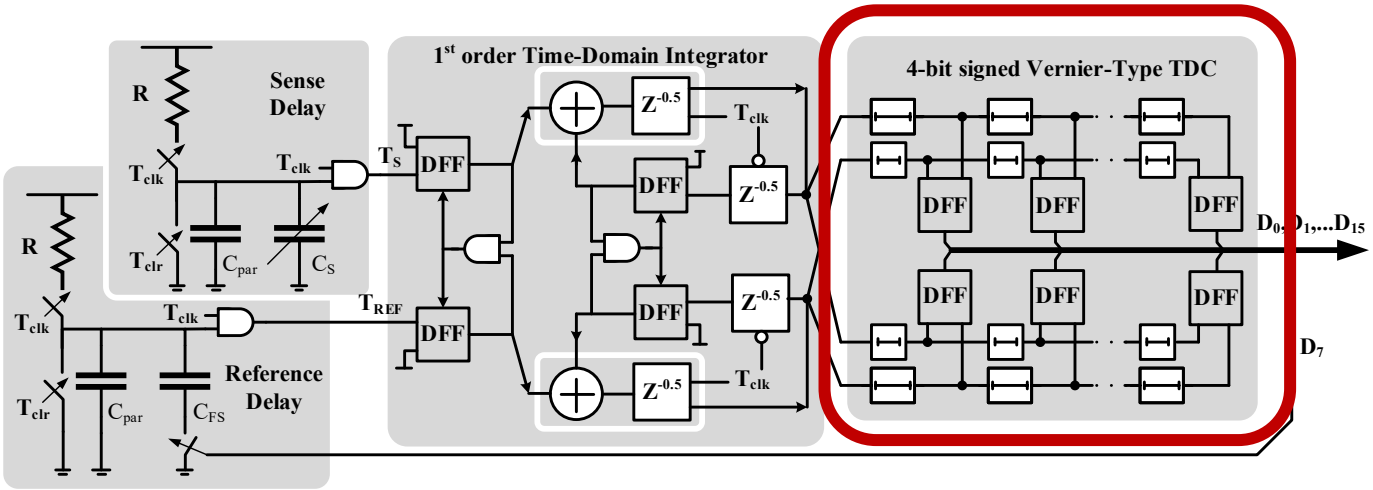
Circuit Implementations

Architecture overview



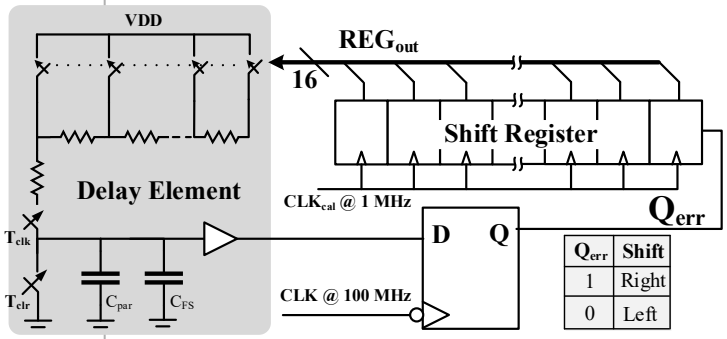


Delay Elements

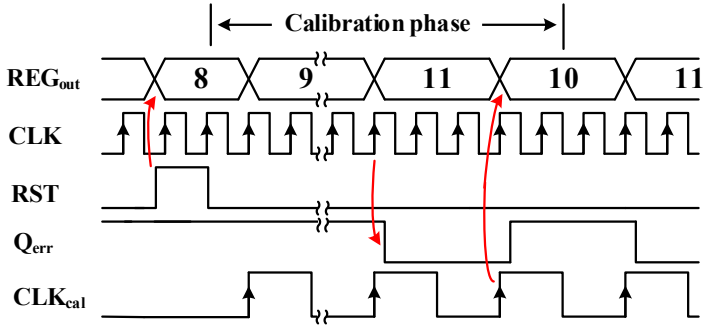


Rad-hard Hardened Time-domain ΔΣ Capacitance-to-Digital Convertor

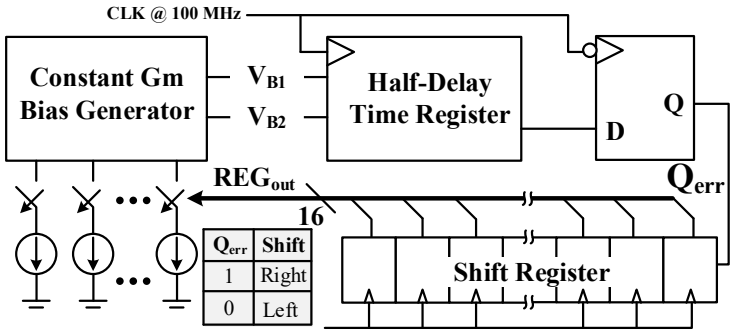
Calibration circuit



Delay element calibration



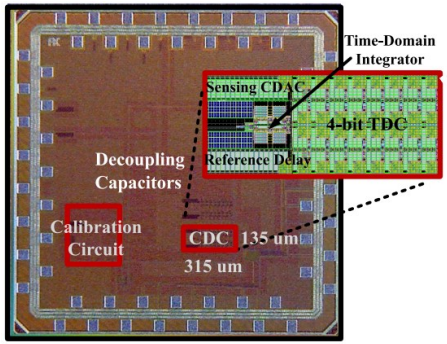
Timing Diagram



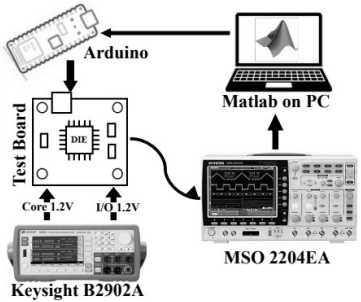
Bias Current calibration

Rad-hard Time-domain ΔΣ Capacitance-to-Digital Convertor

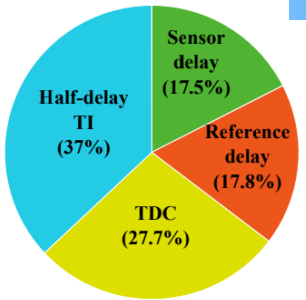
Measurement Results



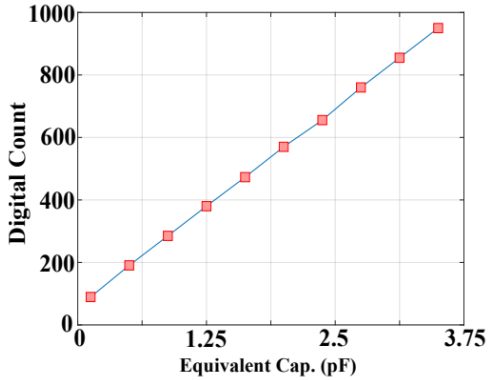
Die micrograph

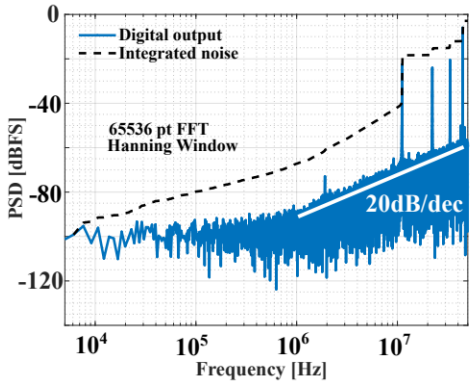


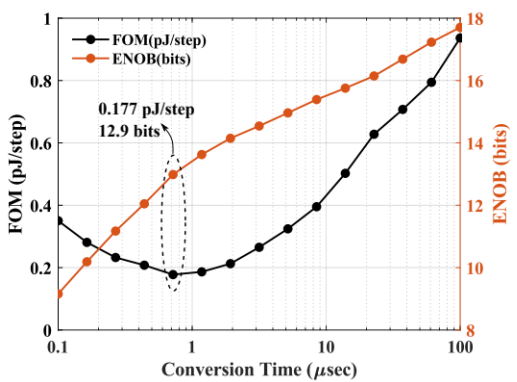
Test Setup



Power Breakdown







Rad-hard Time-domain ΔΣ Capacitance-to-Digital Convertor

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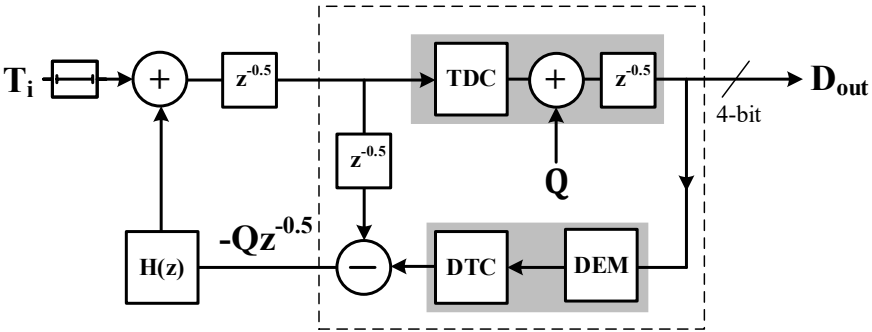
Measurement Results

	JSSC-20 [5]	JSSC-17 [10]	**This Work**	TIM-19 [11]	TCASI-18 [12]	JSSC-19 [1]	ISSCC-15 [13]
Process (nm)	40	40	**65**	180	180	180	160
Method	Time + Voltage	Time + Voltage	**Time**	Voltage	Voltage	Voltage	Time
Topology	ΔΣ+SAR	SAR+VCO	ΔΣ	SAR	ΔΣ	ΔΣ+SAR	PM†
Power Supply (V)	0.6/1.1	1	**1.2**	0.8/1	1.5	1.1	1
Cap. Range (pF)	0-5	0-5	**0-3.75**	0-3.6	1-10^5	0-18.12	0-8
Conv. Time (μs)	12.5	1	**0.76**	810	128	850	210
Energy (nJ)	0.083	0.075	**1.52**	1.28	1.92	2.62	2.902
ENOB(bits)	12.3	10.4	**12.9**	12.7	13	11.8	10.6
SNR(dB)	75.8	64.2	**79.4**	78.5	80	72.8	65.6
FOM(fJ/step)	16	55	**177**	187	230	660	1870

†PM= Pulse-width Modulation

Rad-hard Multi-order ΔΣ Time-to-Digital Convertor



$$D_{out} = T_i z^{-1} + Qz^{-0.5}(1 - H.z^{-1})$$

Configurable Time-domain FIR filter

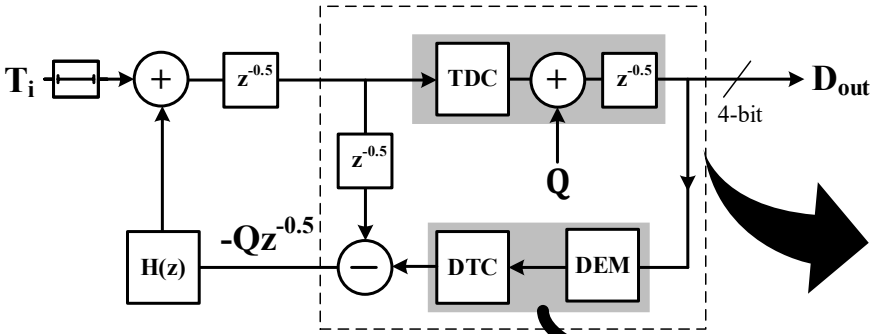
For 1st order, $H(z) = 1$

For 2nd order, $H(z) = 2 - z^{-1}$

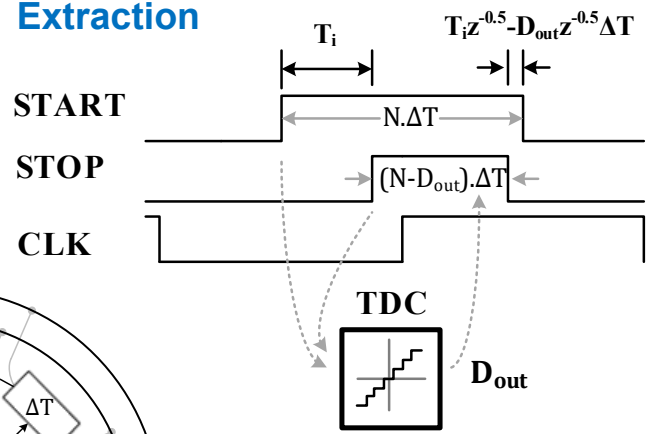
For 3rd order, $H(z) = 3(1 - z^{-1}) + z^{-2}$

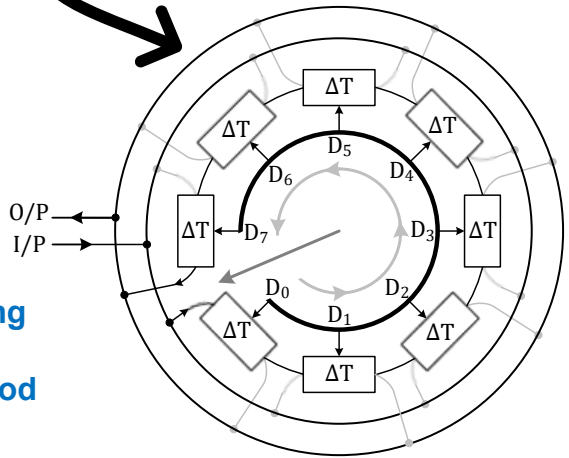
- **Key Features:**
  - **Target Spec:**
    - PWR <5 uW @10MSa/s,
    - ENOB >12 bit, FoM <50 fJ/step
  - **TID mitigation**
    - DLL based calibration
  - **SEE mitigation**
    - TMR (FIR filter and DTC block)
    - Bubble Error correction (TDC)

Rad-hard Multi-order ΔΣ Time-to-Digital Convertor



Quantization Noise Extraction





DTC+DEM (N~7) using Individual Level Averaging (ILA) Method

Conclusion

- Research Goal: Implement rad-hard time-domain sensor interfaces (immune against TID and SEEs).
- Key learning : SEE can be mitigated at circuit level but TID effects are primarily reduced by choosing appropriate process technology.
- Performance of Time-domain circuits is better than voltage–domain circuits in terms of SEE, but similar in terms of TID.
- Designs discussed:
  - Rad-hard CDC
  - Rad-hard TDC (ongoing).

Conclusion

Publications:

- A. Karmakar, V. De Smedt, and P. Leroux, “Pseudo-Differential Time-Domain Integrator Using Charge-Based Time-Domain Circuits,” in 2021 *IEEE 12th Latin American Symposium on Circuits and Systems* (LASCAS), 2021.
- A. Karmakar, V. De Smedt, and P. Leroux, “A 0.18 pJ/step Time-Domain 1st Order ΔΣ Capacitance-to-Digital Converter in 65-nm CMOS,” in 2021 *IEEE International Symposium on Circuits and Systems* (ISCAS), 2021.

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Thank you!

Questions

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