RADSAGA

Radiation hardening digital circuits against SET using design techniques

17-19 May, 2021

RADSAGA Final Conference and Industrial event

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RADiation and Reliability Challenges for Electronics used in Space, Aviation, Ground and Accelerators (RADSAGA) is a project funded by the European Commission under the Horizon2020 Framework Program under the Grant Agreement 721624. RADSAGA began in Mars 2017 and will run for 5 years.

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Presentation outline

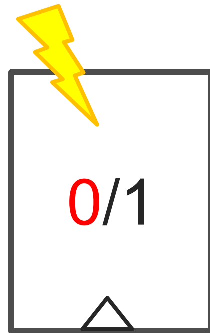
- ❑ Introduction
- ❑ Objectives
- ❑ Methodology
- ❑ Hardening techniques
  - ❑ Layout level
  - ❑ Circuit level
  - ❑ Hardness Improvement
- ❑ Conclusions

Introduction

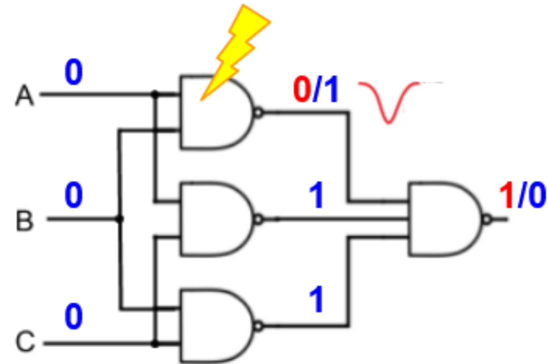
Single-Event Effects:

Radiation effects from a **single particle strike** at the device leading to **nondestructive** (*soft errors*) or destructive faults.

Single-Event Upset (SEU)



Single-Event Transient (SET)



Objectives

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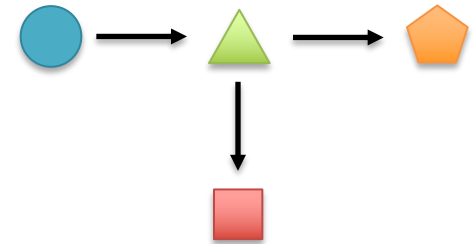
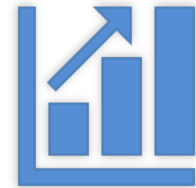
1. Propose a **general methodology based on a simulation chain** to predict the SEE susceptibility of digital circuits



2. Provide analysis of hardening techniques at design level and **propose guidelines to improve their efficiency**



Methodology

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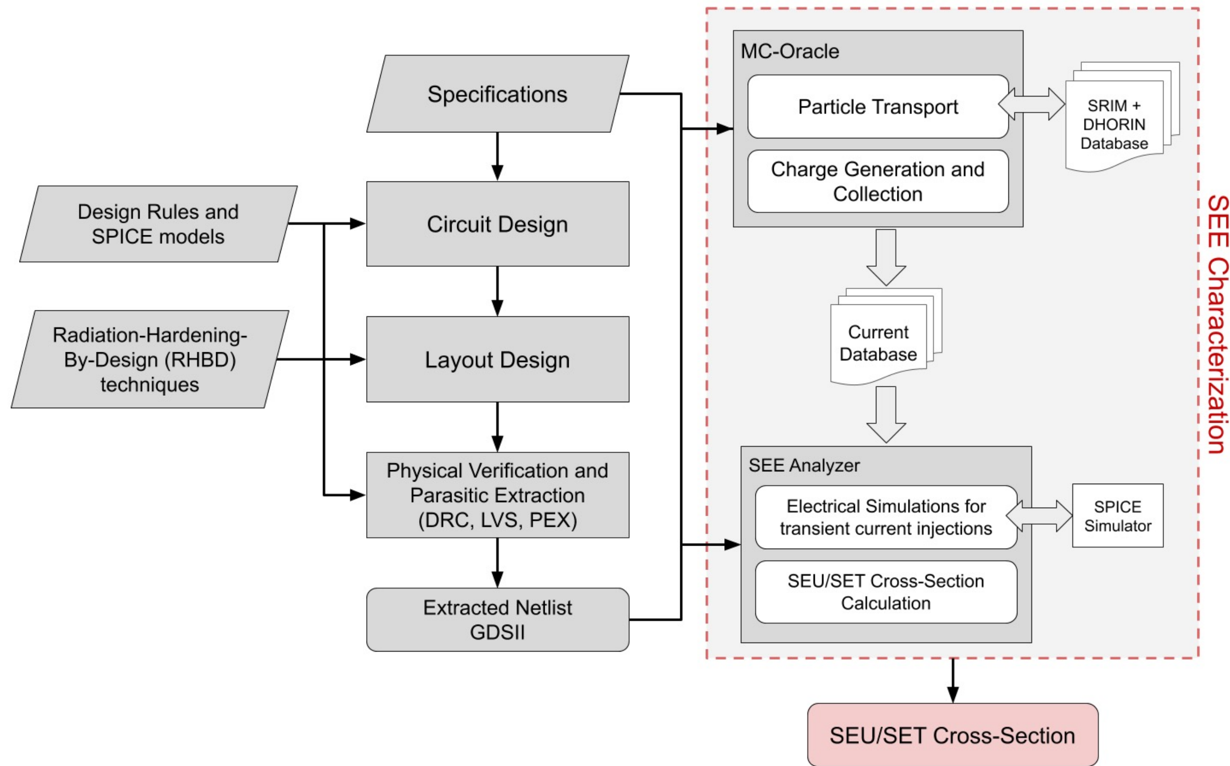

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Hardening techniques

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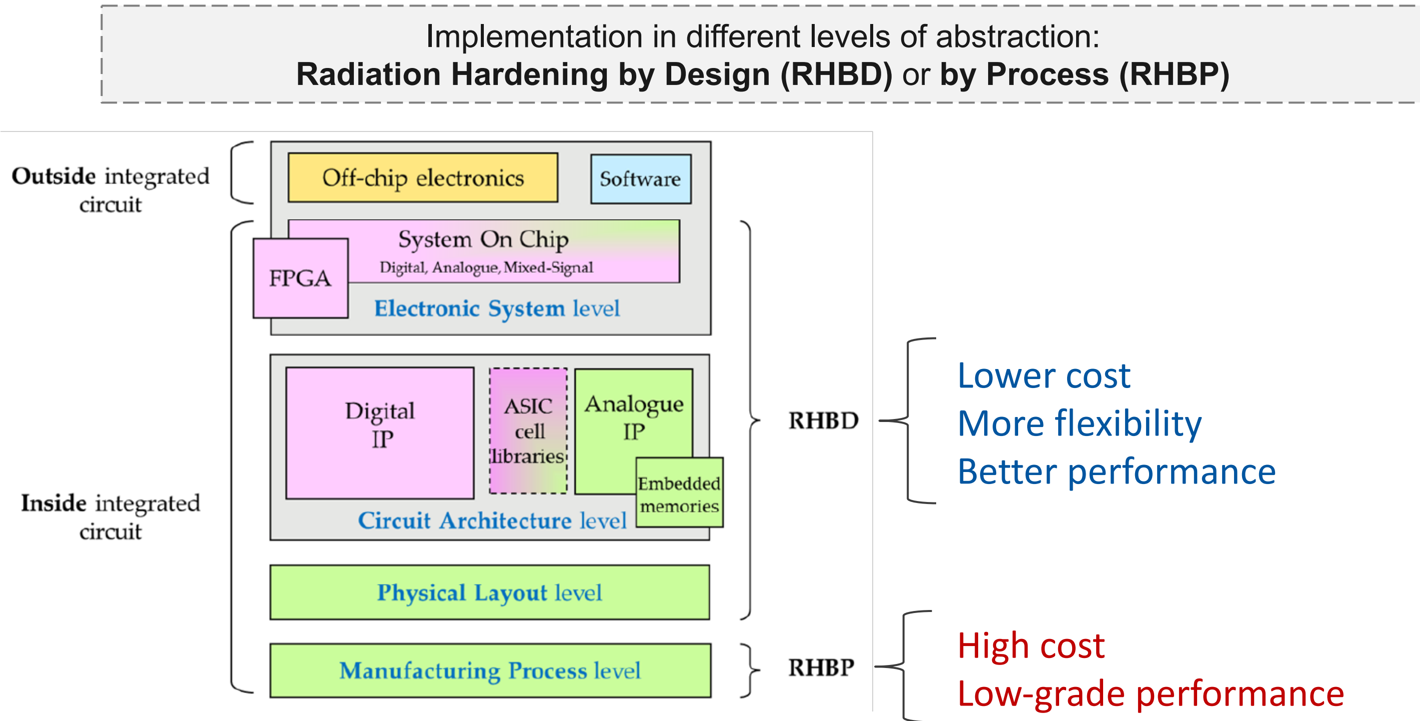
Implementation in different levels of abstraction:
Radiation Hardening by Design (RHBD) or **by Process (RHBP)**



ECSS-Q-HB-60-02A
Space Product Assurance: Techniques for radiation effects mitigation in ASICs and FPGAs handbook

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Gate Sizing and Transistor Stacking

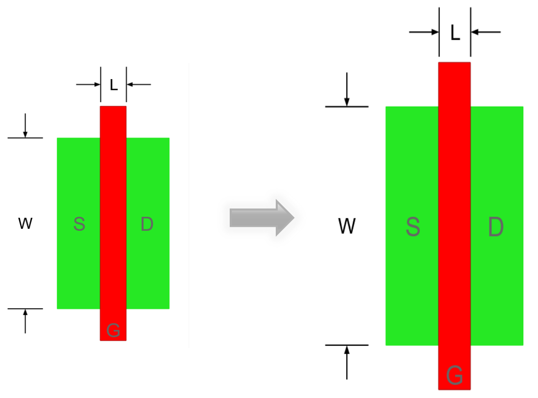
Y.Q. Aguiar et al. Radiation Hardening Efficiency of Gate Sizing and Transistor Stacking based on Standard Cells, **Microelectronics Relliability**, 2019

Selective Node Hardening:

To harden a circuit by selectively using logic gates that **minimize the SET generation or propagation** in the **most vulnerable nodes** of a complex VLSI design.

Gate Sizing:

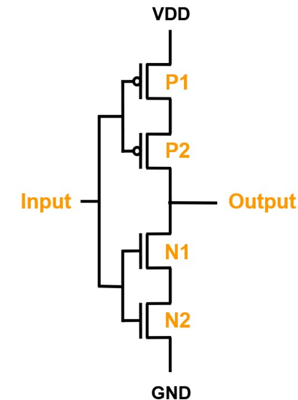
increases circuit capacitance and drive current.



Discrete process when using std cells!

Transistor Stacking:

increases circuit capacitance and **reduces leakage current**.



Gate Sizing and Transistor Stacking

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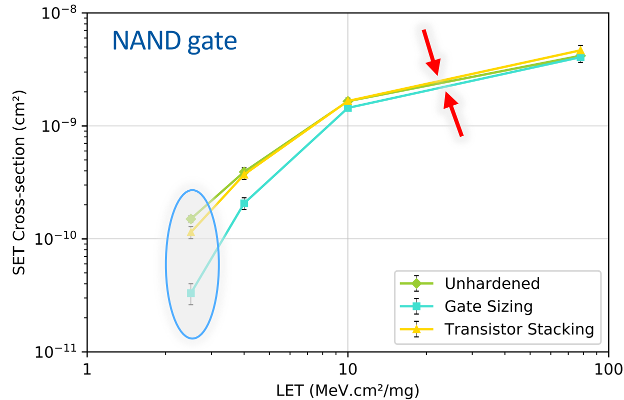
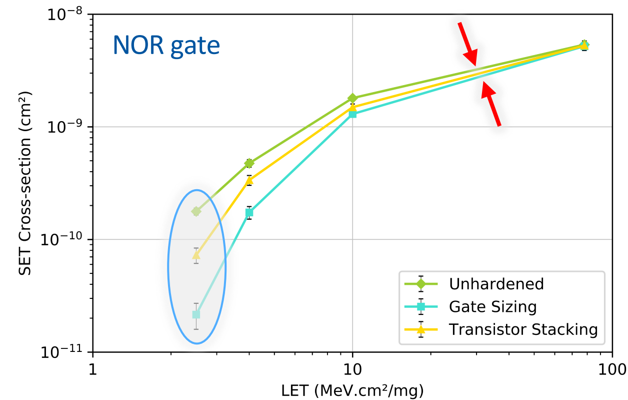
Y.Q. Aguiar et al. *Radiation Hardening Efficiency of Gate Sizing and Transistor Stacking based on Standard Cells*, **Microelectronics Reliability**, 2019

The cross-section was calculated for each input signal combination and the **arithmetic mean** for each particle LET is shown:



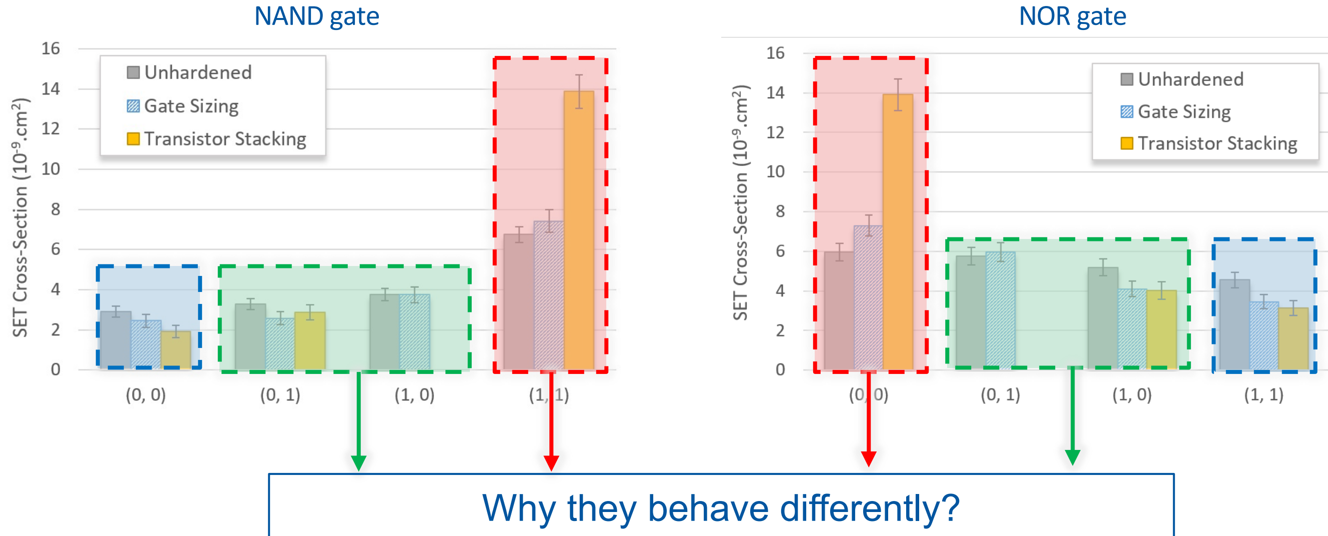


The efficiency of both techniques reduces as the particle LET increases.

For higher particle LET, the dominant effect on the circuit reliability is the charge collection efficiency enhanced by the larger transistors.

SET Input Dependence

Y.Q. Aguiar et al. *Radiation Hardening Efficiency of Gate Sizing and Transistor Stacking based on Standard Cells*, **Microelectronics Relliability**, 2019



- Impact of the transistor network for each input scenario:
  - Different restoring currents
  - Different collection areas

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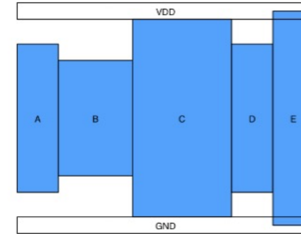
Transistor Folding Layout

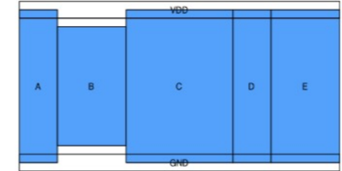
Y.Q. Aguiar et al. Exploiting Transistor Folding Layout as RHBD Technique against Single-Event Transients, **IEEE Transactions on Nuclear Science**, 2020.

It is used to provide **layout regularity** in standard-cell layout designs.

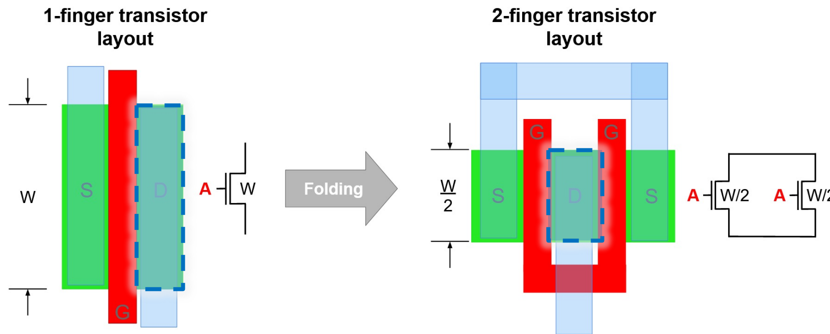
A large transistor can be implemented by adopting smaller transistors in parallel



(a) Different cell heights for non-folded designs



(b) Folded designs

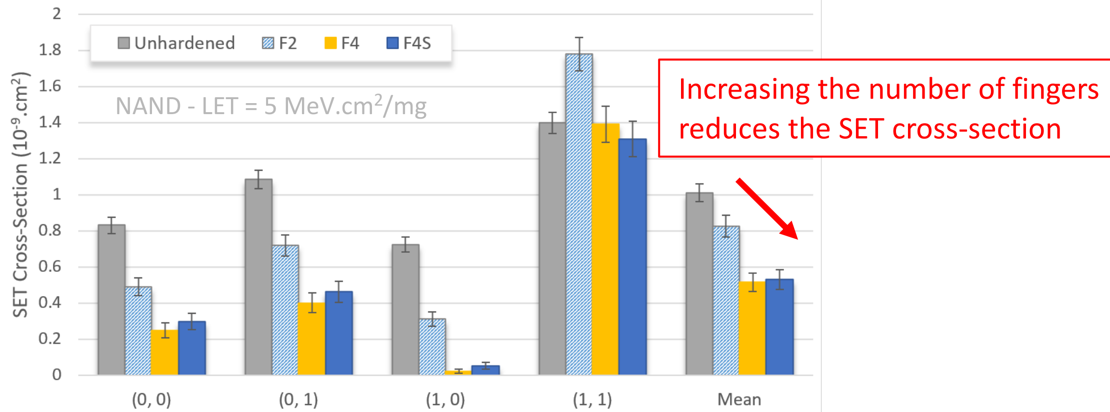


Reduced collecting drain area while maintaining the **same drive strength**.

Attractive to radiation hardening

Transistor Folding Layout

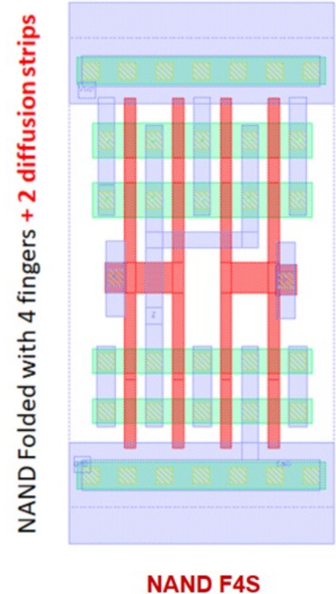
Y.Q. Aguiar et al. *Exploiting Transistor Folding Layout as RHBD Technique against Single-Event Transients*, **IEEE Transactions on Nuclear Science**, 2020.



Increasing the number of fingers reduces the SET cross-section

The technique shows a great **input dependence** and **LET dependence**

- **Diffusion Splitting** (DS) technique
- Asymmetric designs



NAND F4S

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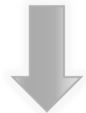
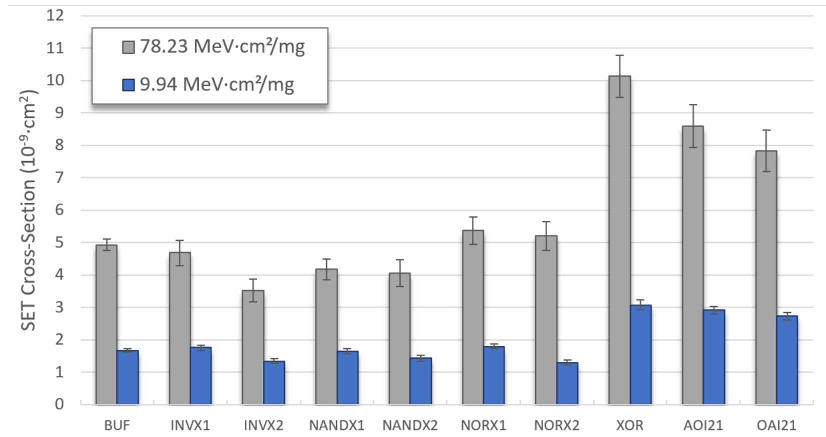
Impact of Logical Synthesis

- The logic synthesis determines the main characteristics of a circuit design: **performance, power consumption, area usage** and its **reliability.**
- Each standard cell provided in a cell library shows different SEE sensitivity.

Assessment of the SET immunity of single cells and combinations of cells



Reliability-driven synthesis

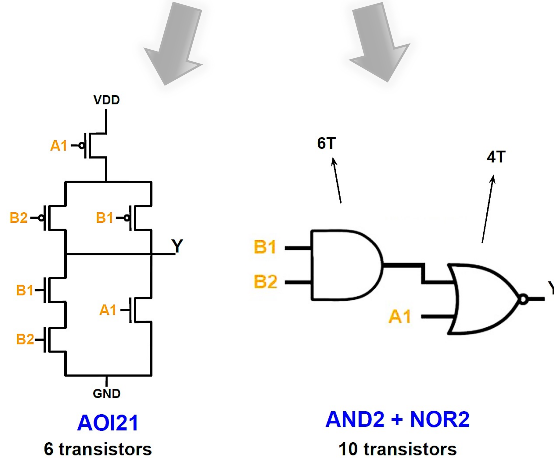


Y.Q. Aguiar et al. *Mitigation and Predictive Assessment of SET Immunity of Digital Logic Circuits for Space Missions*, ***Aerospace***, 2020

Technology Mapping

Technology mapping: boolean functions are translated to logic gates (INV, NAND, NOR…)

$$Y = \neg(A1 \wedge (B1 \vee B2))$$



AOI21
6 transistors

AND2 + NOR2
10 transistors

- ~42% in the total layout area
- ~14% reduction of the total collection area

Table 1
Total area for each cell layout design, total sensitive region and P-hit and N-hit sensitive area (μm^2)

	Layout Area	Total Collection Area	P-hit Collection Area	N-hit Collection Area
NOR2	0.895	0.212	0.154	0.058
AND2	1.193	0.205	0.110	0.095
AOI21	1.193	0.359	0.243	0.116
AND + NOR	2.088	0.418	0.265	0.153

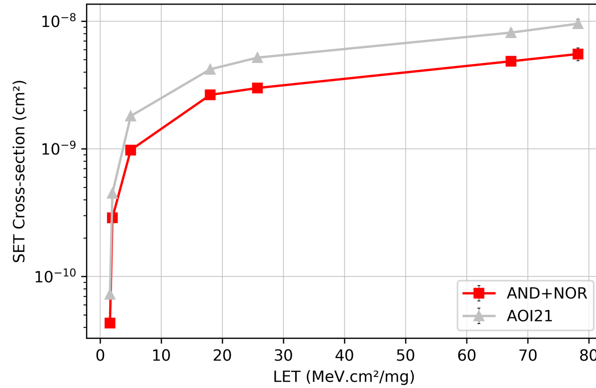
Complex-logic gates are widely used to **improve performance, reduce power consumption and layout usage**.

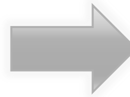
Improved radiation robustness?

Y.Q. Aguiar et al. *Impact of Complex-Logic Cell Layout on the Single-Event Transient Sensitivity*, ***IEEE Transactions on Nuclear Science***, 2019.

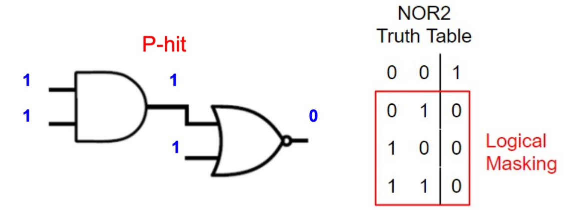
Technology Mapping

Y.Q. Aguiar et al. *Impact of Complex-Logic Cell Layout on the Single-Event Transient Sensitivity*, ***IEEE Transactions on Nuclear Science***, 2019.

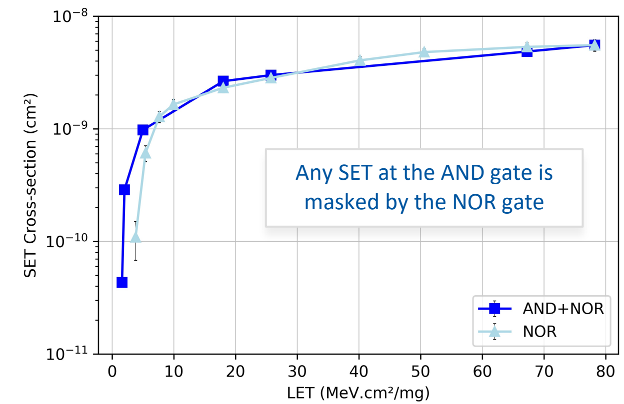




The complex-logic gate **eliminates** the **Logic Masking Effect!**



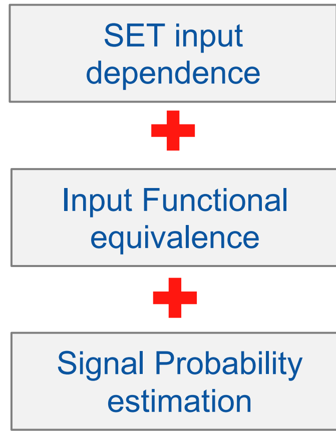
0	0	1
0	1	0
1	0	0
1	1	0

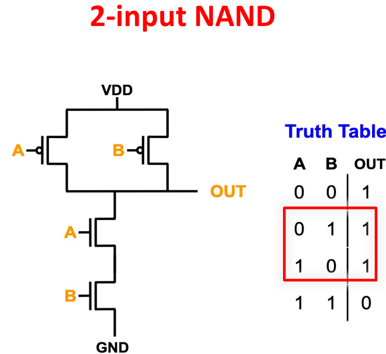


Technology mapping can benefit from these analysis to generate an SET-aware gate netlist.

Pin Assignment

The SET characterization of logic gates presents an **input dependence** due to the different interplay relation of sensitive collecting areas and restoring current.





(0, 1) and **(1, 0)** are the interchangeable input combinations

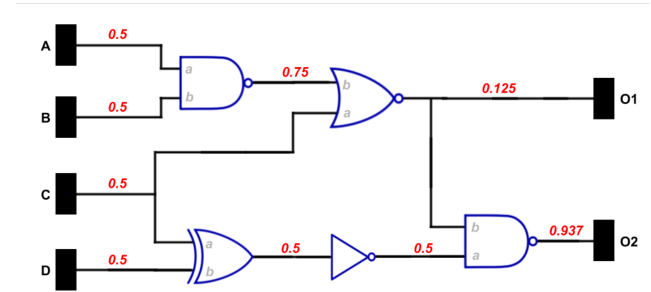


Table 5.4: Signal Probability Estimation for the INV, NAND, NOR and XOR gates

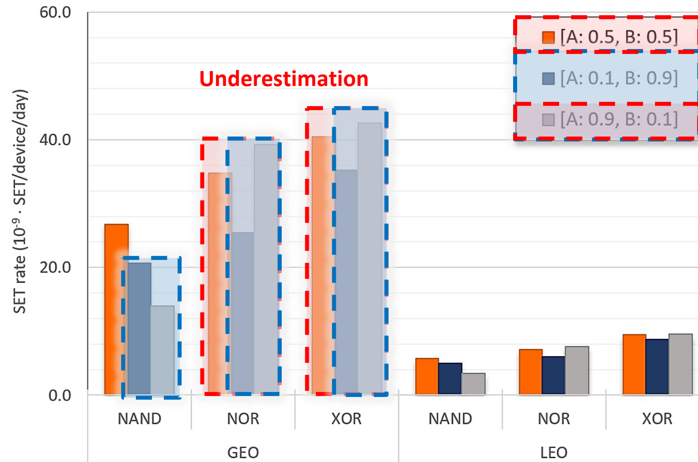
Cells	Input Signals	Output Signal Probability [1]
INV	1: a	$P_{INV} = 1 - p_A$
NAND	2: a, b	$P_{NAND} = 1 - (p_A \times p_B)$
NOR	2: a, b	$P_{NOR} = (1 - p_A) \times (1 - p_B)$
XOR	2: a, b	$P_{XOR} = p_A \times (1 - p_B) + p_B \times (1 - p_A)$

[1] Signal probability is the probability of the signal to be at logic value 1

Y.Q. Aguiar et al. *Reliability-driven pin assignment optimization to improve in-orbit soft-error rate*, ***Microelectronics Reliability***, 2019.

Pin Assignment

Y.Q. Aguiar et al. Reliability-driven pin assignment optimization to improve in-orbit soft-error rate, ***Microelectronics Reliability***, 2019.



- Not considering the input dependence can lead to the underestimation of the circuit sensitivity
- For lower SET rate, the **lowest signal probability** should be assigned to the input pin:
  - **A** for NOR and XOR gate
  - **B** for NAND gate

Pin assignment can reduce the SET rate and provide an application-specific hardening without any increase in area.

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Hardness Improvement of RHBD techniques

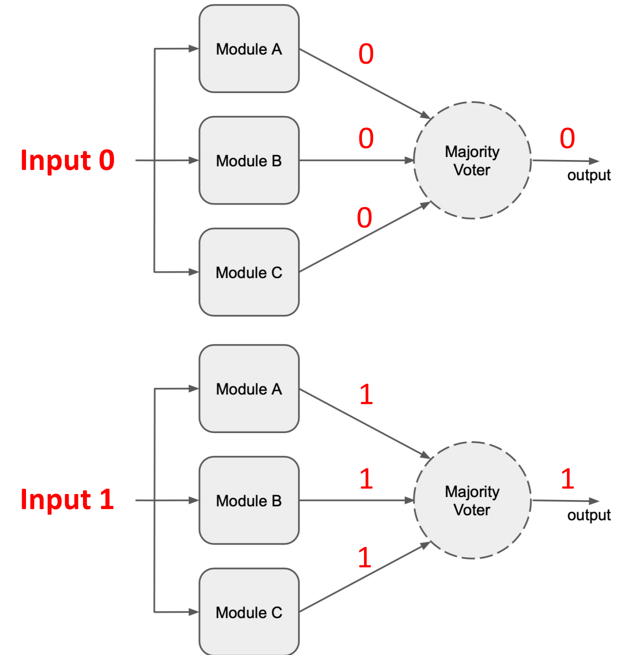
Y.Q. Aguiar et al. *Design exploration of majority voter architectures based on the signal probability for TMR strategy optimization in space applications*, ***Microelectronics Reliability***, 2020.

Triple-Modular Redundancy (TMR): critical component or electronic circuit is triplicated and their outputs are connected to a majority voter (MJV) architecture.

BUT…

Faults in the MJV cannot be masked

Signal probability of the TMR node can reduce the sensitivity of the MJV architecture based on its **input dependence**



Input configuration in a **fault-free TMR condition**

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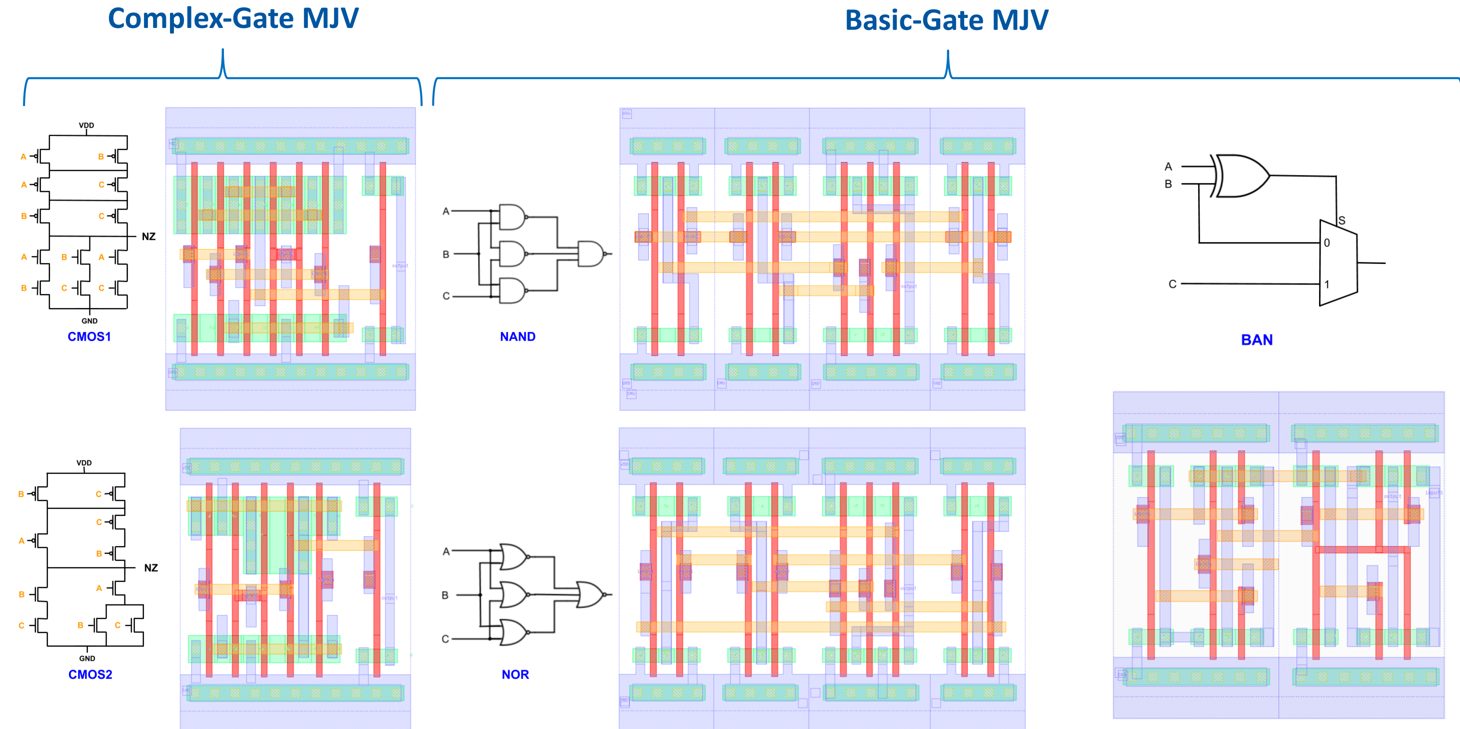
Hardness Improvement of RHBD techniques

Y.Q. Aguiar et al. Design exploration of majority voter architectures based on the signal probability for TMR strategy optimization in space applications, ***Microelectronics Reliability***, 2020.

Five majority voter architectures exploring complex-logic design and basic logic gates:



Hardness Improvement of RHBD techniques

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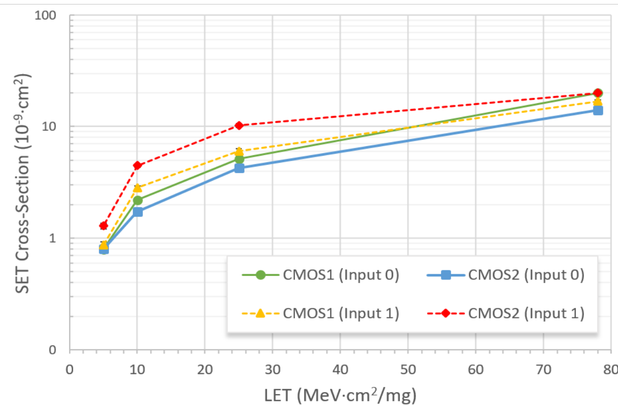
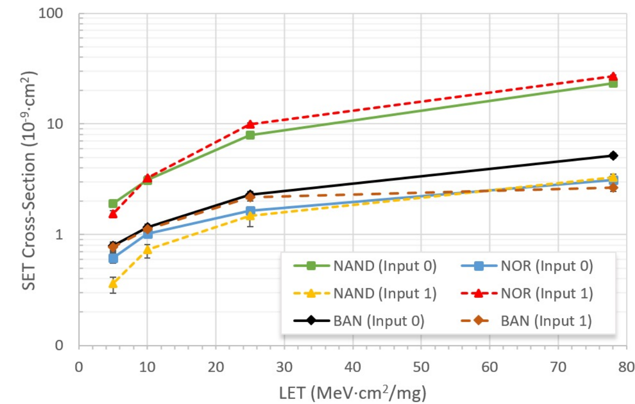
Complex-Gate MJV architectures



Low input dependence

No logic masking effect

Basic-Gate MJV architectures



High input dependence

Except for BAN voter

Logic masking effect within the MJV architecture of the standard-cell basic logic gates can increase the input dependence.

Hardness Improvement of RHBD techniques

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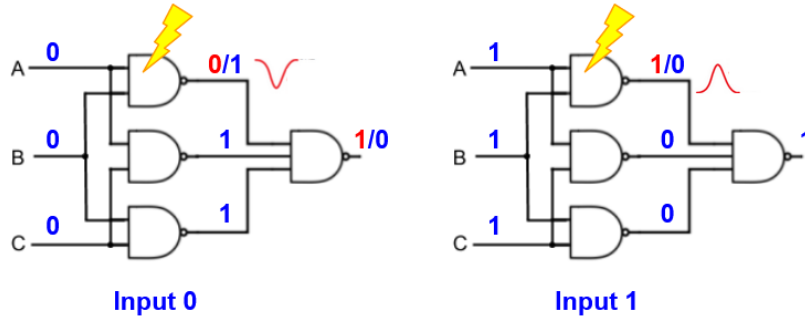
Y.Q. Aguiar et al. *Design exploration of majority voter architectures based on the signal probability for TMR strategy optimization in space applications*, ***Microelectronics Reliability***, 2020.

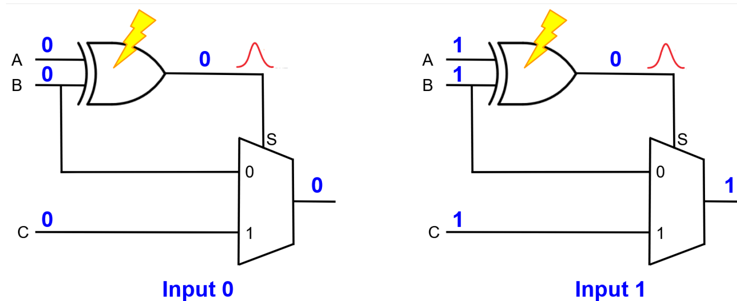
NAND-based MJV



The 3-input NAND gate masks any SET from the 2-input NAND gate for the **Input 1 configuration**.

Similar behaviour occurs in the **NOR-based voter**

BAN MJV



The **MUX gate** in the output **masks any SET** in the **XOR circuit**

Hardness Improvement of RHBD techniques

Y.Q. Aguiar et al. Design exploration of majority voter architectures based on the signal probability for TMR strategy optimization in space applications, ***Microelectronics Reliability****, 2020.*

Gate SET cross-section

$$\sigma_{\mathrm{G}} = \sum_{i=1}^{n} \sigma_i \times p(i)$$

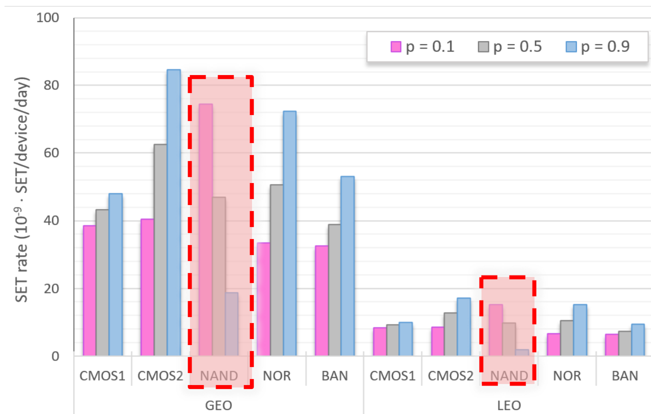
Only 2 input configurations in a fault-free scenario

MJV SET cross-section

$$\sigma_{\mathrm{MJV}} = p_{\mathrm{TMR}} \times (\sigma_1 - \sigma_0) + \sigma_0$$

p_{TMR} = *signal probability in the TMR insertion node*

σ_0 = *input*-0 scenario σ_1 = *input*-1 scenario



- **BAN/NOR** for **low** signal probability
- **NAND** for **high** signal probability

- Two trends:
  - SET rate **increases** with the increase of the signal probability
  - SET rate **decreases** with the increase of the signal probability
- NAND is the only to show a decrease with increase on the signal probability

Increase of masking effects

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Conclusions

- Mean value of the SET cross-section can be misleading when qualifying complex digital logic circuits for radiation environments.
- Hardening techniques can improve the reliability of circuit but their efficiency is LET dependent and **input dependent.**
- SET input dependence can be used to improve the hardening efficiency based on the input functional equivalence and signal probability estimation.
- A **novel circuit-level hardening technique** is proposed based on the *pin assignment*.
- The input dependence analysis can also be used to improve fault-tolerant techniques such as TMR methodology

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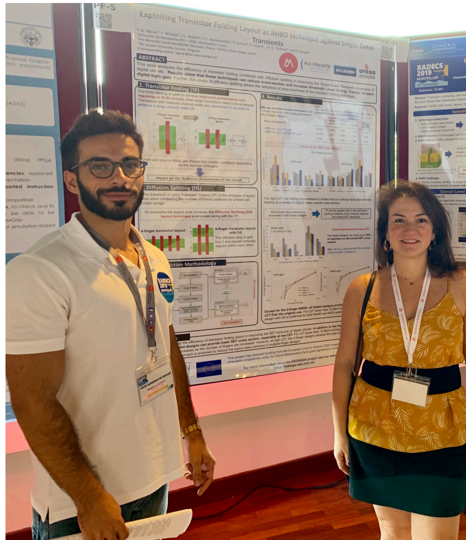
Thank you, RADSAGA!

Oral presentation at ESREF2018,
Aalborg, Denmark.



Poster session at RADECS2019,
Montpellier, France.

2018 Summer School,
Jyvaskyla, Finland.

Social Event at RADECS2019,
Montpellier, France.