Radiation hardening digital circuits against SET using design techniques

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Presentation outline

- Introduction
- Objectives
- Methodology
- Hardening techniques
  - Layout level
  - Circuit level
  - Hardness Improvement
- Conclusions
Introduction

Single-Event Effects: Radiation effects from a single particle strike at the device leading to nondestructive (soft errors) or destructive faults.

Single-Event Upset (SEU)

Single-Event Transient (SET)
Objectives

1. Propose a **general methodology based on a simulation chain** to predict the SEE susceptibility of digital circuits

2. Provide analysis of hardening techniques at design level and **propose guidelines to improve their efficiency**
Methodology

- Design Rules and SPICE models
- Radiation-Hardening-By-Design (RHBD) techniques

Specifications

Circuit Design

Layout Design

Physical Verification and Parasitic Extraction (DRC, LVS, PEX)

Extracted Netlist GDSII

MC-Oracle

- Particle Transport
- Charge Generation and Collection

Current Database

SEE Analyzer

- Electrical Simulations for transient current injections
- SEU/SET Cross-Section Calculation

SPICE Simulator

SEU/SET Cross-Section
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Hardening techniques

Implementation in different levels of abstraction:
Radiation Hardening by Design (RHBD) or by Process (RHBP)

Outside integrated circuit:
- Off-chip electronics
- Software

Inside integrated circuit:
- FPGA
  - System On Chip
    - Digital, Analog, Mixed-Signal
  - Electronic System level
- Circuit Architecture level
  - Digital IP
  - ASIC cell libraries
  - Analogue IP
    - Embedded memories
- Physical Layout level
- Manufacturing Process level

RHBD:
- Lower cost
- More flexibility
- Better performance

RHBP:
- High cost
- Low-grade performance
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Gate Sizing and Transistor Stacking

Selective Node Hardening:

To harden a circuit by selectively using logic gates that minimize the SET generation or propagation in the most vulnerable nodes of a complex VLSI design.

Gate Sizing:

increases circuit capacitance and drive current.

Transistor Stacking:

increases circuit capacitance and reduces leakage current.

Discrete process when using std cells!
Gate Sizing and Transistor Stacking

The cross-section was calculated for each input signal combination and the arithmetic mean for each particle LET is shown:

The efficiency of both techniques reduces as the particle LET increases.

For higher particle LET, the dominant effect on the circuit reliability is the charge collection efficiency enhanced by the larger transistors.
SET Input Dependence

Why they behave differently?

- Impact of the transistor network for each input scenario:
  - Different restoring currents
  - Different collection areas

Y.Q. Aguiar et al., Radiation Hardening Efficiency of Gate Sizing and Transistor Stacking based on Standard Cells, Microelectronics Reliability, 2019

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It is used to provide **layout regularity** in standard-cell layout designs.

A large transistor can be implemented by adopting smaller transistors in parallel.

A large transistor can be implemented by adopting smaller transistors in parallel.

(a) Different cell heights for non-folded designs
(b) Folded designs

Reduced collecting drain area while maintaining the same drive strength.

**Attractive to radiation hardening**
Increasing the number of fingers reduces the SET cross-section

The technique shows a great input dependence and LET dependence

- **Diffusion Splitting** (DS) technique
- Asymmetric designs
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Impact of Logical Synthesis

- The logic synthesis determines the main characteristics of a circuit design: **performance**, **power consumption**, **area usage** and its **reliability**.

- Each standard cell provided in a cell library shows different SEE sensitivity.

Assessment of the SET immunity of single cells and combinations of cells

Reliability-driven synthesis
Technology mapping: boolean functions are translated to logic gates (INV, NAND, NOR…)

\[ Y = \neg (A_1 \land (B_1 \lor B_2)) \]

- ~42% in the total layout area
- ~14% reduction of the total collection area

Complex-logic gates are widely used to **improve performance**, **reduce power consumption** and layout usage.

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Table 1

<table>
<thead>
<tr>
<th></th>
<th>Layout Area</th>
<th>Total Collection Area</th>
<th>P-hit Collection Area</th>
<th>N-hit Collection Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOR2</td>
<td>0.895</td>
<td>0.212</td>
<td>0.154</td>
<td>0.058</td>
</tr>
<tr>
<td>AND2</td>
<td>1.193</td>
<td>0.265</td>
<td>0.110</td>
<td>0.095</td>
</tr>
<tr>
<td>AOI21</td>
<td>1.193</td>
<td>0.359</td>
<td>0.243</td>
<td>0.116</td>
</tr>
<tr>
<td>AND + NOR</td>
<td>2.088</td>
<td>0.418</td>
<td>0.265</td>
<td>0.153</td>
</tr>
</tbody>
</table>

Improved radiation robustness?
Technology mapping can benefit from these analysis to generate an SET-aware gate netlist.

The complex-logic gate eliminates the Logic Masking Effect!

Any SET at the AND gate is masked by the NOR gate.
The SET characterization of logic gates presents an **input dependence** due to the different interplay relation of sensitive collecting areas and restoring current.

(0, 1) and (1, 0) are the **interchangeable input combinations**.

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**Table 5.4: Signal Probability Estimation for the INV, NAND, NOR and XOR gates**

<table>
<thead>
<tr>
<th>Cells</th>
<th>Input Signals</th>
<th>Output Signal Probability $^1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV</td>
<td>1: a</td>
<td>$P_{INV} = 1 - p_A$</td>
</tr>
<tr>
<td>NAND</td>
<td>2: a, b</td>
<td>$P_{NAND} = 1 - (p_A \times p_B)$</td>
</tr>
<tr>
<td>NOR</td>
<td>2: a, b</td>
<td>$P_{NOR} = (1 - p_A) \times (1 - p_B)$</td>
</tr>
<tr>
<td>XOR</td>
<td>2: a, b</td>
<td>$P_{XOR} = p_A \times (1 - p_B) + p_B \times (1 - p_A)$</td>
</tr>
</tbody>
</table>

$^1$ Signal probability is the probability of the signal to be at logic value 1.
Not considering the input dependence can lead to the underestimation of the circuit sensitivity.

For lower SET rate, the **lowest signal probability** should be assigned to the input pin:
- A for NOR and XOR gate
- B for NAND gate

Pin assignment can reduce the SET rate and provide an application-specific hardening without any increase in area.
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**Triple-Modular Redundancy (TMR):** critical component or electronic circuit is triplicated and their outputs are connected to a majority voter (MJV) architecture.

**BUT...**

**Faults in the MJV cannot be masked**

Signal probability of the TMR node can reduce the sensitivity of the MJV architecture based on its input dependence.
Hardness Improvement of RHBD techniques

Five majority voter architectures exploring complex-logic design and basic logic gates:

Complex-Gate MJV

Basic-Gate MJV

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Hardness Improvement of RHBD techniques

Complex-Gate MJV architectures

- Low input dependence
- No logic masking effect

Basic-Gate MJV architectures

- High input dependence
- Except for BAN voter

Logic masking effect within the MJV architecture of the standard-cell basic logic gates can increase the input dependence.


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The 3-input NAND gate masks any SET from the 2-input NAND gate for the **Input 1 configuration**.

Similar behaviour occurs in the **NOR-based voter**.

The **MUX gate** in the output masks any SET in the **XOR circuit**.
Hardness Improvement of RHBD techniques

Two trends:
- SET rate increases with the increase of the signal probability
- SET rate decreases with the increase of the signal probability

NAND is the only to show a decrease with increase on the signal probability

BAN/NOR for low signal probability
NAND for high signal probability

Increase of masking effects
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Conclusions

- Mean value of the SET cross-section can be misleading when qualifying complex digital logic circuits for radiation environments.

- Hardening techniques can improve the reliability of circuit but their efficiency is LET dependent and input dependent.

- SET input dependence can be used to improve the hardening efficiency based on the input functional equivalence and signal probability estimation.

- A novel circuit-level hardening technique is proposed based on the pin assignment.

- The input dependence analysis can also be used to improve fault-tolerant techniques such as TMR methodology.
Thank you, RADSAGA!

Oral presentation at ESREF2018, Aalborg, Denmark.

Poster session at RADECS2019, Montpellier, France.

2018 Summer School, Jyvaskyla, Finland.

Social Event at RADECS2019, Montpellier, France.