RADSAGA

Layout Effects on CMOS Photosensitive Devices

17-19 May, 2021
RADSAGA Final Conference and Industrial event

Rico Jossel Maestro, RADSAGA ESR 11, Work Package #2

RADiation and Reliability Challenges for Electronics used in Space, Aviation, Ground and Accelerators (RADSAGA) is a project funded by the European Commission under the Horizon2020 Framework Program under the Grant Agreement 721624. RADSAGA began in Mars 2017 and will run for 5 years.

Presentation outline

- Introduction
- Test Chip
- Initial Measurement Results
- Conclusion and Future Work

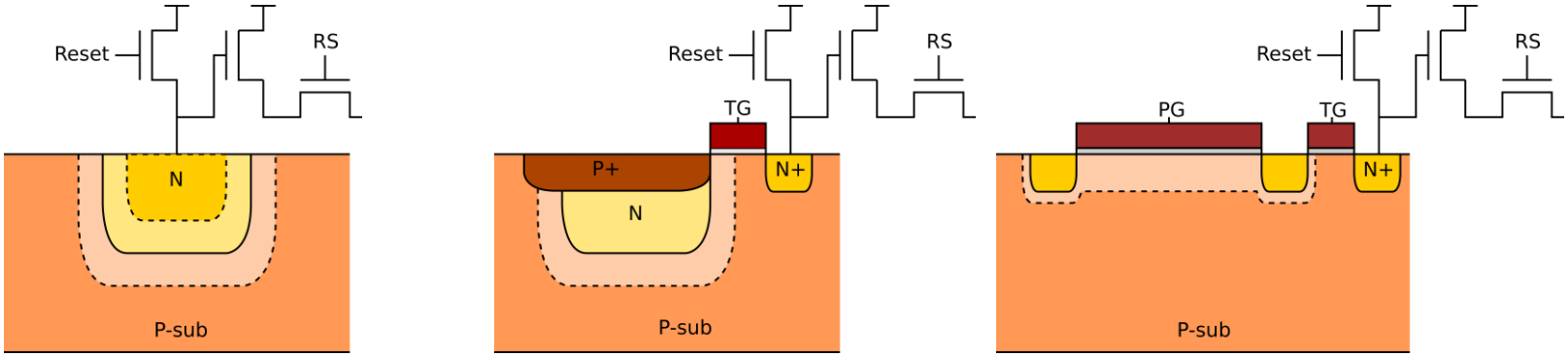
Presentation outline

- **Introduction**
- Test Chip
- Initial Measurement Results
- Conclusion and Future Work

CMOS Image Sensors

- Each block inherently adds error
- Effects of radiation are not always the same
- Approach to reduce radiation effects are also different

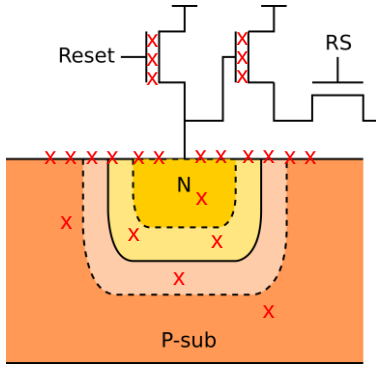
Pixel Structures in CMOS Process



- Photosensitive device for charge collection
- Transistors for operation and control

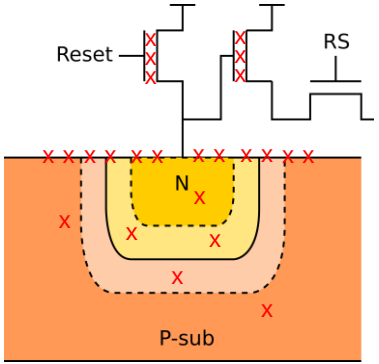
Radiation Effects in Pixels

- Total Ionizing Dose
  - Increase in dark current
  - Change in transistor threshold voltage
  - Transistor leakage paths
- Displacement Damage
  - Increase in dark current
  - Decrease in quantum efficiency
- Single-Event Effects
  - SELs



Radiation-Hardening the Pixel

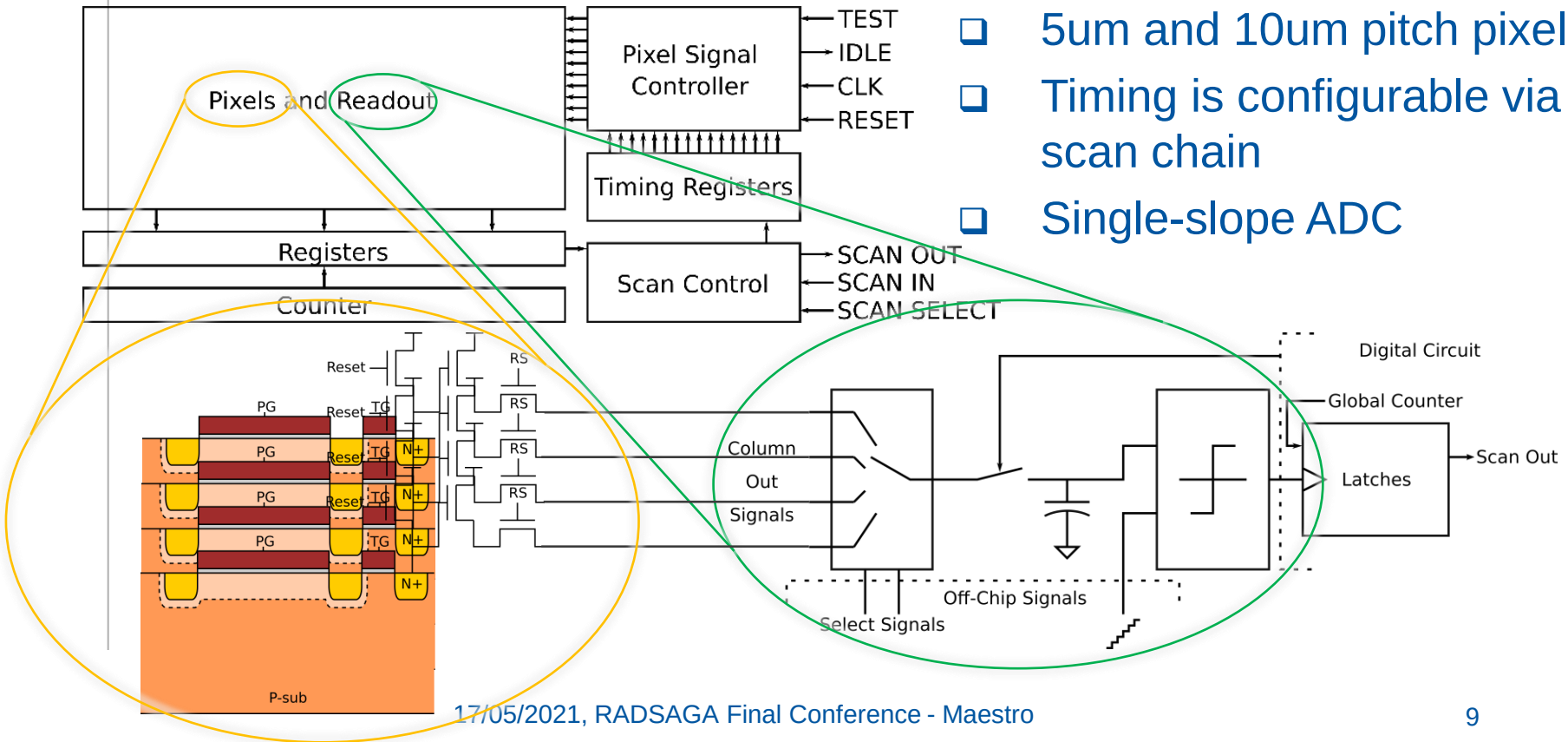
- Additional layers to minimize exposure of depletion region to interface states
- Use of enclosed-layout transistors
- Use of photogates for the ability to compensate



Presentation outline

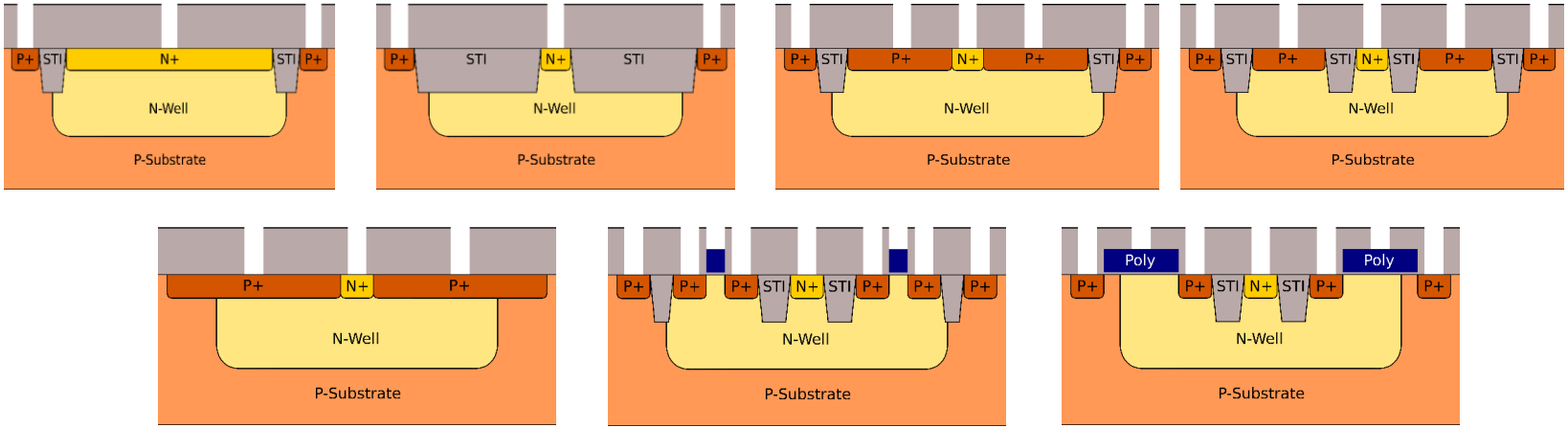
- Introduction
- **Test Chip**
- Initial Measurement Results
- Conclusion and Future

General System Structure



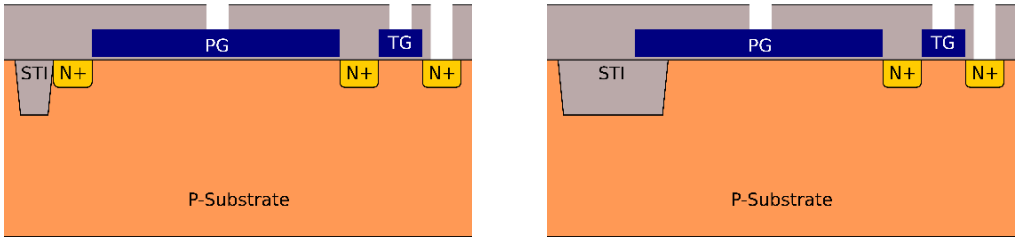
- 5um and 10um pitch pixels
- Timing is configurable via scan chain
- Single-slope ADC

Photodiode Layout



- Conventional, partially-pinned, and gated photodiodes are included
- Placements and sizes of STI are changed
- DRC violations are waived

Photogate Layout



- Other terminal of the photogate is floating
- Investigate effect of floating node to lag
- Photogates with different threshold voltages are included
- Not ELT

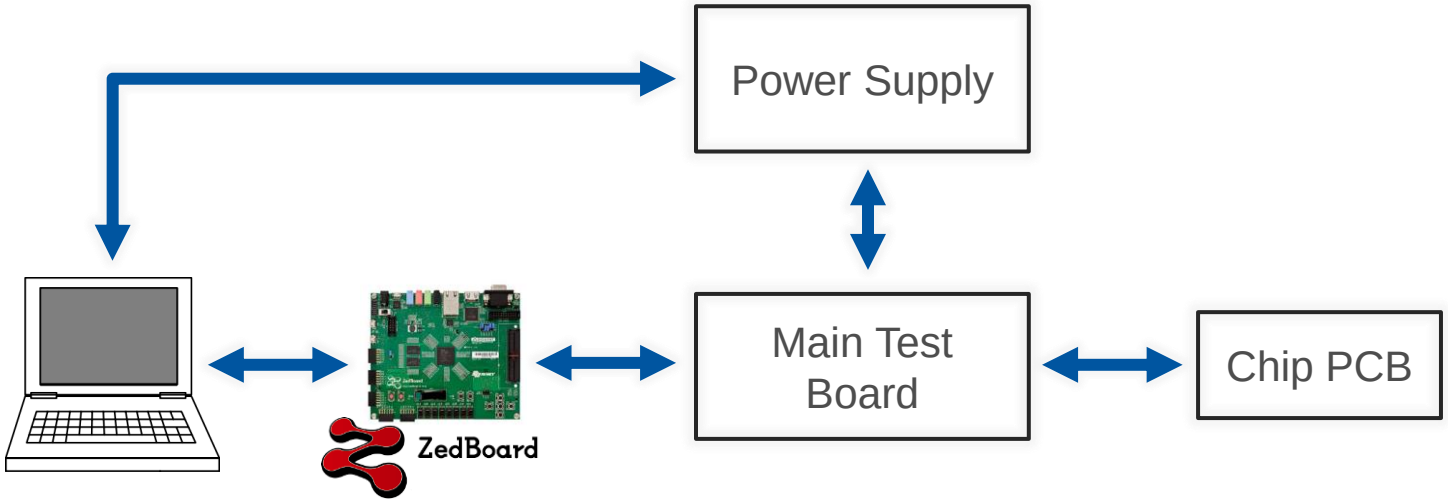
For Other Analog Circuitry…

- Transistors in pixel are enclosed layout transistor
- For other analog blocks like the column read, S/H, dynamic comparator
  - ELT are also used
  - Guard rings are placed in each group of transistors to minimize possibility of latch-up

Presentation outline

- Introduction
- Test Chip
- **Initial Measurement Results**
- Conclusion and Future Work

Test Setup



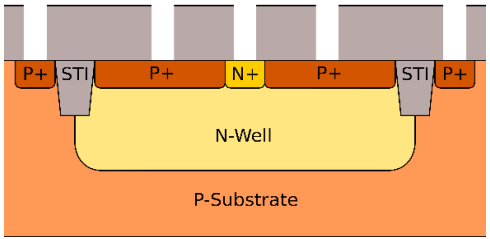
- FPGA system and software were developed
- Chip PCB is put inside a box and covered with black cloth to ensure that there will be no light

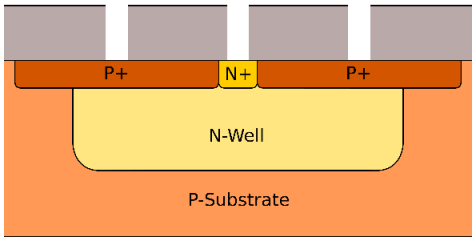
Tests and Characterizations

- Electrical and functional tests
  - Determine if blocks were working as intended
- Characterization
  - Fixed pattern noise
  - Temporal noise
  - Dark current levels

Electrical and Functional Tests

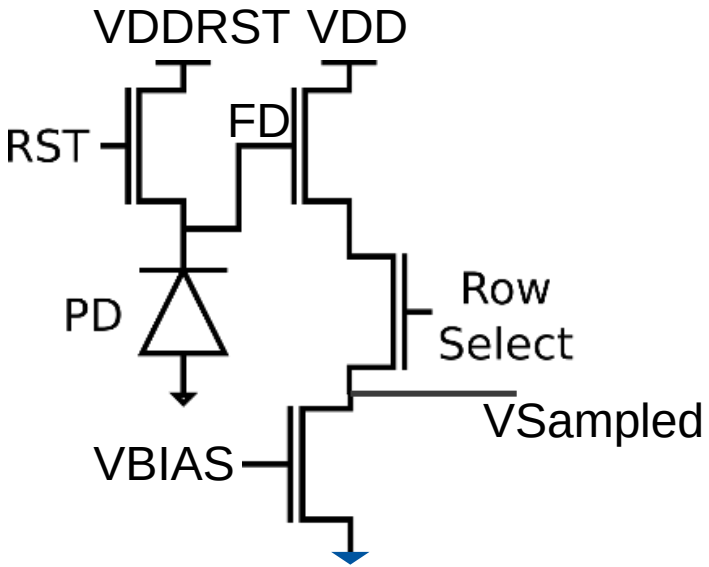
- All blocks are working
- Some pixel types are not working:
  - N+/P+ short





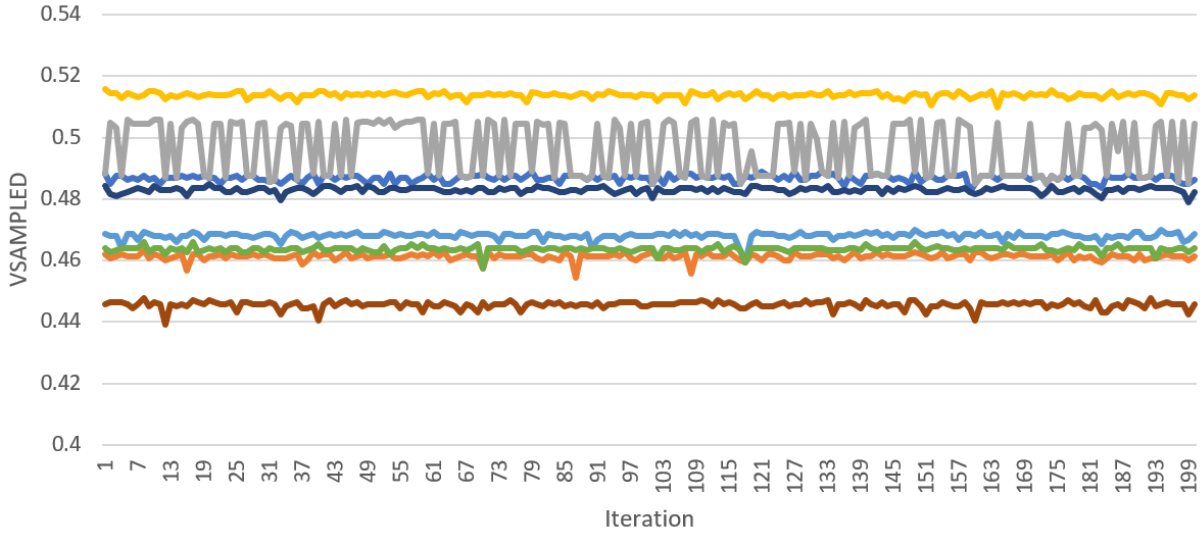
Fixed Pattern and Temporal Noise Characterization

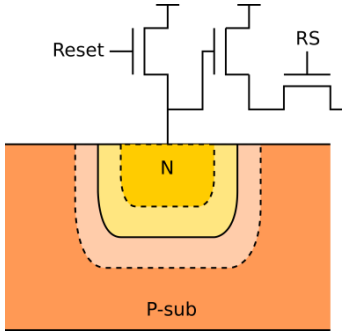
- VDDRST is set below VDD – $V_{th,RST}$ to make sure V_{FD} = VDDRST
- For temporal noise, pixel values are sampled 200 times
- For other tests, pixel values are sampled at least 10 times then the results are averaged



Temporal Noise

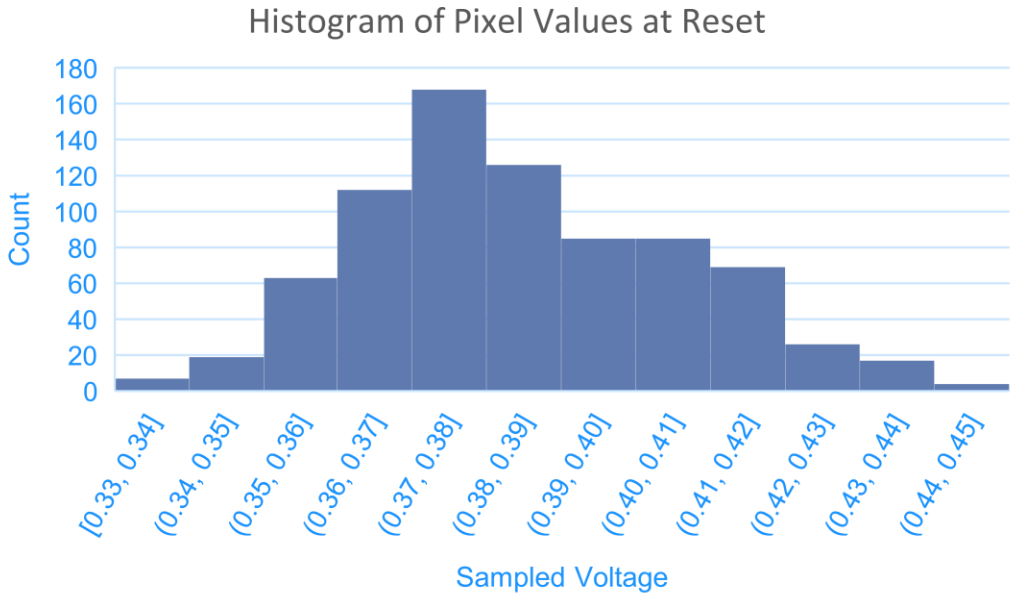
- Due to charges that are trapped and released after some time
- Heavily pixel-dependent





Fixed Pattern Noise

- Fixed pattern variation include variations in the path to the output
- Can easily be removed in software



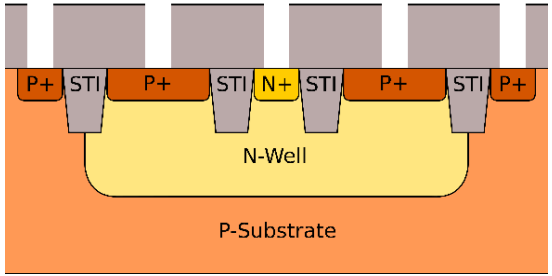
Ideal = 0.3946V
Mean = 0.3847V
StdDev = 0.0211V

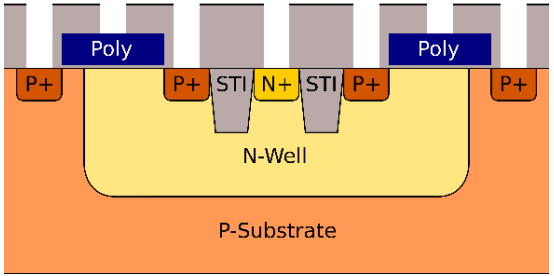
Dark Current Levels: Photodiode

- Output is sampled after reset
- After some time, output is sampled again
- Dark current is then computed from the difference in voltage, the time difference and the capacitance

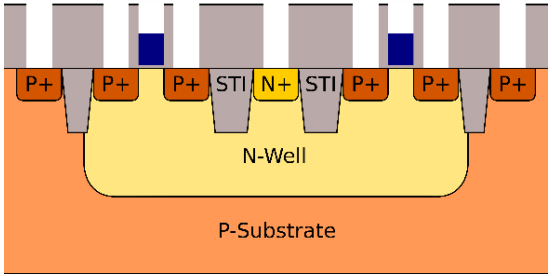
Dark Current Levels: Photodiode

- Lower dark current were observed for these layouts



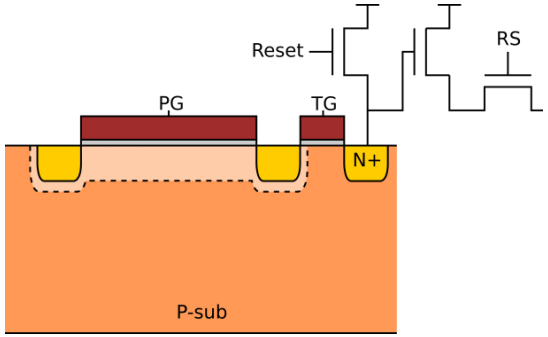


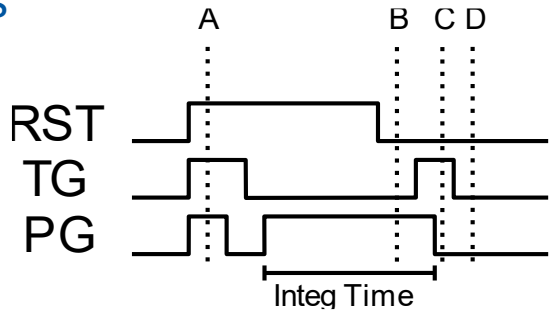
- Lower dark current when poly layer in this layout is biased with lower voltages



Dark Current Levels: Photogate

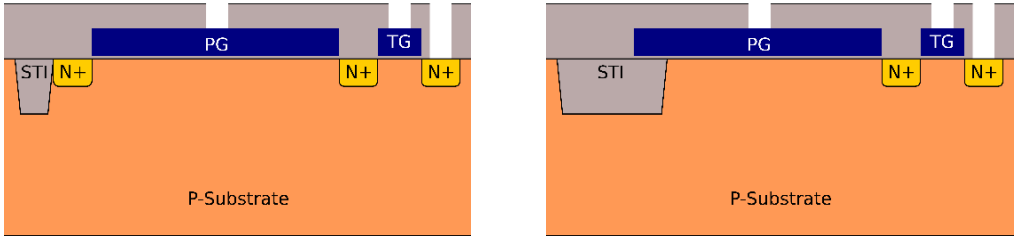
- Point A is needed to remove any charges on the left terminal of PG
- Point B is reset value of the FD
- Point D is where the final value of the pixel is sampled
- Integration time is increased





Dark Current Levels: Photogate

- The lower the threshold voltage, the higher the dark current
- Increasing the gate voltage increases the dark current
- Lower dark current for photogate without the left terminal



Presentation outline

- Introduction
- Test Chip
- Initial Measurement Results
- **Conclusion and Future Work**

Conclusions and Future Work

- From initial tests, dark current levels indeed depend on layout of the pixels for both photodiodes and photogates
- Gate structures might offer another degree of control for dark current
- Radiation tests will be done to characterize how the dark current will evolve with increasing dose
- Optical tests will also be done after thinning the Silicon bulk

RADSAGA

Thank you for your attention!
Questions?

RADiation and Reliability Challenges for Electronics used in Space, Aviation, Ground and Accelerators (RADSAGA) is a project funded by the European Commission under the Horizon2020 Framework Program under the Grant Agreement 721624.
RADSAGA began in Mars 2017 and will run for 5 years.