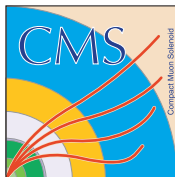




National
Taiwan
University



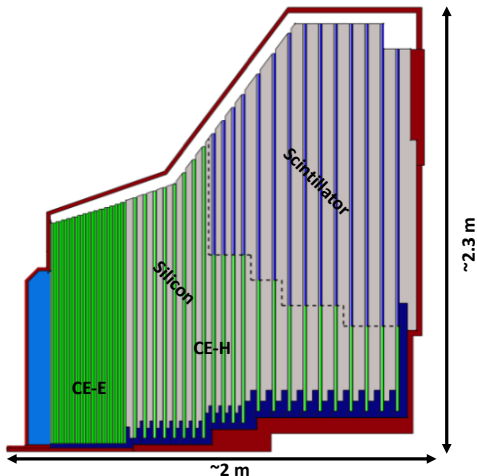
Trenz-based test systems in CMS HGCAL

SoC Interest Group Meeting

Arnaud Steen, on behalf of the HGCAL

February 16, 2021

CMS HGCAL for phase 2

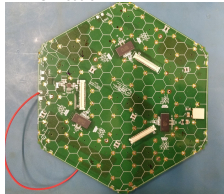


Electromagnetic calorimeter (CE-E): **Si**, Cu/CuW/Pb absorbers, 28 layers, $25.5 X_0$ & $\sim 1.7 \lambda$
Hadronic calorimeter (CE-H): **Si** & **scintillator**, steel absorbers, 22 layers, $\sim 9.5 \lambda$

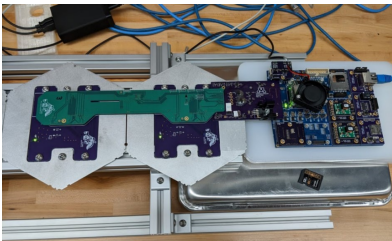
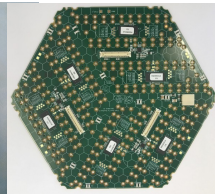
FE hardware to test in CMS HGICAL

- HGICAL needs test systems to test the quality of many individual components:
 - ▶ $\approx 100k$ HGCROCs (the readout chip)
 - ▶ $\approx 25k$ Si-Modules (and their hexaboard PCB) with 3 or 6 HGCROCs
 - ▶ $\approx 4k$ Tileboards
 - ▶ ECONs : ≈ 2 per module
 - ▶ Mother boards (engines and wagons)

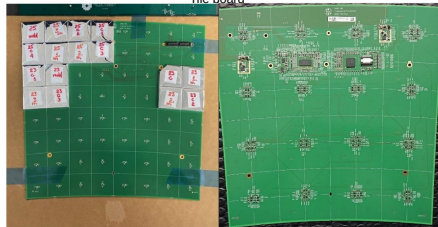
LD Si-module



HD Hexaboard



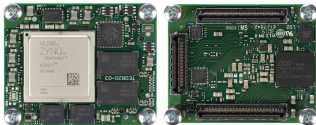
Tile board



Trenz-based test systems in CMS HGCAL

- Test systems based on Trenc module

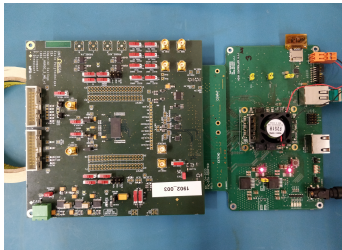
- ▶ Trenc module in HGCAL : TE0820



- ▶ Common architecture for single ROC, hexaboard and tileboard tester → same firmware IPs, same software

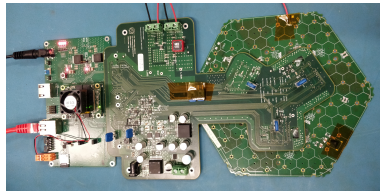
- Current test systems in HGCAL:

- ▶ Single ROC tester (tested ≈ 200 ROCs → will test ≈ 300 more in few weeks)

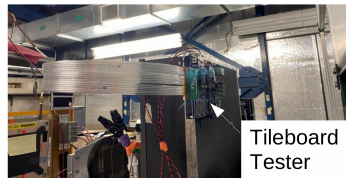


- Current test systems in HGCAL:

- ▶ Single Hexaboard test system (tested about 50 boards → 50 more in 2 months)

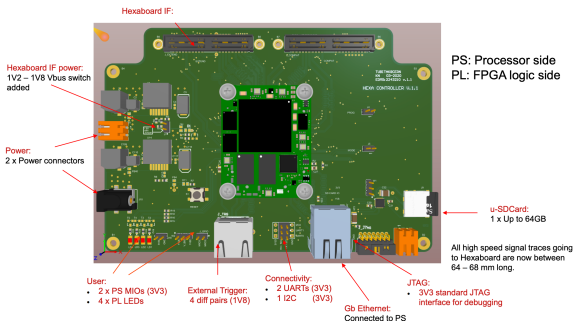


- ▶ TB tester (during a beam test at FNAL)



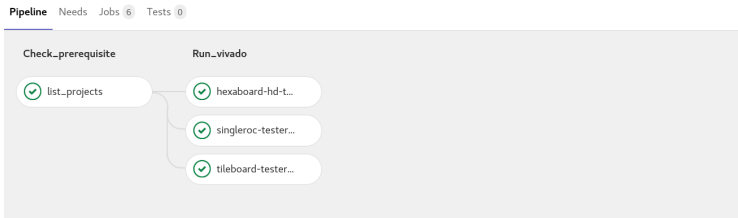
Our trenz based system

- TE0820 module in HGAL tester:
 - ▶ Run a centos 7 image → very convenient for SW development
 - ▶ Xilinx IPs:
 - ★ I2C for ROC configuration + ADC (ROC power consumption, DC levels) readout on the "trophy" board
 - ★ GPIO
 - ★ (CDMA testing)
 - ▶ Drivers: uio for all non-Xilinx IPs → AXI registers/FIFOs accessible in `/dev/uioX`
 - ▶ TE0820 has MAC address EEPROM. Value available to uboot and linux.
- The hexa-controller board:



Our trenz based system

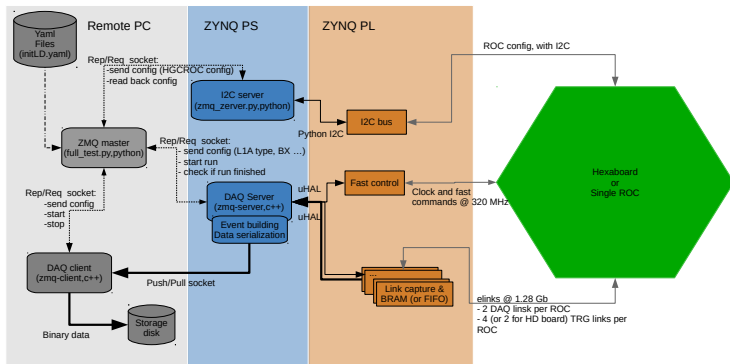
- Firmware .bit and device tree files prepared by gitlab CI/CD for our three designs.



- ▶ Vivado 2019.2 docker in dedicated runner
- ▶ Labels added to the device tree to map UIO devices, I2C buses, GPIO lines
- ▶ Firmware loaded using custom **Makefile**:
 - ★ creates .dtbo from .dtsi files
 - ★ loads the FW using the xilinx **fpgautil** tool : [link](#)
 - ★ [Link](#) to mylittledt.
- ▶ Firmware can be reloaded without rebooting:
 - ★ when changing the DUT
 - ★ very convenient for debugging
- ▶ Plan to add the .dtbo creation inside our gitlab CI process

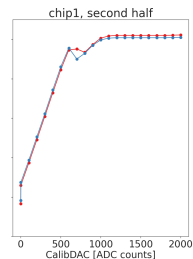
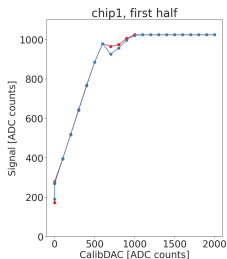
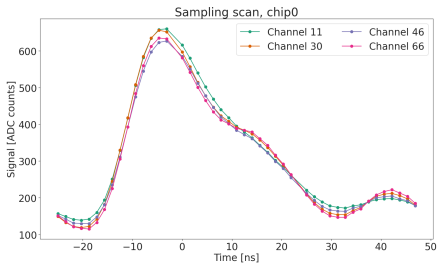
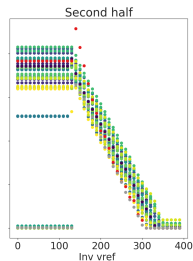
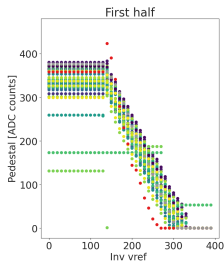
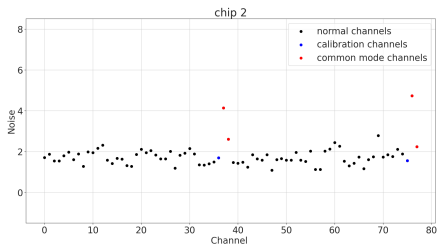
DAQ overview

- Using an extended uhal library to memory map the AXI registers and read the FIFOs : [Dan Gastler's presentation](#). We added:
 - Interrupt signal handler
 - "Non-incremental" block read (to read FIFOs)
- Synchronization of the software by using zmq library <https://zeromq.org/>



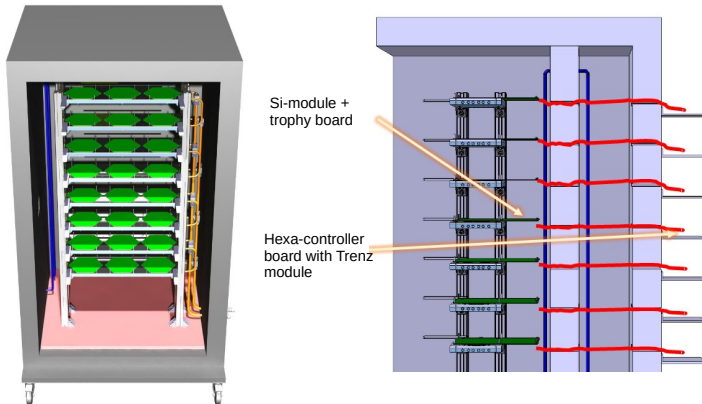
- No direct I2C for the tileboard:
 - A GBT-SCA is used to configure the ROCS
 - Interface between GBT-SCA and SW using the same "AXI-over-uio-over-uhal"

Test system output



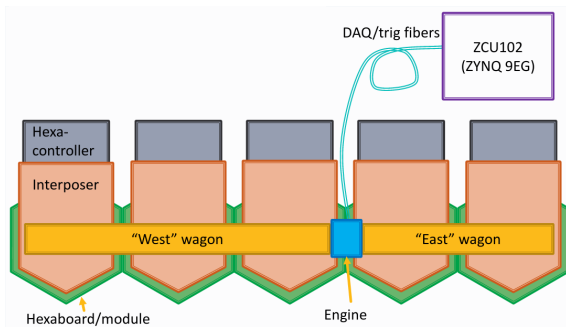
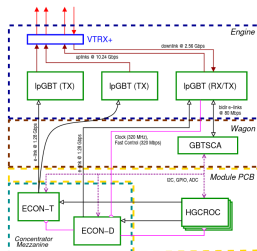
Future multi-module test system

- Si-modules will be tested inside a cold box ($\approx -30^{\circ}\text{C}$) after assembly



"V2" test system

- HGCAL communication chain : ROCs → ECONs → IpGBTs → BE
- "V2" test system : first system with full communication chain ("V2" ↔ 2nd version of the HGCROC):
 - ECONs not yet available (ECON-T design review was Feb 03)
 - ECONs emulated in the ZYNQ of HGCROC



Summary

- CMS-HGCAL test systems started to use test board with Trenz module about 1 year ago
 - ▶ Trenz based test systems used for several platforms (single ROC, hexaboards or Si-modules and tileboard/tilemodule).
 - ▶ All test systems use the same (or almost the same) firmware and software
- Test systems are now being distributed to Si-module and tile-module assembly centers (Germany, Taiwan, US).
- Knowledge on the Trenz is being useful for the "V2" test system:
 - ▶ Hexa-controller will be used as ECON chip emulators
 - ▶ FW and SW developed for the hexa-controller board and the tiler board testers will be recycled with the ZCU.
- Future multi-module tester plans to use the hexa-controller boards.
- Links to our gitlab repos (Access may need to be requested):
 - ▶ [firmware](#) repo.
 - ▶ [software](#) repo.

Back-Up