



SERENITY

Update on ZynqMP SoM for Serenity Boards

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Next revision ATCA hardware

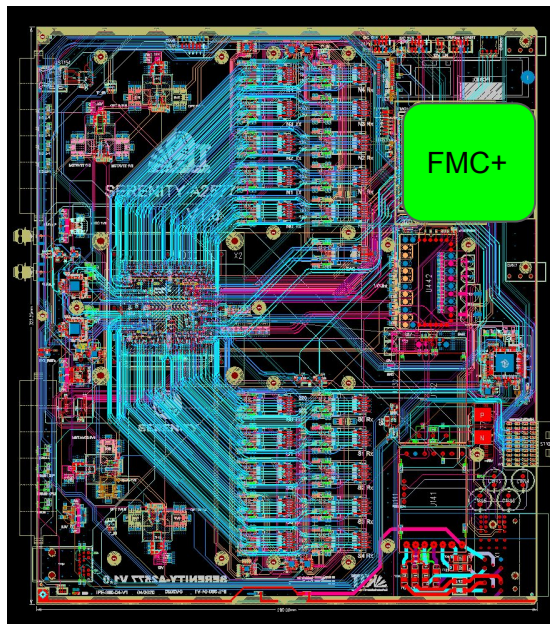


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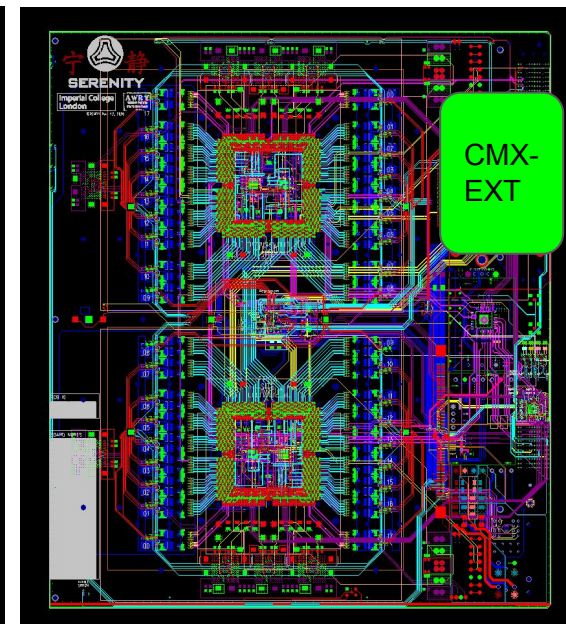
Common objectives for this prototype iteration

- Support for large A2577 footprint
 - VU9P & VU13P
- Support for 10 Gb/s TCDS
- **Support for Zynq & integrated IPMC**
 - Retaining option for COM-Express / dimm based IPMC where it exists.
- Production style design
 - Simplified
 - Designed for test & mass manufacture

Serenity-A1.0



Serenity-Z1.2



Custom ZynqMP SoM - Why?

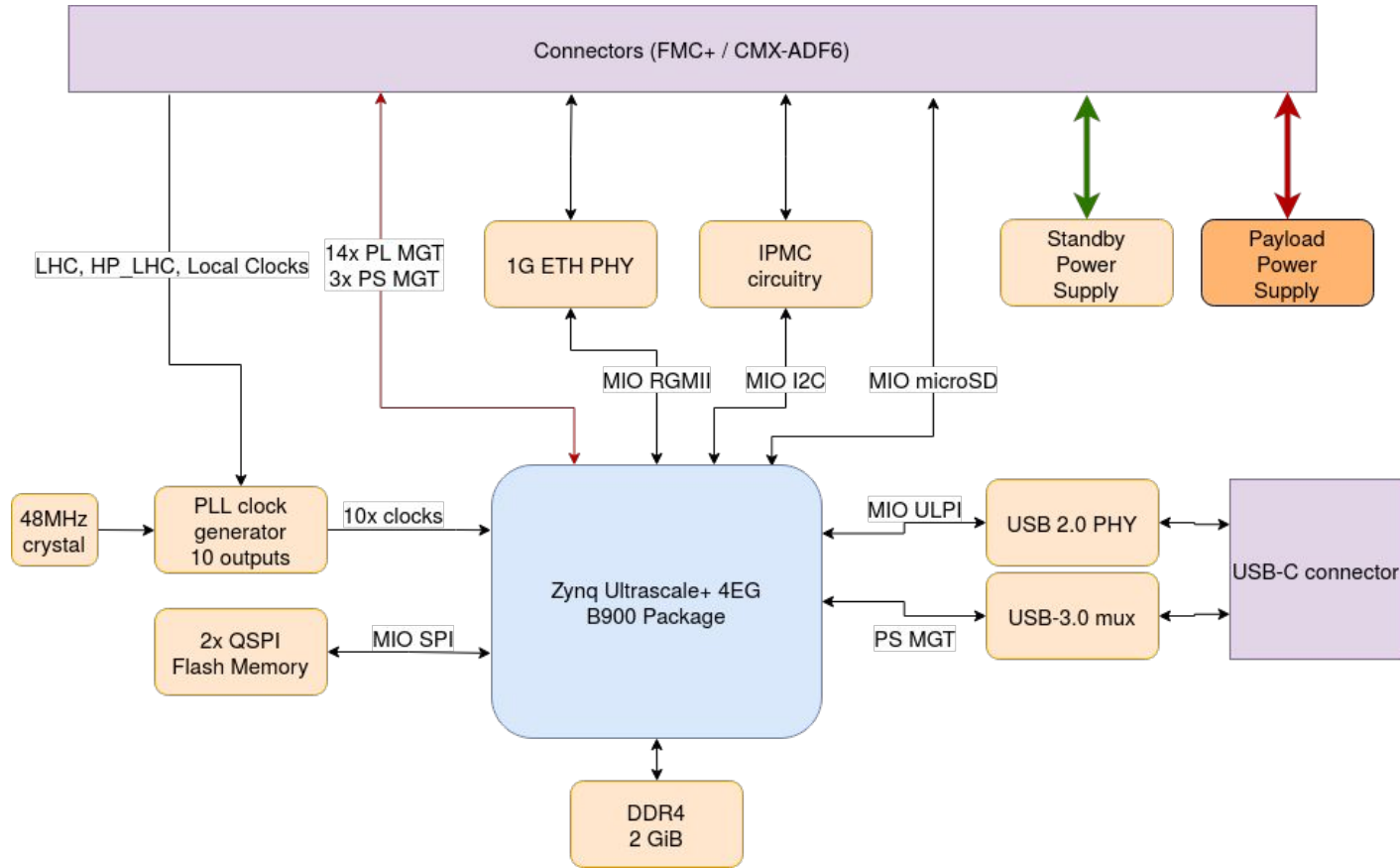
Technical requirements (Serenity specific)

- availability of high speed transceivers limited on commercial boards
 - ZU4EG with 16 lanes not available
- specific requirements (integration of IPMC into ZynqMP)
 - individual powering of the domains (LPD, FPD, PL)
 - IPMB circuitry
- compatibility with CMX form factor
 - flexible choice between x86 CMX boards and the ZynqMP SoM

Soft requirements

- full control of the design sources
- long term availability
- designed using KiCAD, an open source EDA software
- could evolve to a SoM (family) shared across multiple projects

Integrated ZynqMP SoM - Block Design

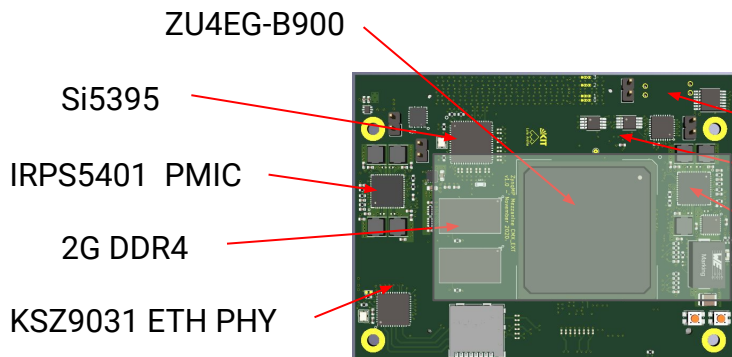


Integrated ZynqMP SoM - Layout



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EXT
8 PL MGTs
2 PS MGT

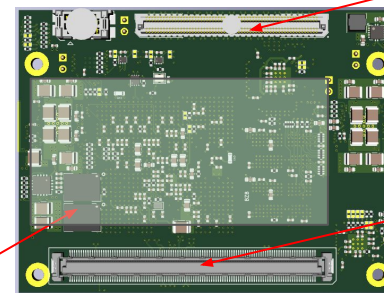


CMX-EXT module

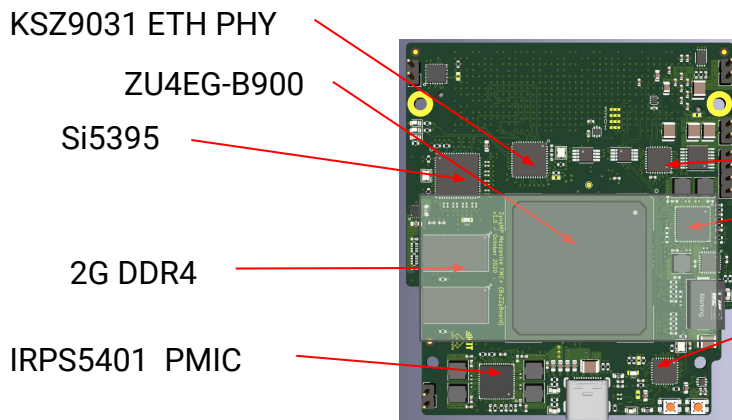
Integrated IPMC
functionality
I2C IPMC I/O
USB PHY

IRPS5401 PMIC

QSPI FLASH



CMX
6 PL MGTs
2 PS MGTs



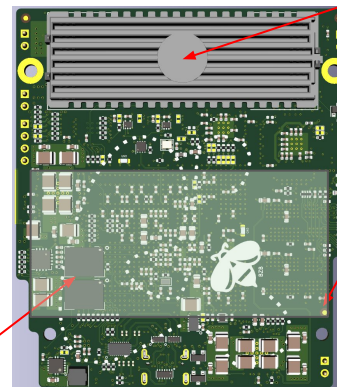
FMC+ module

Integrated IPMC
functionality
I2C IPMC I/O

IRPS5401 PMIC

USB PHY

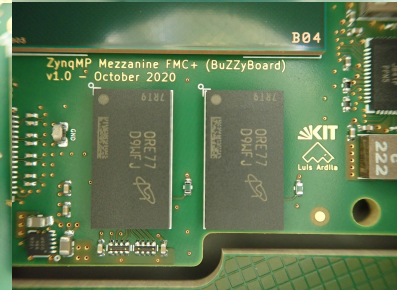
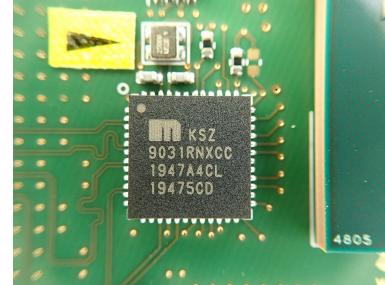
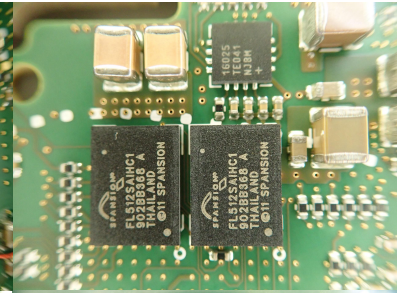
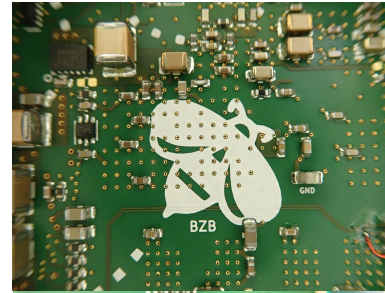
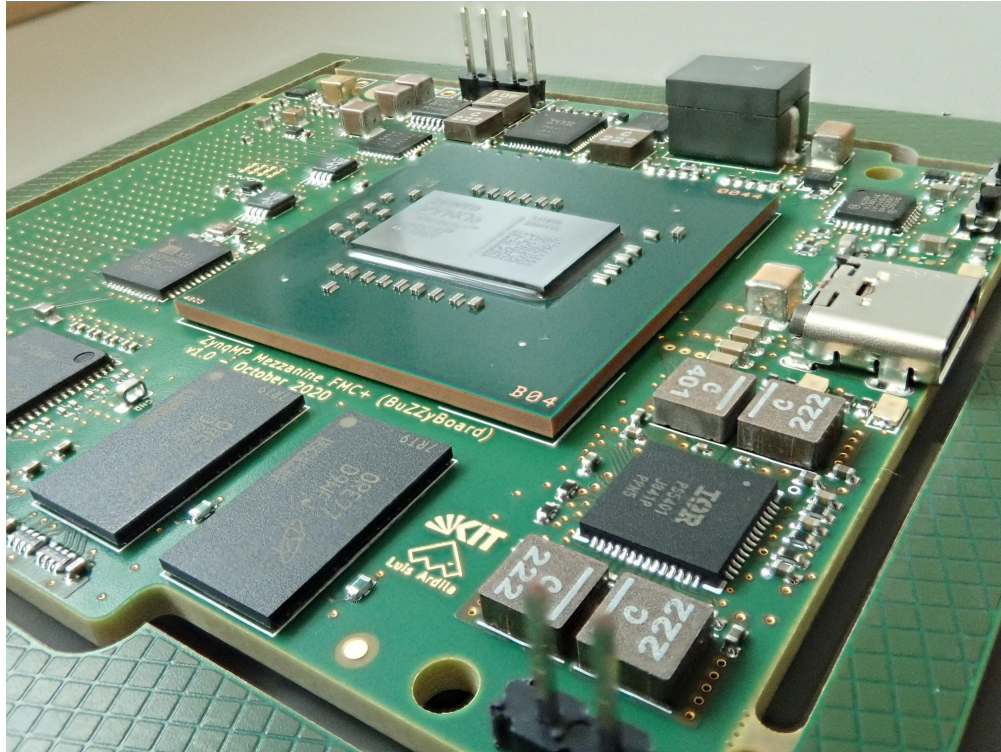
QSPI FLASH



FMC+
5 PL MGTs
3 PS MGTs

Highlighted
area is
common
between
them

Money shots





ZynqMP FMC+ Power Plan

+3V3_STBY @ 2.68A (7.43W) (67% of 11W)

12V @ 2 A

- VDDO+VDDA_Si5395 @ 0.433A
- IRPS5401MTRPBF @ 2.25A (70% eff)
 - 3) +2V5_STBY @ 0.060A
 - VPP_DDR4x2 @ 0.060A
 - 3) +1V2_STBY @ 1.235A
 - VCCO_PSDDR_504 @ 0.354A
 - VDD_DDR4x2 @ 0.660A
 - ETH_PHY @ 0.221A
 - 1) +0.85V_STBY @ 2.62A
 - VCCINT_IO @ 0.058A
 - VCCRAM @ 0.011A
 - VCC_PSINTFP @ 1.062A
 - VCC_PSINTLP @ 0.171A
 - VCC_PSINTFP_DDR @ 0.677A
 - PS_MGTRAVCC @ 0.641A
 - 2) +1V8_STBY @ 0.690A
 - VCCAUX @ 0.117A
 - VCCAUX_IO @ 0.041A
 - VCC_PSAUX @ 0.002A
 - VCCO @ 0.053A
 - VCC_PSDDR_PLL @ 0.026A
 - VCC_PSADC @ 0.011A
 - VCCADC @ 0.008A
 - PS_MGTRAVTT @ 0.1A
 - VDD_Si5395 @ 0.270A
 - VCC_QSPI @ 0.062A
 - 2) +1V2_PS_PLL @ 0.026A
 - VCC_PS_PLL @ 0.026A

- IRPS5401MTRPBF
 - 1) +0.85_PL_VCCINT
 - VCCINT @ 6A
 - 4) +5V_USB_VBUS
 - 3) +1V2_PL_MGTAVTT
 - V_MGTAVTT_R @ 1.892A
 - 2) +0.9V_PL_MGTAVCC
 - V_MGTAVCC @ 1.339A
 - 3) +1V8_PL_MGTAVCCAUX
 - V_MGTAVCCAUX_R @ 0.049A

Measured power consumption:

Case1: 3V3_STBY ON, DC-DC unconfigured

3V3_STBY = 208mA

Case2: DC-DC configured

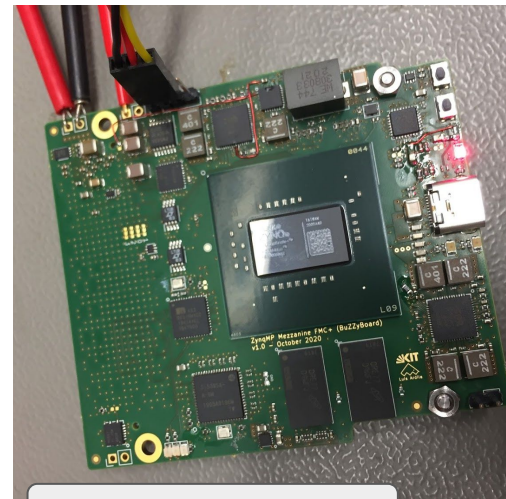
3V3_STBY = 743 mA (2.45W)

12V = 72.8 mA

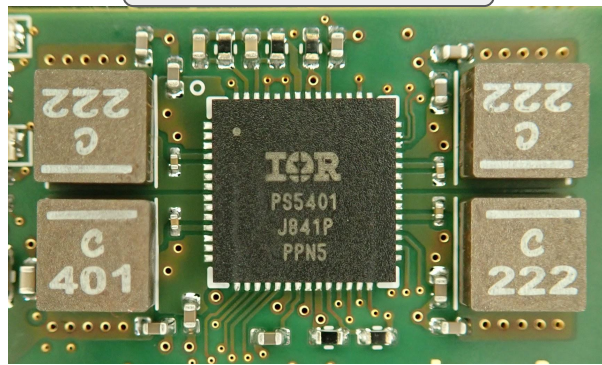
Case3: DC-DC configured Plugged-In

3V3_STBY = 743 mA (2.45W)

48V = 127mA (6.1W)

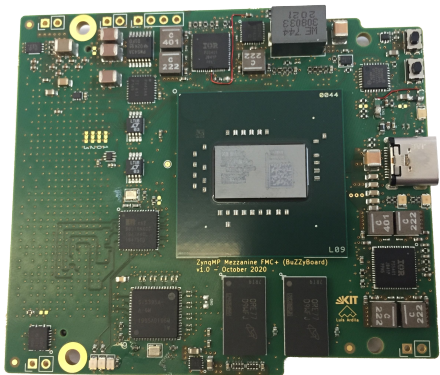
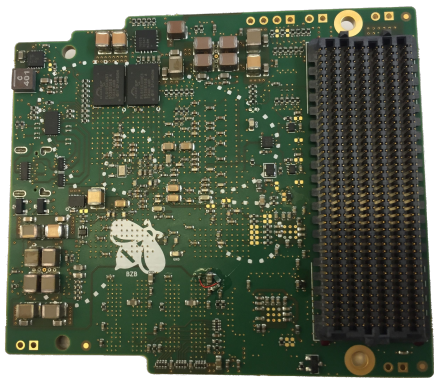


13x21mm layout area



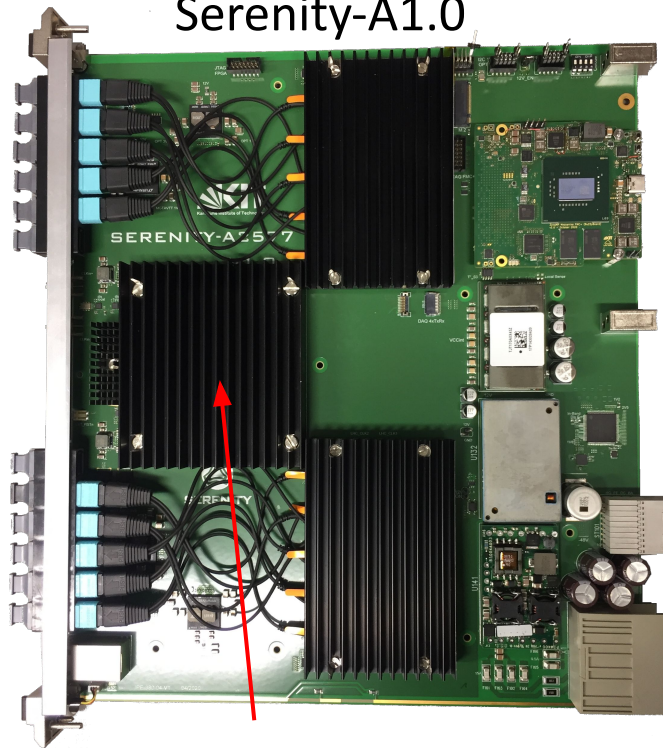


Current status



- Three Mezzanines fabricated
- Programmable power supplies configured successfully
- One board tested all the way down to "Hello-World" from R5 and from A53 using only STBY power 2.67 W
- Some minor bugs found, but DDR4 layout works!
- boot from SDcard and JTAG works.

Serenity-A1.0



VU9P



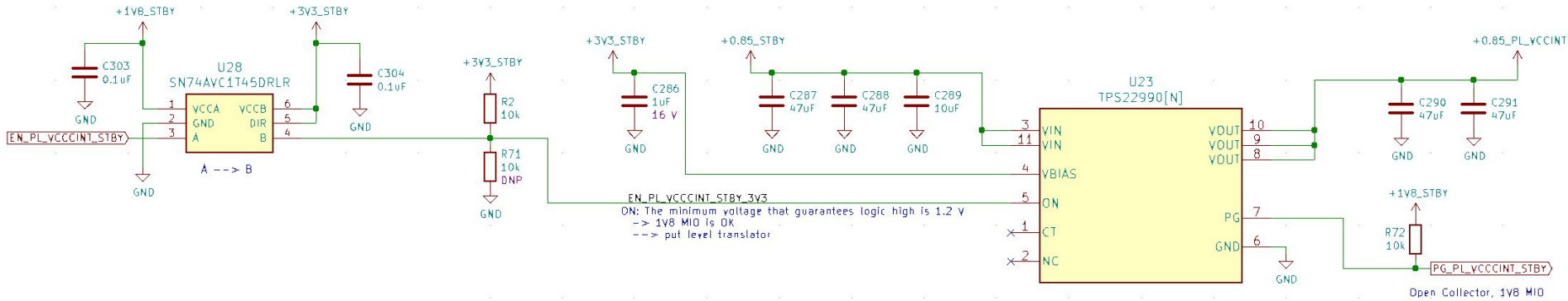
Summary and Outlook

- first revision of the module with minor bugs but operational
- in the following days, all interfaces of the SoM need to be tested and validated
- after fixing PCB bugs both versions will be fabricated in same panel
- integrated OpenIPMC firmware + CentOS linux currently getting migrated from other ZynqMP based platform

In case you are interested in the design sources, please contact us.



ZynqMP FMC+ PL_VCCINT Power Rail



The PL_VCCINT 0.85V rail can be supplied from the 3.3V_Standby power by using the power switch TPS2290N (U23)

Quiescent current for PL_VCCINT is ~700mA for 4EG, 5EG and ~ 1200mA for 7EG, currently with 4EG total current in 0.85V is 2A (4A possible)

Heatsinks

