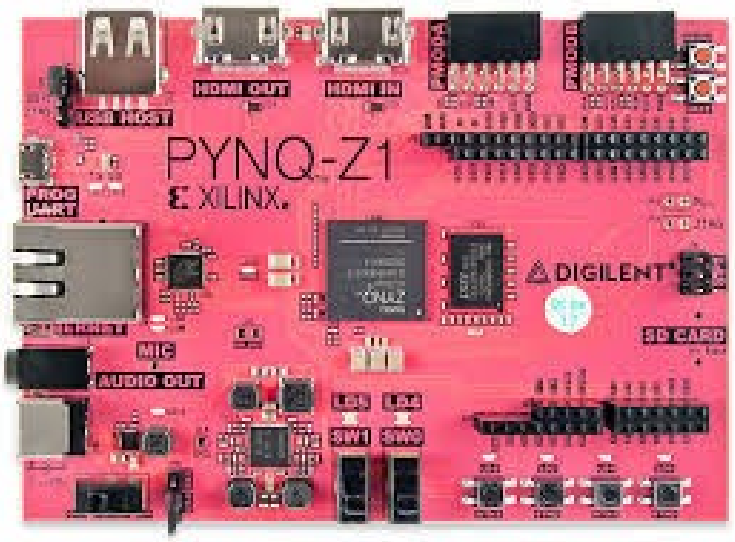
hls4mlxPYNQ demo

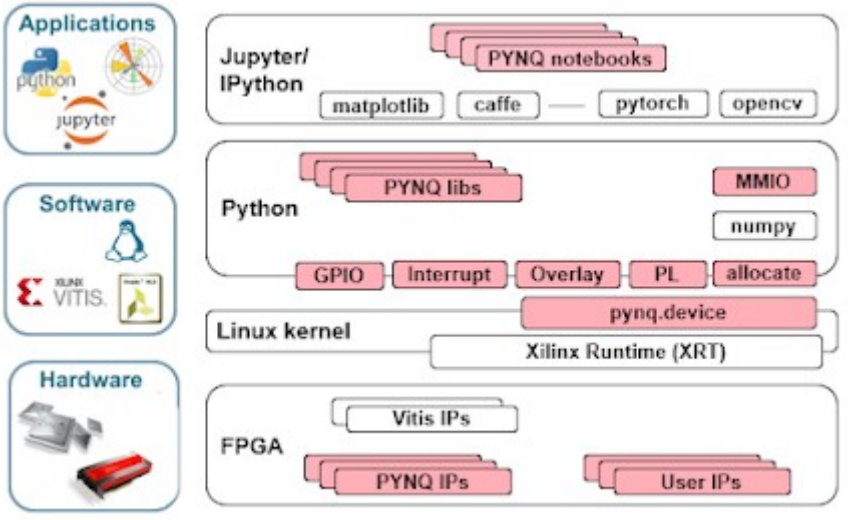
Intro

- We don’t do much “hands on” hardware work in this group
- Normally that’s fine, but from time to time we need to run these things on real FPGAs
- We have the PYNQ boards: they are not very powerful devices but are easy to use and good learning tools
  - But they may also have a useful role for low power embedded applications: can easily stream peripherals (e.g. cameras, microphones, other sensors) into FPGA



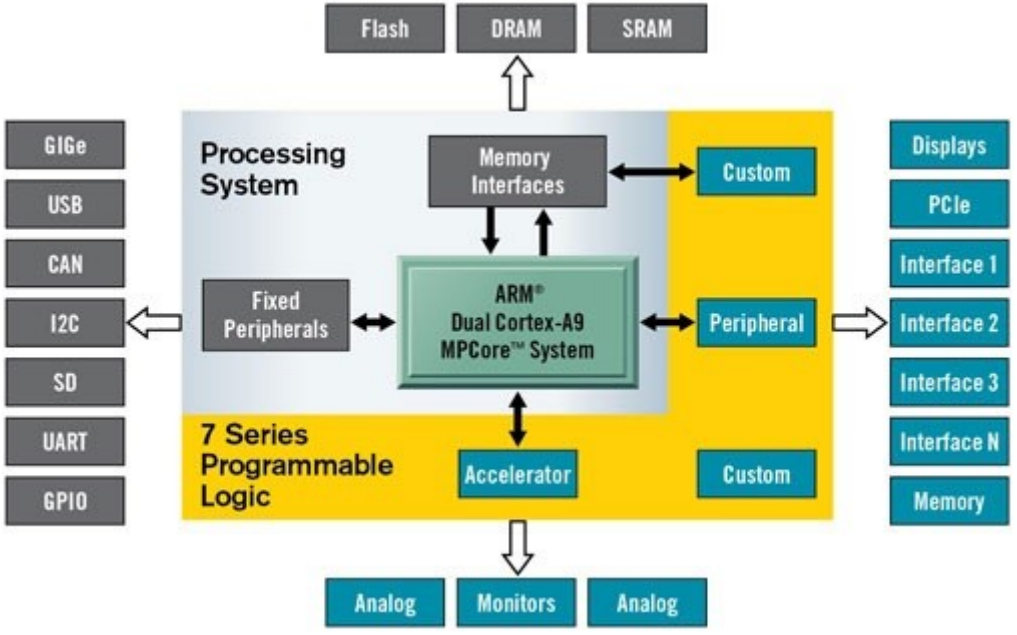
PYNQ

- The ‘PYNQ ecosystem’ covers hardware, drivers and Python APIs to work with Xilinx hardware
- We have the PYNQ-Z2 board
- We’ll be using the Python API (through notebooks) that should also adapt to other hardware e.g. Alveo



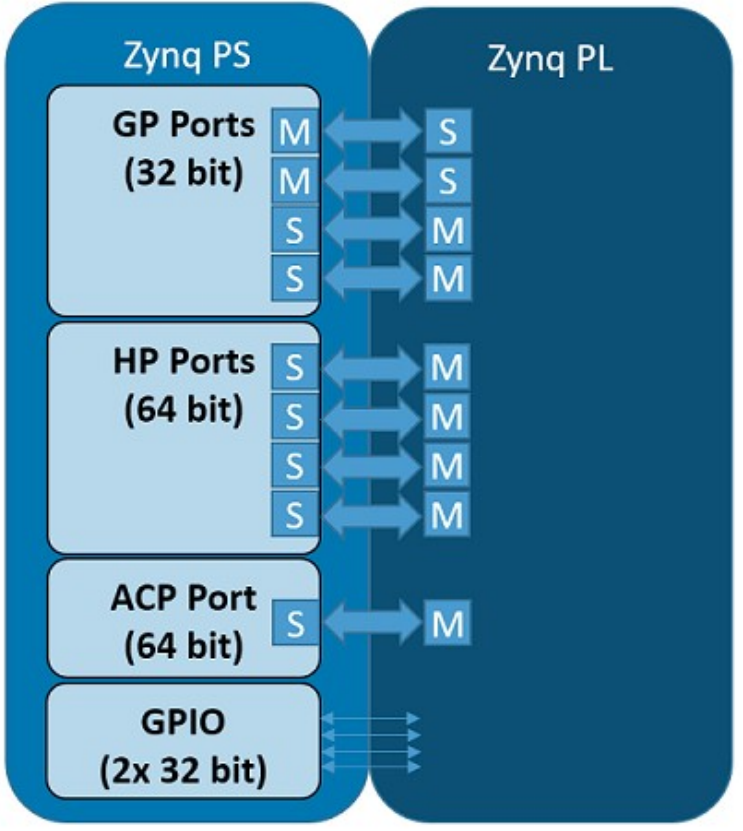
ZYNQ

- The PYNQ board has a ZYNQ SoC as its processor
- It’s a combination of ARM CPU (Processing System = PS) and FPGA (Programmable Logic = PL)
- We’ll run Python notebooks on the PS, and a NN on the PL
- We have to add some extra code to communicate between them



Interfaces

- The PYNQ (Actually Zynq) hardware has multiple interface possibilities
- They all use AXI as the protocol
- Generally… some memory mapping takes place so that we can read/write to memory on the PS, and it will be ‘mapped’ to memory on the PL
- We will use the lowest performance option – but the only one I could get working so far :)



Wrapper / Pynq backend

- The usual hls4ml flow gives us an *IP core*
- We need to provide some extra code to communicate between this IP core and the outside world
- This will define the type of interface, and maybe do some optimizations
  - Batching/bursting/buffering, type casting
- We have a WIP ‘Pynq Backend’ that adds the most simple wrapper
  - https://github.com/thesps/hls4ml/tree/pynq

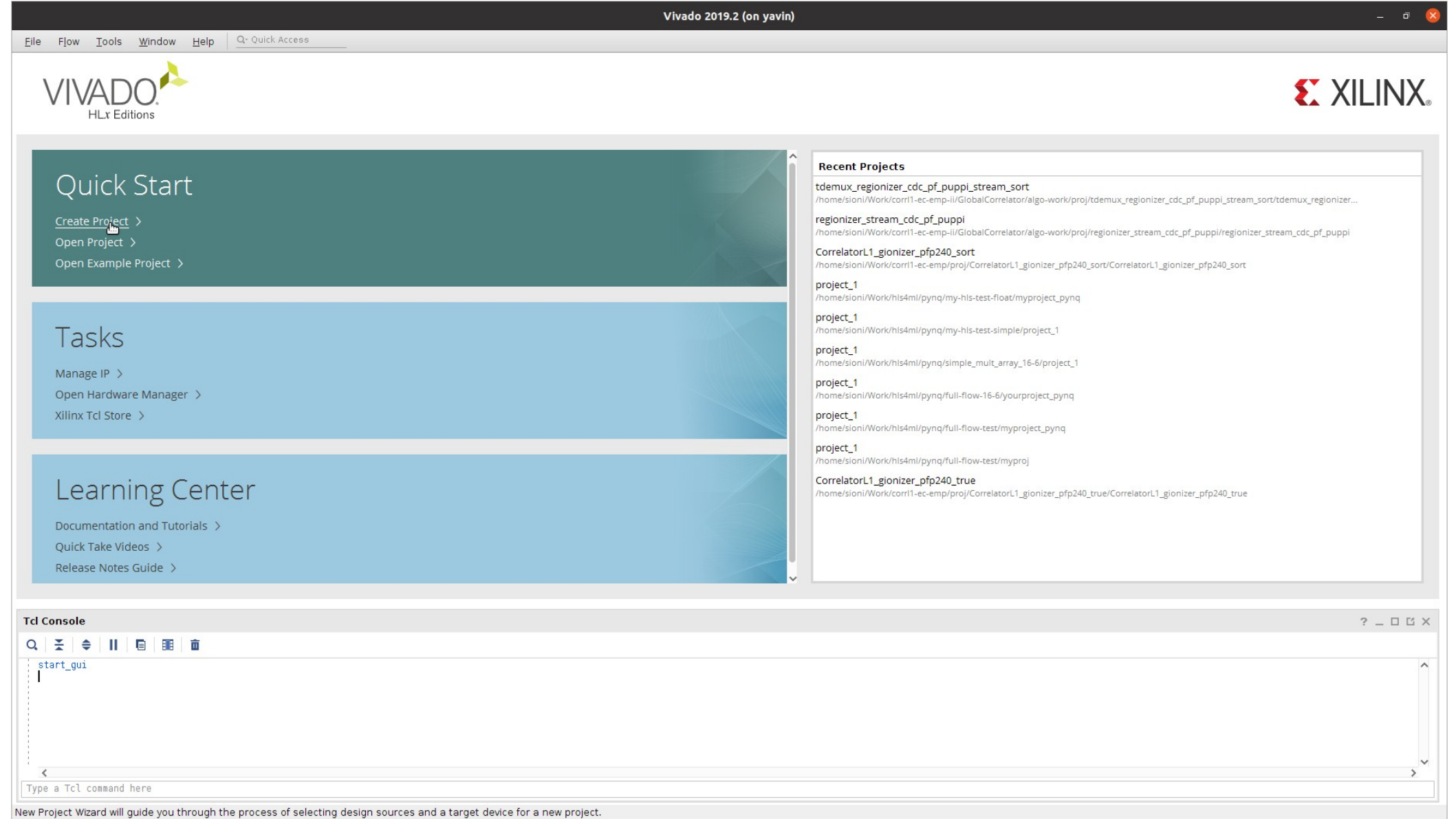
```
void myproject(
    input_axi_t in[N_IN],
    output_axi_t out[N_OUT]
        ){

    #pragma HLS INTERFACE ap_ctrl_none port=return
    #pragma HLS INTERFACE s_axilite port=in
    #pragma HLS INTERFACE s_axilite port=out

    unsigned short in_size = 0;
    unsigned short out_size = 0;

    //hls-fpga-machine-learning insert local vars

    for(unsigned i = 0; i < N_IN; i++){
        #pragma HLS unroll
        in_local[i] = in[i]; // Read input with cast
    }

    //hls-fpga-machine-learning insert call
    for(unsigned i = 0; i < N_OUT; i++){
        #pragma HLS unroll
        out[i] = out_local[i]; // Write output cast
    }
}
```

Workflow

- Thankfully, most of what takes place to make a bitfile is defined by those interface pragmas, & Vivado figures out which IPs to use to stitch it together
- We'll go through it once with the Vivado GUI, but there is a Python API for the script-based flow
- Let's go: on either yavin or geonosis machines, clone this repo and make the conda environment https://github.com/thesps/pynq_hls4ml/
  - $ conda env create -f environment.yml
  - $ conda activate pynq
  - $ jupyter notebook –no-browser & # note the port (e.g. 8888)
  - On another lxplusXYZ: $ ssh -N -f -L 8888:localhost:8888 <geonosis, yavin>
  - On your laptop: $ ssh -N -f -L 8888:localhost:8888 <you>@lxplusXYZ.cern.ch
  - On your laptop browser, go to: http://localhost:8888 and enter the token printed by Jupyter

Vivado Flow

- Once you get to the “Bitfile time” cell in the notebook, go back to the command line and execute $ vivado &
- We will follow the awesome readme from Giuesseppe here: https://github.com/fastmachinelearning/tiny-mlperf/tree/master/projects/tinyslider_pynq_z1/vivado_flow/sys
- But with a few simplifications
  - Create new board design
  - Add Zynq processing system
  - Run automation
  - Add hls4ml IP to IP repository
  - Add hls4ml NN IP to board design (myproject_axi)…
  - Run automation
  - (Skip address unmap & interface change stuff)
  - Create HDL Wrapper
  - Generate bitstream!
- Screenshots for each step in following slides


Vivado 2019.2 (on yavin)
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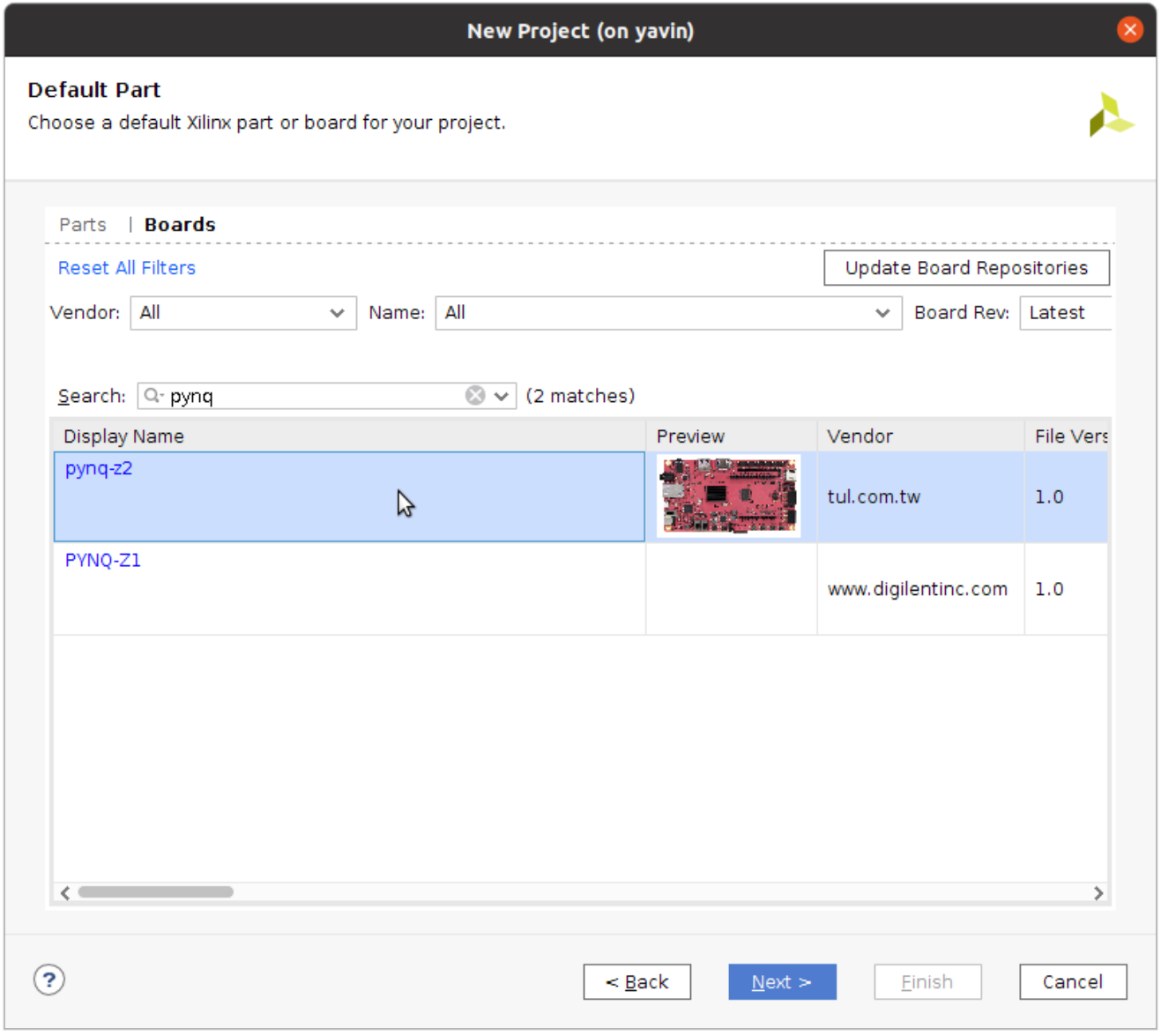
VIVADO HLx Editions
XILINX
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
Recent Projects
tdemux_regionizer_cdc_pf_puppi_stream_sort
/home/sioni/Work/corrl1-ec-emp-ii/GlobalCorrelator/algo-work/proj/tdemux_regionizer_cdc_pf_puppi_stream_sort/tdemux_regionizer...
regionizer_stream_cdc_pf_puppi
/home/sioni/Work/corrl1-ec-emp-ii/GlobalCorrelator/algo-work/proj/regionizer_stream_cdc_pf_puppi/regionizer_stream_cdc_pf_puppi
CorrelatorL1_gionizer_pfp240_sort
/home/sioni/Work/corrl1-ec-emp/proj/CorrelatorL1_gionizer_pfp240_sort/CorrelatorL1_gionizer_pfp240_sort
project_1
/home/sioni/Work/hls4ml/pynq/my-hls-test-float/myproject_pynq
project_1
/home/sioni/Work/hls4ml/pynq/my-hls-test-simple/project_1
project_1
/home/sioni/Work/hls4ml/pynq/simple_mult_array_16-6/project_1
project_1
/home/sioni/Work/hls4ml/pynq/full-flow-16-6/yourproject_pynq
project_1
/home/sioni/Work/hls4ml/pynq/full-flow-test/myproject_pynq
project_1
/home/sioni/Work/hls4ml/pynq/full-flow-test/myproj
CorrelatorL1_gionizer_pfp240_true
/home/sioni/Work/corrl1-ec-emp/proj/CorrelatorL1_gionizer_pfp240_true/CorrelatorL1_gionizer_pfp240_true
Tcl Console
start_gui
Type a Tcl command here
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

- Create a project, click “next” on each page until you reach...

Then click
“next” again,
and then “finish”



project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
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- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Open Elaborated Design

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manager

PROJECT MANAGER - project_1

Sources

Design Sources
Constraints
Simulation Sources
sim_1
Utility Sources

Hierarchy Libraries Compile Order

Properties

Select an object to see properties

Project Summary

Overview | Dashboard

Settings Edit

Project name:	project_1
Project location:	/home/sioni/Work/hls4ml/pynq/demo/project_1
Product family:	Zynq-7000
Project part:	pynq-z2 (xc7z020clg400-1)
Top module name:	Not defined
Target language:	VHDL
Simulator language:	Mixed

Board Part

Display name:	pynq-z2
Board part name:	tul.com.tw:pynq-z2:part0:1.0
Board revision:	1.0
Connectors:	No connections
Repository path:	/opt/Xilinx/Vivado/2019.2/data/boards/board_files
URL:	http://www.tul.com.tw
Board overview:	pynq-z2

Synthesis

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z020clg400-1
Strategy:	Vivado Synthesis Defaults

Implementation

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z020clg400-1
Strategy:	Vivado Implementation Defaults

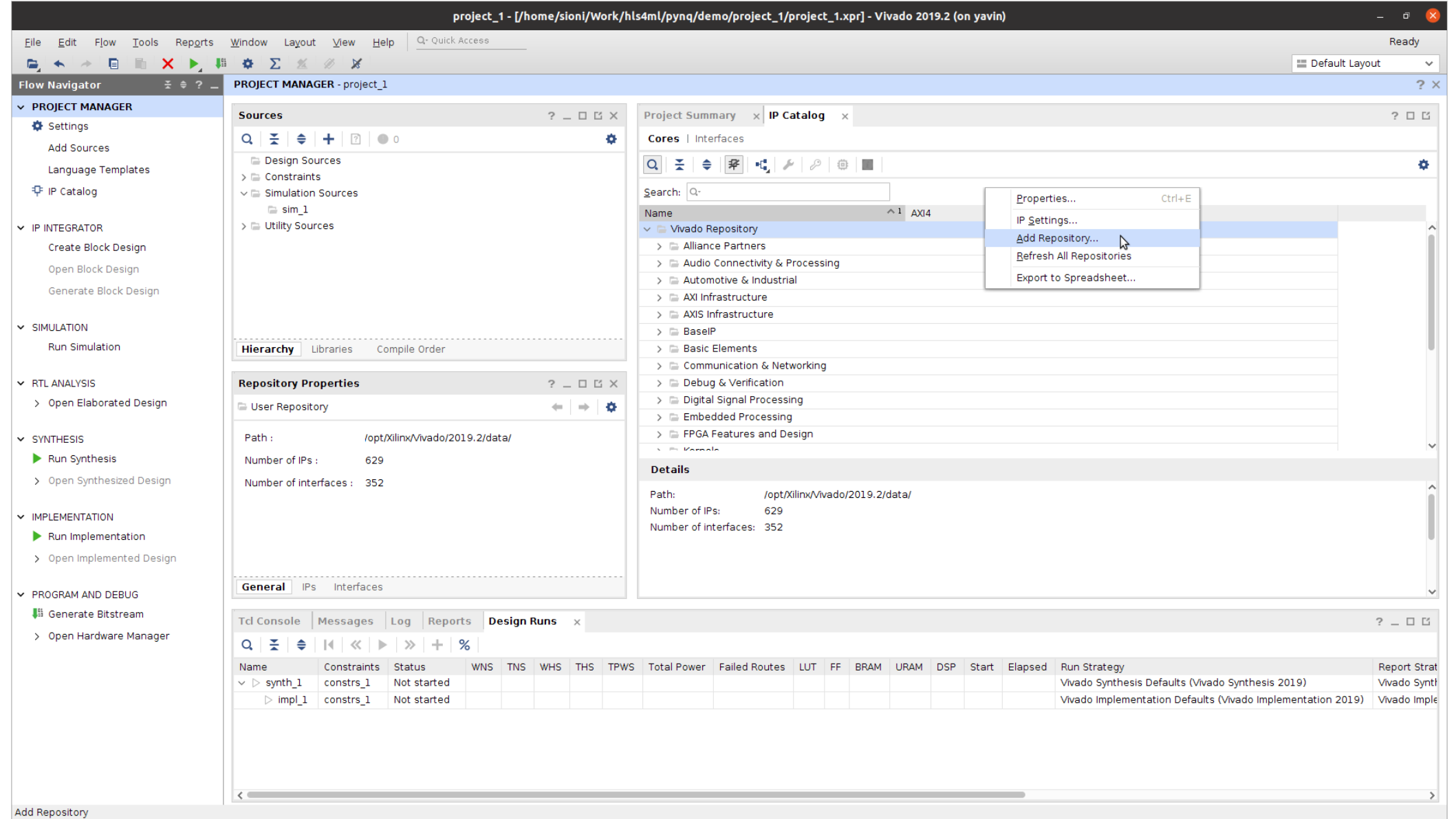
Tcl Console | Messages | Log | Reports | Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strat
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synth
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Imple

Show IP Integrator actions. Switch to IP Integrator environment.

Add NN IP

- Click “IP Catalog”
- Right click (in IP Catalog view)
- → Add repository
- → navigate to hls4ml_prj_gui
- Screenshots follow


project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)
File Edit Flow Tools Reports Window Layout View Help
Quick Access
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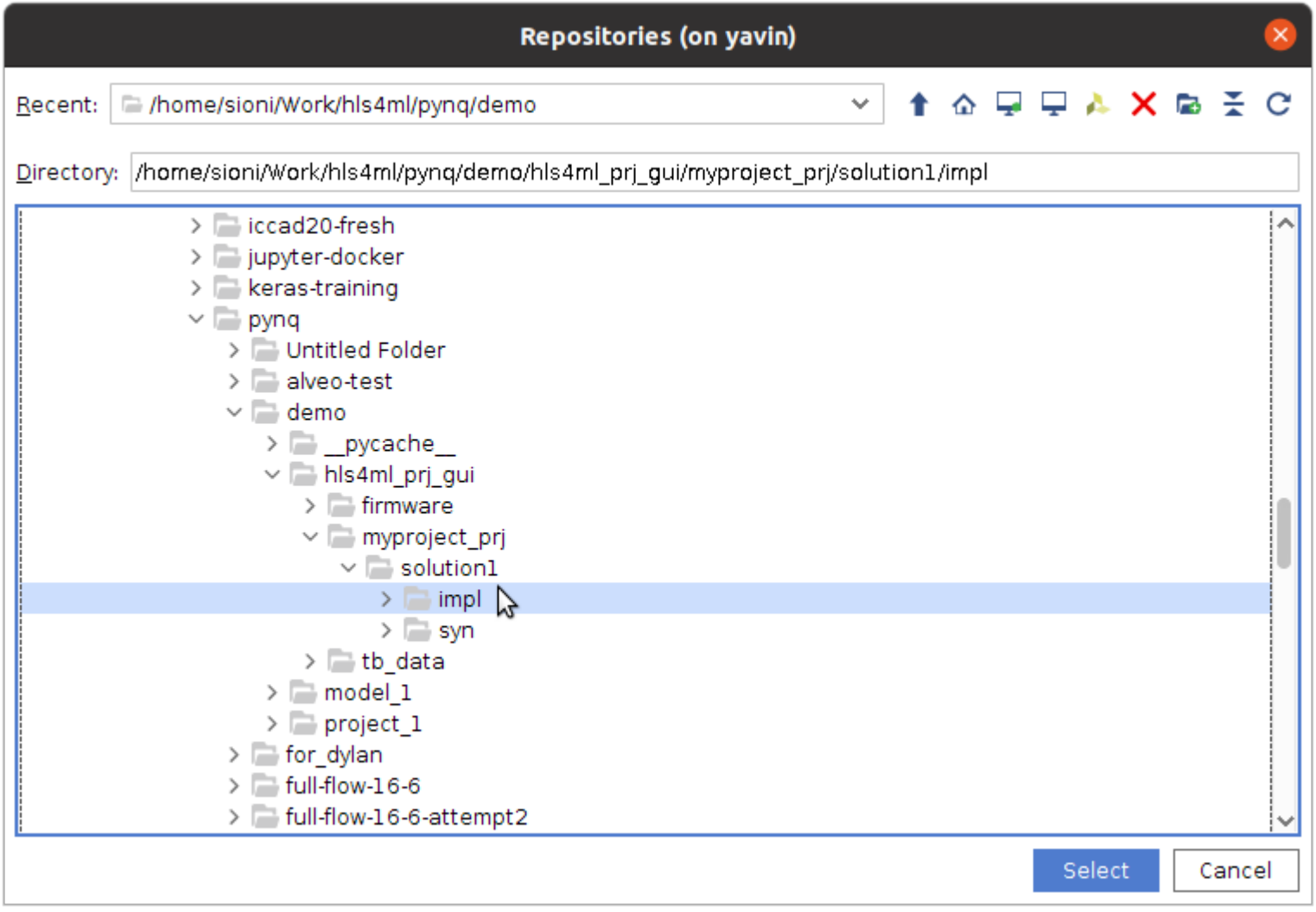
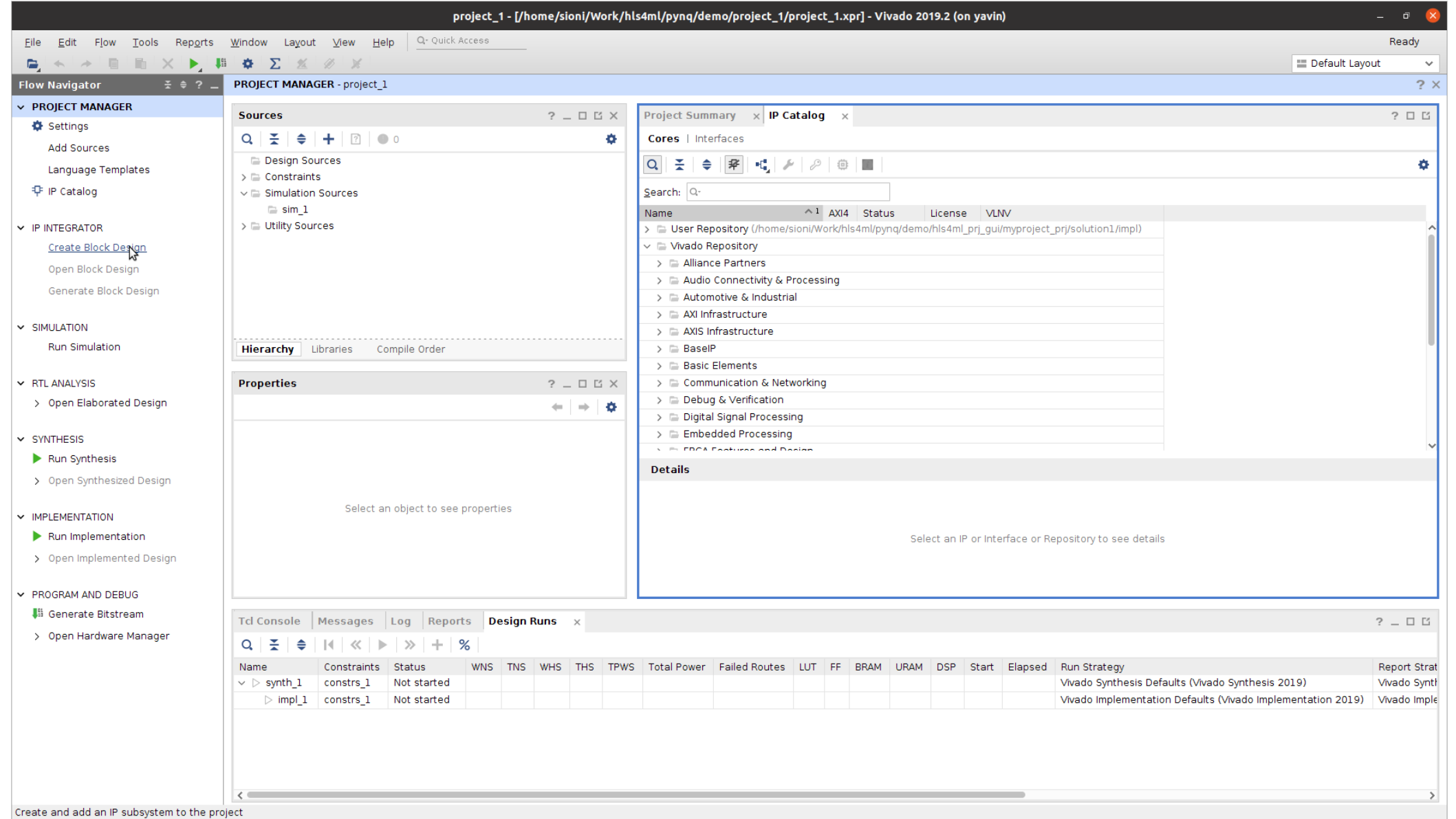
PROJECT MANAGER - project_1
Sources
Design Sources
Constraints
Simulation Sources
sim_1
Utility Sources
Hierarchy Libraries Compile Order
Repository Properties
User Repository
Path : /opt/Xilinx/Vivado/2019.2/data/
Number of IPs : 629
Number of interfaces : 352
General IPs Interfaces
Project Summary
IP Catalog
Cores | Interfaces
Search:
Name
AXI4
Vivado Repository
Alliance Partners
Audio Connectivity & Processing
Automotive & Industrial
AXI Infrastructure
AXIS Infrastructure
BaseIP
Basic Elements
Communication & Networking
Debug & Verification
Digital Signal Processing
Embedded Processing
FPGA Features and Design
Properties... Ctrl+E
IP Settings...
Add Repository...
Refresh All Repositories
Export to Spreadsheet...
Details
Path: /opt/Xilinx/Vivado/2019.2/data/
Number of IPs: 629
Number of interfaces: 352
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy Report Strat
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthesis 2019) Vivado Synth
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementation 2019) Vivado Imple
Add Repository


Repositories (on yavin)
Recent:
/home/sioni/Work/hls4ml/pynq/demo
Directory:
/home/sioni/Work/hls4ml/pynq/demo/hls4ml_prj_gui/myproject_prj/solution1/impl
iccad20-fresh
jupyter-docker
keras-training
pynq
Untitled Folder
alveo-test
demo
__pycache__
hls4ml_prj_gui
firmware
myproject_prj
solution1
impl
syn
tb_data
model_1
project_1
for_dylan
full-flow-16-6
full-flow-16-6-attempt2
Select
Cancel


project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)
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Utility Sources
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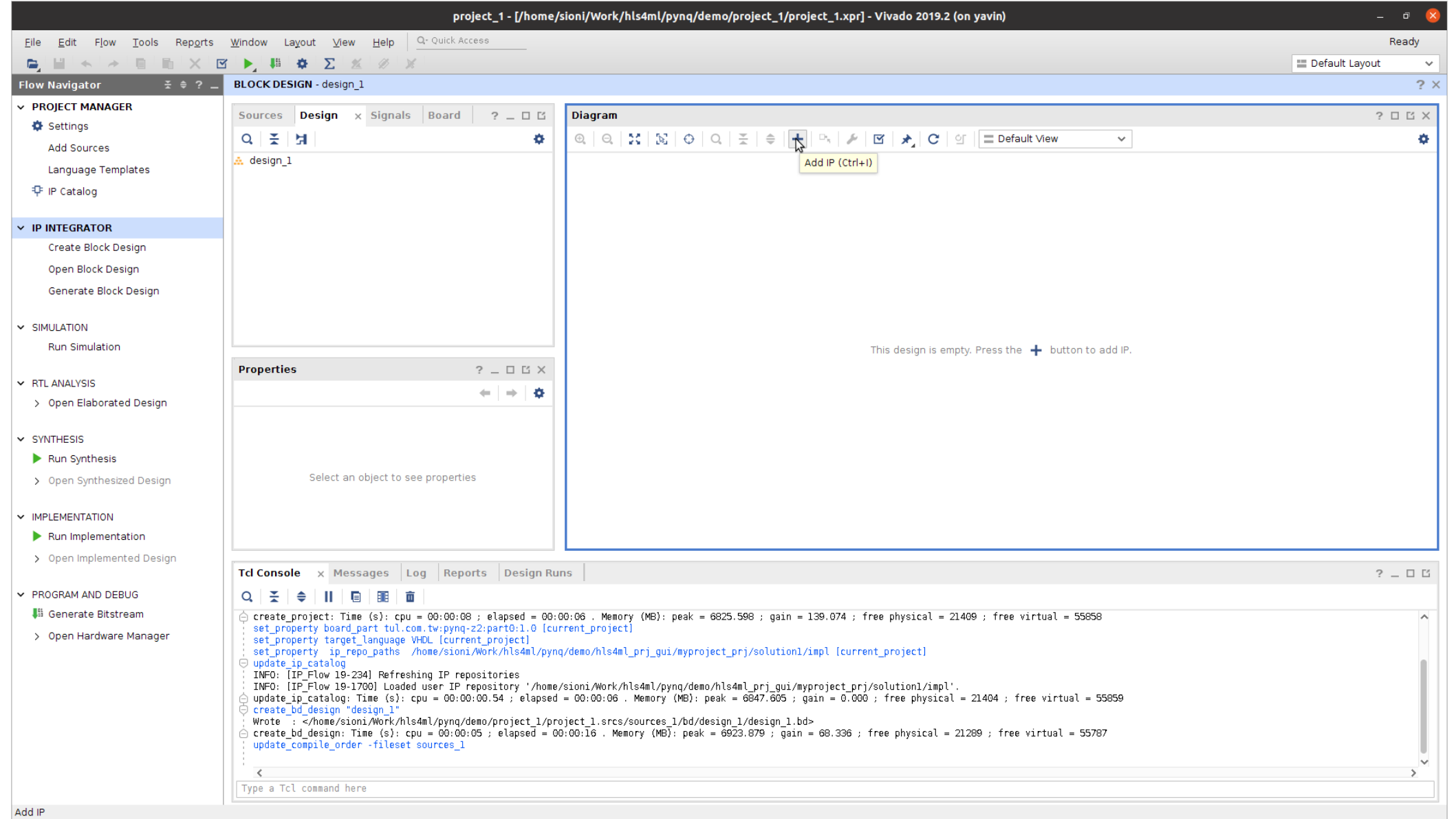
Properties
Select an object to see properties
Project Summary
IP Catalog
Cores | Interfaces
Search:
Name AXI4 Status License VLNV
User Repository (/home/sioni/Work/hls4ml/pynq/demo/hls4ml_prj_gui/myproject_prj/solution1/impl)
Vivado Repository
Alliance Partners
Audio Connectivity & Processing
Automotive & Industrial
AXI Infrastructure
AXIS Infrastructure
BaseIP
Basic Elements
Communication & Networking
Debug & Verification
Digital Signal Processing
Embedded Processing
Details
Select an IP or Interface or Repository to see details
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy Report Strat
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthesis 2019) Vivado Synth
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementation 2019) Vivado Imple
Create and add an IP subsystem to the project

- Now under ‘IP Integrator’ → Create Block Design
- Then “Okay” with the default name


project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)
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BLOCK DESIGN - design_1
Sources
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Signals
Board
design_1
Properties
Select an object to see properties
Diagram
Default View
Add IP (Ctrl+I)
This design is empty. Press the + button to add IP.
Tcl Console
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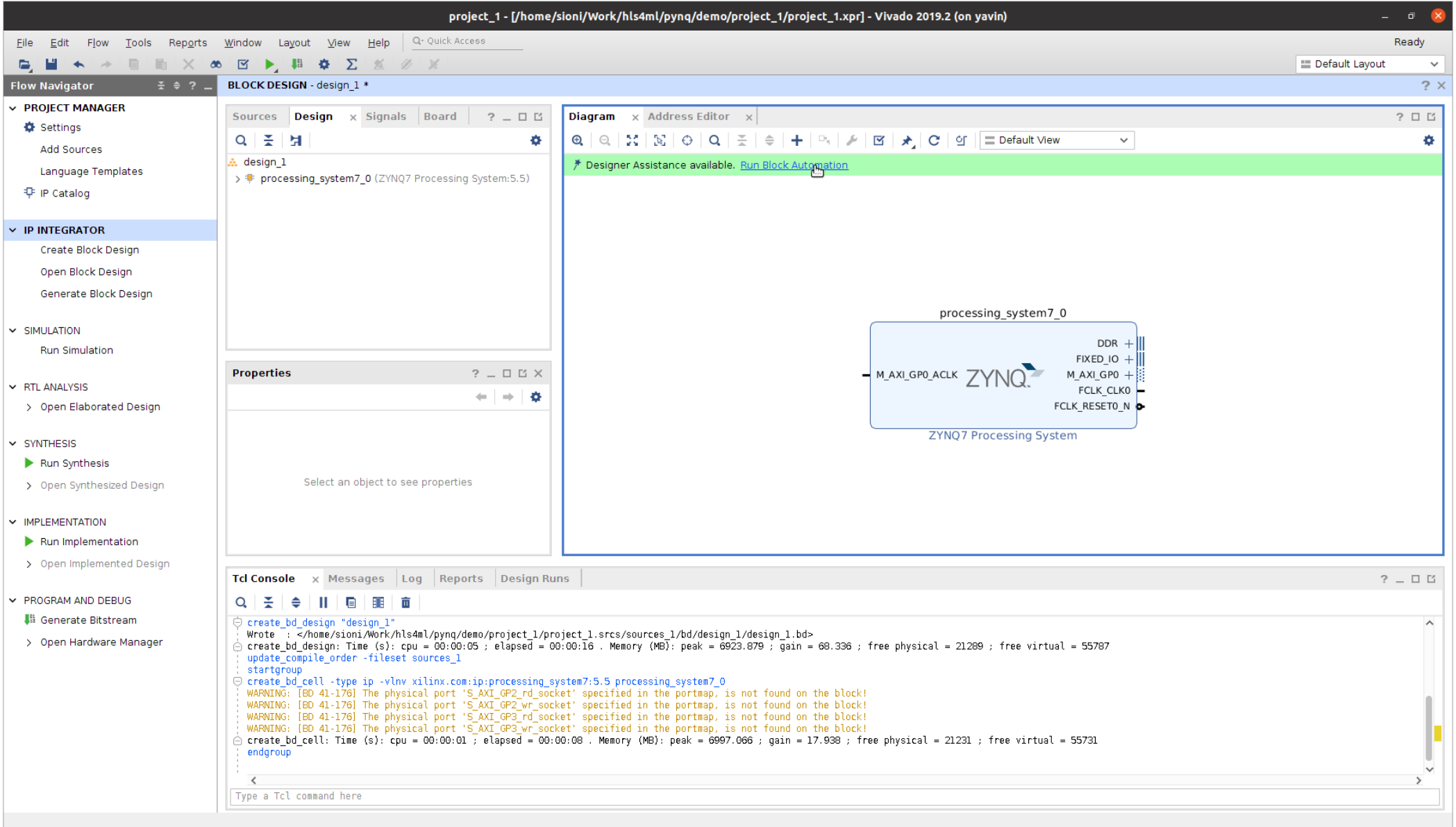
create_project: Time (s): cpu = 00:00:08 ; elapsed = 00:00:06 . Memory (MB): peak = 6825.598 ; gain = 139.074 ; free physical = 21409 ; free virtual = 55858
set_property board_part tul.com.tw:pynq-z2:part0:1.0 [current_project]
set_property target_language VHDL [current_project]
set_property ip_repo_paths /home/sioni/Work/hls4ml/pynq/demo/hls4ml_prj_gui/myproject_prj/solution1/impl [current_project]
update_ip_catalog
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1700] Loaded user IP repository '/home/sioni/Work/hls4ml/pynq/demo/hls4ml_prj_gui/myproject_prj/solution1/impl'.
update_ip_catalog: Time (s): cpu = 00:00:00.54 ; elapsed = 00:00:06 . Memory (MB): peak = 6847.605 ; gain = 0.000 ; free physical = 21404 ; free virtual = 55859
create_bd_design "design_1"
Wrote : </home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.srcs/sources_1/bd/design_1/design_1.bd>
create_bd_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:16 . Memory (MB): peak = 6923.879 ; gain = 68.336 ; free physical = 21289 ; free virtual = 55787
update_compile_order -fileset sources_1
Type a Tcl command here
Add IP

- Now we will add IPs (components, basically)
- Search “zynq” in the tab and add the zynq7 processing system
- → In the green tab click “Run Block automation”
- Click “Okay” with default values


project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)
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BLOCK DESIGN - design_1 *
Sources Design Signals Board
design_1
processing_system7_0 (ZYNQ7 Processing System:5.5)
Properties
Select an object to see properties
Diagram Address Editor
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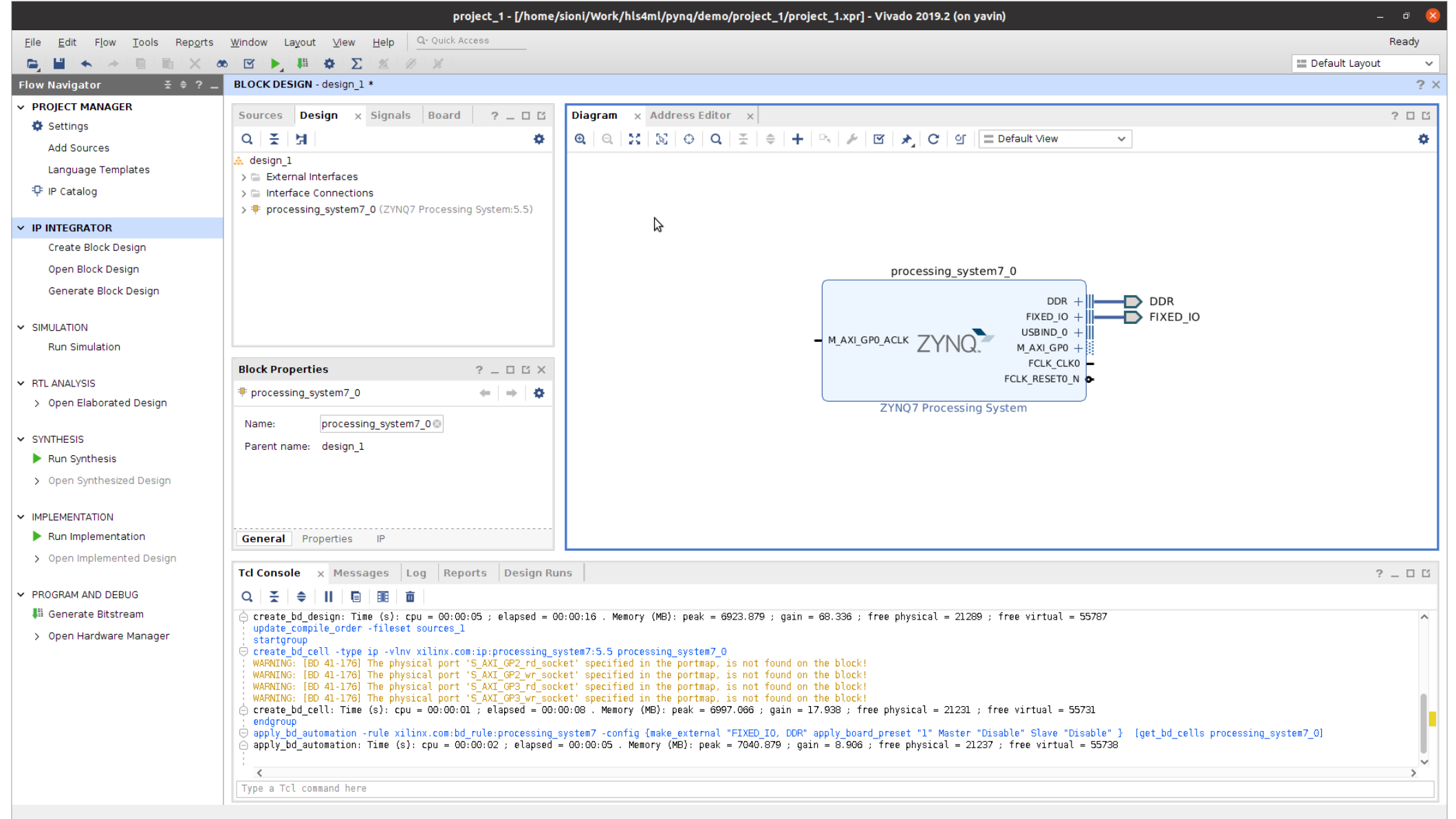
Designer Assistance available. Run Block Automation
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
Tcl Console Messages Log Reports Design Runs
create_bd_design "design_1"
Wrote : </home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.srcs/sources_1/bd/design_1/design_1.bd>
create_bd_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:16 . Memory (MB): peak = 6923.879 ; gain = 68.336 ; free physical = 21289 ; free virtual = 55787
update_compile_order -fileset sources_1
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
WARNING: [BD 41-176] The physical port 'S_AXI_GP2_rd_socket' specified in the portmap, is not found on the block!
WARNING: [BD 41-176] The physical port 'S_AXI_GP2_wr_socket' specified in the portmap, is not found on the block!
WARNING: [BD 41-176] The physical port 'S_AXI_GP3_rd_socket' specified in the portmap, is not found on the block!
WARNING: [BD 41-176] The physical port 'S_AXI_GP3_wr_socket' specified in the portmap, is not found on the block!
create_bd_cell: Time (s): cpu = 00:00:01 ; elapsed = 00:00:08 . Memory (MB): peak = 6997.066 ; gain = 17.938 ; free physical = 21231 ; free virtual = 55731
endgroup
Type a Tcl command here


project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)
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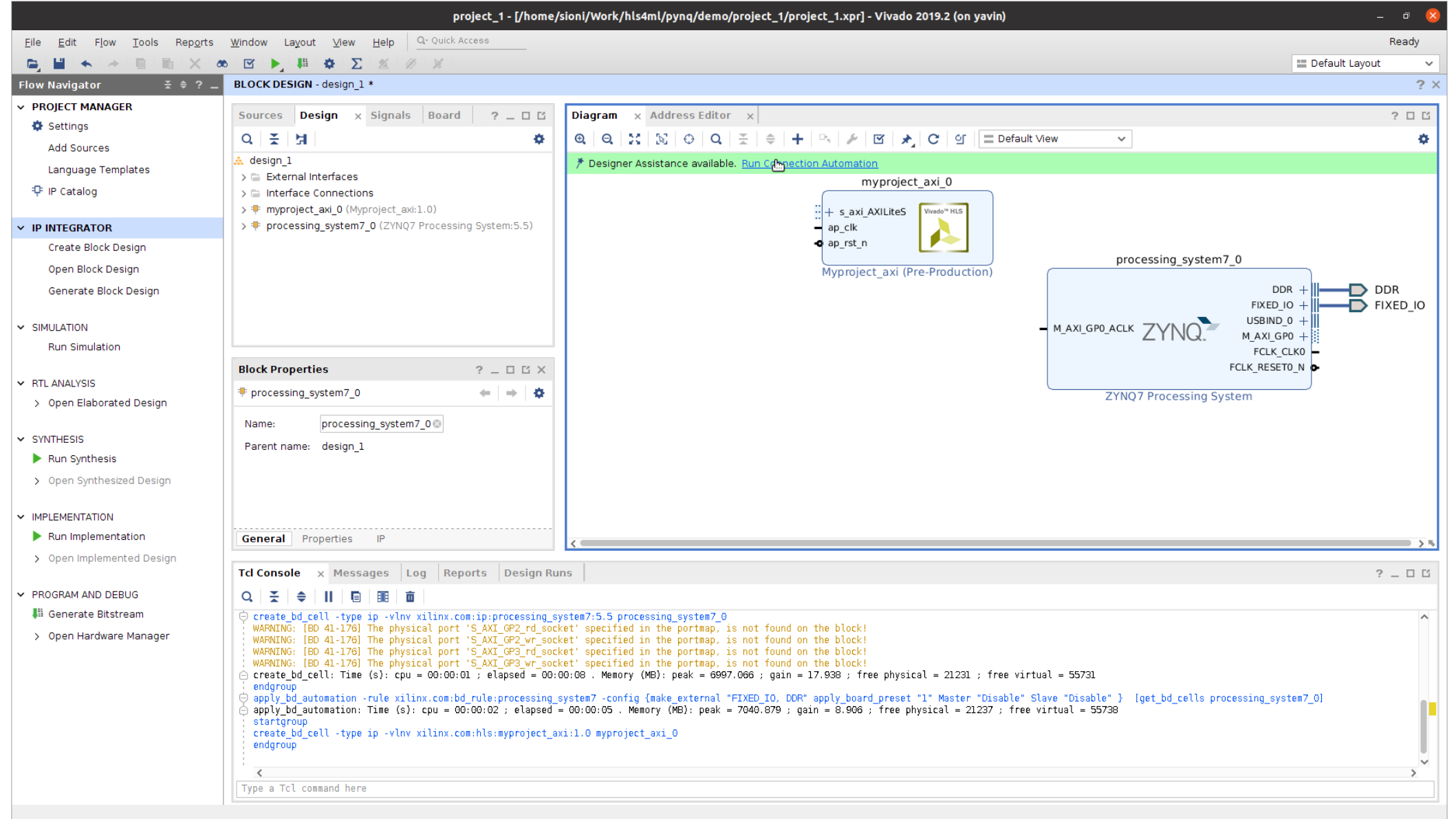
Sources Design Signals Board
design_1
External Interfaces
Interface Connections
processing_system7_0 (ZYNQ7 Processing System:5.5)
Block Properties
processing_system7_0
Name: processing_system7_0
Parent name: design_1
General Properties IP
Diagram Address Editor
Default View
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
USBIND_0
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
DDR
FIXED_IO
ZYNQ7 Processing System
Tcl Console Messages Log Reports Design Runs
create_bd_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:16 . Memory (MB): peak = 6923.879 ; gain = 68.336 ; free physical = 21289 ; free virtual = 55787
update_compile_order -fileset sources_1
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
WARNING: [BD 41-176] The physical port 'S_AXI_GP2_rd_socket' specified in the portmap, is not found on the block!
WARNING: [BD 41-176] The physical port 'S_AXI_GP2_wr_socket' specified in the portmap, is not found on the block!
WARNING: [BD 41-176] The physical port 'S_AXI_GP3_rd_socket' specified in the portmap, is not found on the block!
WARNING: [BD 41-176] The physical port 'S_AXI_GP3_wr_socket' specified in the portmap, is not found on the block!
create_bd_cell: Time (s): cpu = 00:00:01 ; elapsed = 00:00:08 . Memory (MB): peak = 6997.066 ; gain = 17.938 ; free physical = 21231 ; free virtual = 55731
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master "Disable" Slave "Disable" } [get_bd_cells processing_system7_0]
apply_bd_automation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 . Memory (MB): peak = 7040.879 ; gain = 8.906 ; free physical = 21237 ; free virtual = 55738
Type a Tcl command here

- Now hit the “+” add IP again
- Search “myproject” and add “Myproject_axi”
- This is our NN


project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)
File Edit Flow Tools Reports Window Layout View Help
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Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - design_1 *
Sources Design Signals Board
design_1
External Interfaces
Interface Connections
myproject_axi_0 (Myproject_axi:1.0)
processing_system7_0 (ZYNQ7 Processing System:5.5)
Block Properties
processing_system7_0
Name: processing_system7_0
Parent name: design_1
General Properties IP
Diagram Address Editor
Default View
Designer Assistance available. Run Connection Automation
myproject_axi_0
s_axi_AXILiteS
ap_clk
ap_rst_n
Vivado HLS
Myproject_axi (Pre-Production)
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
USBIND_0
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
Tcl Console Messages Log Reports Design Runs
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
WARNING: [BD 41-176] The physical port 'S_AXI_GP2_rd_socket' specified in the portmap, is not found on the block!
WARNING: [BD 41-176] The physical port 'S_AXI_GP2_wr_socket' specified in the portmap, is not found on the block!
WARNING: [BD 41-176] The physical port 'S_AXI_GP3_rd_socket' specified in the portmap, is not found on the block!
WARNING: [BD 41-176] The physical port 'S_AXI_GP3_wr_socket' specified in the portmap, is not found on the block!
create_bd_cell: Time (s): cpu = 00:00:01 ; elapsed = 00:00:08 . Memory (MB): peak = 6997.066 ; gain = 17.938 ; free physical = 21231 ; free virtual = 55731
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master "Disable" Slave "Disable" } [get_bd_cells processing_system7_0]
apply_bd_automation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 . Memory (MB): peak = 7040.879 ; gain = 8.906 ; free physical = 21237 ; free virtual = 55738
startgroup
create_bd_cell -type ip -vlnv xilinx.com:hls:myproject_axi:1.0 myproject_axi_0
endgroup
Type a Tcl command here

project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

- PROJECT MANAGER
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  - Generate Block Design
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  - Run Simulation
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  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

BLOCK DESIGN - design_1 *

Sources | Design | Signals | Board

- design_1
  - External Interfaces
  - Interface Connections
  - Nets
  - myproject_axi_0 (Myproject_axi:1.0)
    - s_axi_AXILiteS
    - ap_clk
    - ap_rst_n
  - processing_system7_0 (ZYNQ7 Processing System:5.5)
  - ps7_0_axi_periph
  - rst_ps7_0_100M (Processor System Reset:5.0)

Block Interface Properties

s_axi_AXILiteS

Name: s_axi_AXILiteS

Mode: SLAVE

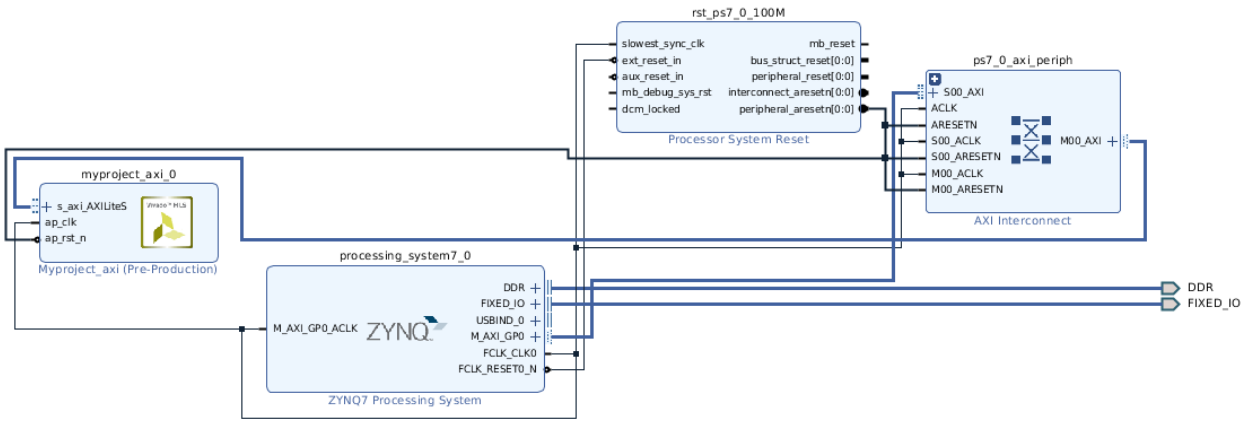
Connection: ps7_0_axi_periph_M00_AXI

Associated clock: ap_clk

General | Properties

Diagram | Address Editor

Default View

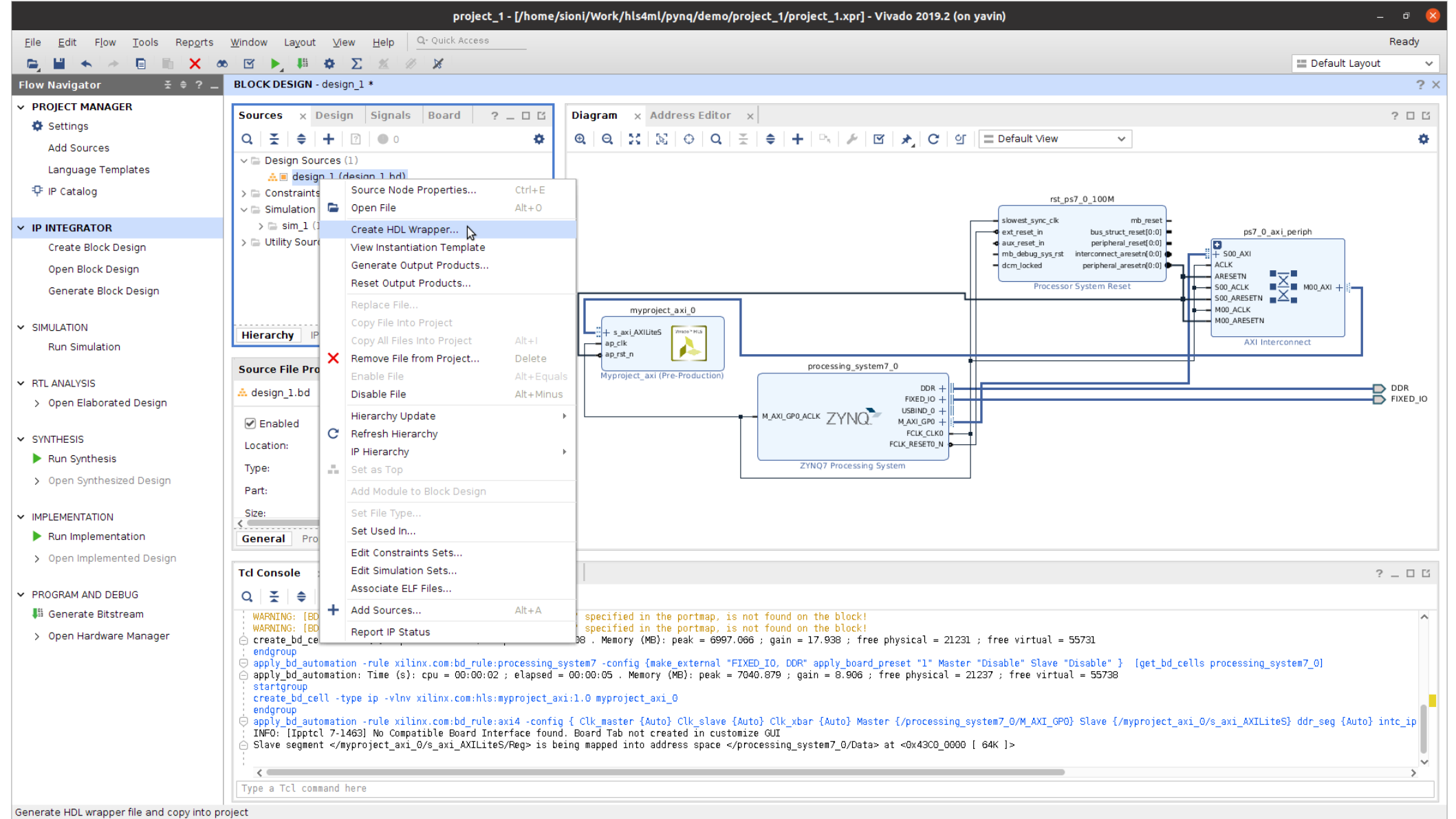


Tcl Console | Messages | Log | Reports | Design Runs

```
WARNING: [BD 41-176] The physical port 'S_AXI_GP3_rd_socket' specified in the portmap, is not found on the block!
WARNING: [BD 41-176] The physical port 'S_AXI_GP3_wr_socket' specified in the portmap, is not found on the block!
create_bd_cell: Time (s): cpu = 00:00:01 ; elapsed = 00:00:08 . Memory (MB): peak = 6997.066 ; gain = 17.938 ; free physical = 21231 ; free virtual = 55731
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master "Disable" Slave "Disable" }  [get_bd_cells processing_system7_0]
apply_bd_automation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 . Memory (MB): peak = 7040.879 ; gain = 8.906 ; free physical = 21237 ; free virtual = 55738
startgroup
create_bd_cell -type ip -vlnv xilinx.com:hls:myproject_axi:1.0 myproject_axi_0
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config { Clk_master {Auto} Clk_slave {Auto} Clk_xbar {Auto} Master {/processing_system7_0/M_AXI_GP0} Slave {/myproject_axi_0/s_axi_AXILiteS} ddr_seg {Auto} intc_ip
INFO: [Ipptcl 7-1463] No Compatible Board Interface found. Board Tab not created in customize GUI
Slave segment </myproject_axi_0/s_axi_AXILiteS/Reg> is being mapped into address space </processing_system7_0/Data> at <0x43C0_0000 [ 64K ]>
```

Type a Tcl command here

- In “sources” tab, right click “design 1” and “generate HDL wrapper”
- Hit “okay” again


project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)
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Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - design_1 *
Sources
Design
Signals
Board
Design Sources (1)
design_1 (design_1.bd)
Constraints
Simulation
sim_1
Utility Sour
Hierarchy
Source File Pro
design_1.bd
Enabled
Location:
Type:
Part:
Size:
General
Source Node Properties... Ctrl+E
Open File Alt+O
Create HDL Wrapper...
View Instantiation Template
Generate Output Products...
Reset Output Products...
Replace File...
Copy File Into Project
Copy All Files Into Project Alt+I
Remove File from Project... Delete
Enable File Alt+Equals
Disable File Alt+Minus
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Set as Top
Add Module to Block Design
Set File Type...
Set Used In...
Edit Constraints Sets...
Edit Simulation Sets...
Associate ELF Files...
Add Sources... Alt+A
Report IP Status
Diagram
Address Editor
Default View
rst_ps7_0_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
ps7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
myproject_axi_0
s_axi_AXILiteS
ap_clk
ap_rst_n
Myproject_axi (Pre-Production)
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
USBIND_0
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
Tcl Console
WARNING: [BD
specified in the portmap, is not found on the block!
create_bd_ce
08 . Memory (MB): peak = 6997.066 ; gain = 17.938 ; free physical = 21231 ; free virtual = 55731
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master "Disable" Slave "Disable" } [get_bd_cells processing_system7_0]
apply_bd_automation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 . Memory (MB): peak = 7040.879 ; gain = 8.906 ; free physical = 21237 ; free virtual = 55738
startgroup
create_bd_cell -type ip -vlnv xilinx.com:hls:myproject_axi:1.0 myproject_axi_0
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config { Clk_master {Auto} Clk_slave {Auto} Clk_xbar {Auto} Master {/processing_system7_0/M_AXI_GP0} Slave {/myproject_axi_0/s_axi_AXILiteS} ddr_seg {Auto} intc_ip
INFO: [Ipptcl 7-1463] No Compatible Board Interface found. Board Tab not created in customize GUI
Slave segment </myproject_axi_0/s_axi_AXILiteS/Reg> is being mapped into address space </processing_system7_0/Data> at <0x43C0_0000 [64K]>
Type a Tcl command here
Generate HDL wrapper file and copy into project

- Generate Bitstream!
- Click “Yes” (run synth and implementation first)
- And “okay” one more time...

project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

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- Open Block Design
- Generate Block Design

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- Run Simulation

RTL ANALYSIS
- Open Elaborated Design

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manager

BLOCK DESIGN - design_1

Sources | Design | Signals | Board

Design Sources (1)
- design_1_wrapper(STRUCTURE) (design_1_wrapper.
Constraints
Simulation Sources (1)
- sim_1 (1)
Utility Sources

Hierarchy | IP Sources | Libraries | Compile Order

Block Interface Properties

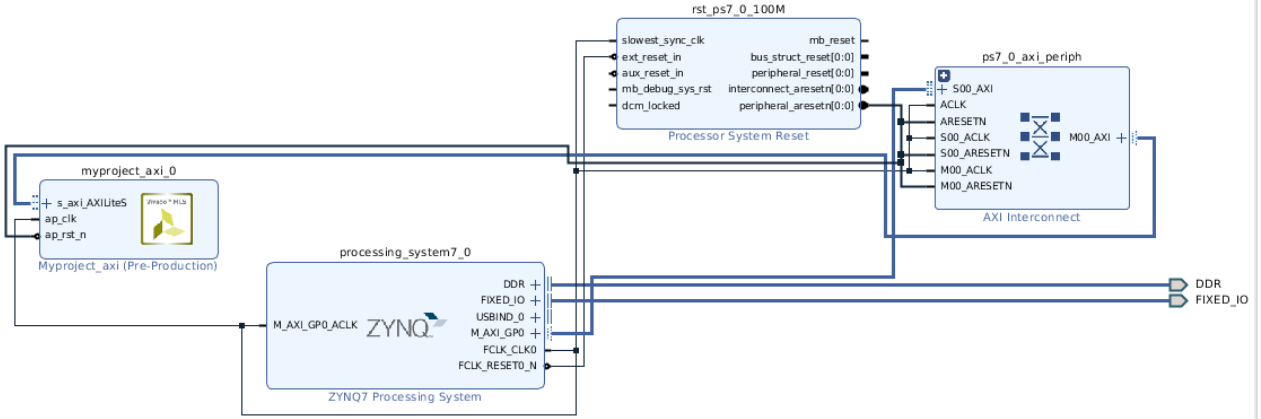
s_axi_AXILiteS

Name: s_axi_AXILiteS
Mode: SLAVE
Connection: ps7_0_axi_periph_M00_AXI
Associated clock: ap_clk

General | Properties

Diagram | Address Editor

Default View



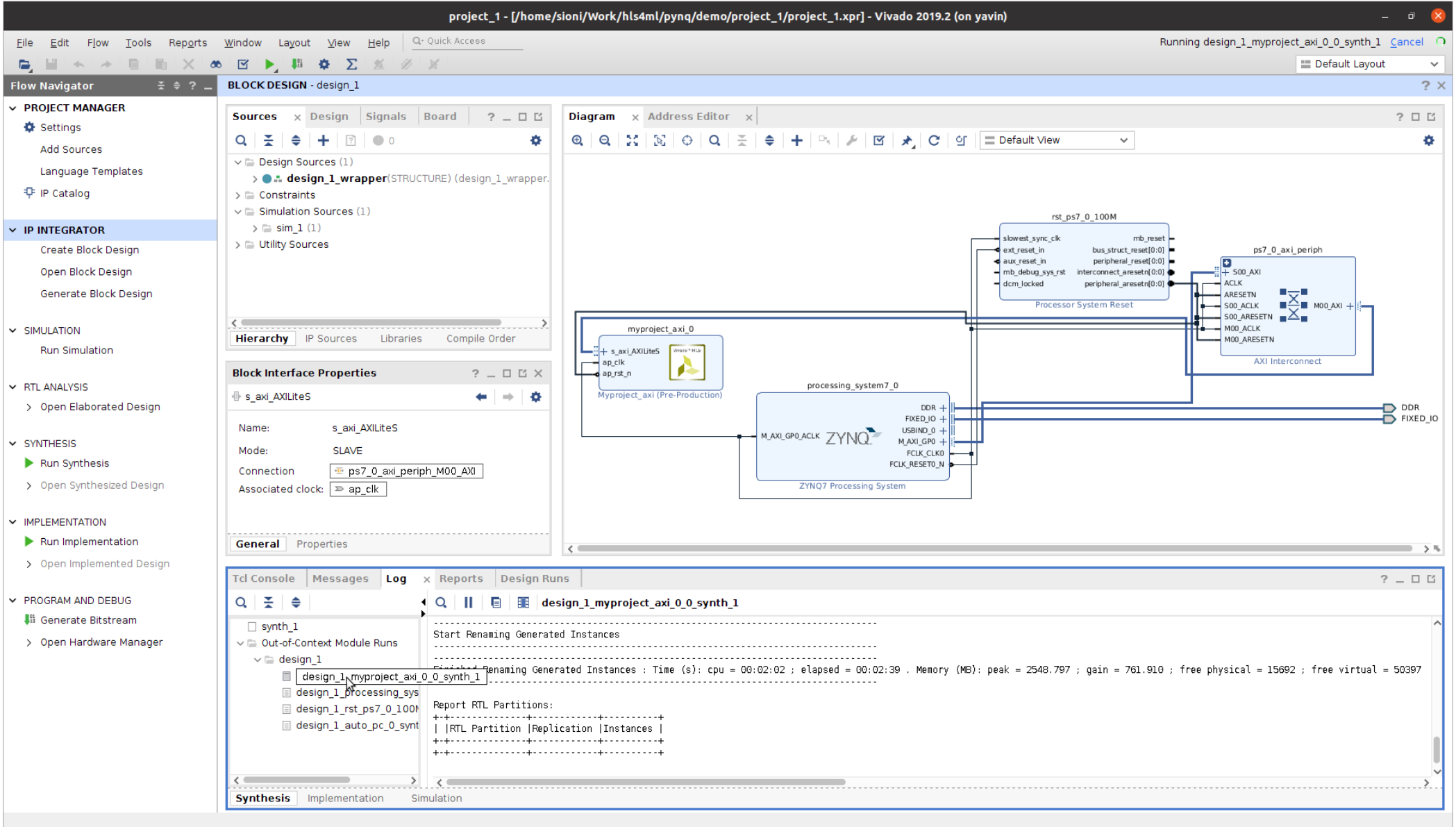
Tcl Console | Messages | Log | Reports | Design Runs

```
apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config { Clk_master {Auto} Clk_slave {Auto} Clk_xbar {Auto} Master {/processing_system7_0/M_AXI_GP0} Slave {/myproject_axi_0/s_axi_AXILiteS} ddr_seg {Auto} intc_ip
INFO: [Ipptcl 7-1463] No Compatible Board Interface found. Board Tab not created in customize GUI
Slave segment </myproject_axi_0/s_axi_AXILiteS/Reg> is being mapped into address space </processing_system7_0/Data> at <0x43C0_0000 [ 64K ]>
make_wrapper -files [get_files /home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.srcs/sources_1/bd/design_1/design_1.bd] -top
WARNING: [BD 41-702] Propagation TCL tries to overwrite USER strength parameter POW_M_AXI_GP0_FREQMHZ(10) on '/processing_system7_0' with propagated value(100). Command ignored
Wrote  : </home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.srcs/sources_1/bd/design_1/design_1.bd>
Wrote  : </home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.srcs/sources_1/bd/design_1/ui/bd_1f5defd0.ui>
VHDL Output written to : /home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.srcs/sources_1/bd/design_1/synth/design_1.vhd
VHDL Output written to : /home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.srcs/sources_1/bd/design_1/sim/design_1.vhd
VHDL Output written to : /home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.srcs/sources_1/bd/design_1/hdl/design_1_wrapper.vhd
make_wrapper: Time (s): cpu = 00:00:02 ; elapsed = 00:00:13 . Memory (MB): peak = 7175.809 ; gain = 93.750 ; free physical = 21110 ; free virtual = 55610
add_files -norecurse /home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.srcs/sources_1/bd/design_1/hdl/design_1_wrapper.vhd
```

Type a Tcl command here

Generate a programming file after implementation

- Then wait ~10 minutes
- Look in “log” at the bottom to see what’s going on
- It will synthesize each IP (4 of them), then the whole board design, then run implementation


project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Running design_1_myproject_axi_0_0_synth_1 Cancel
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
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IP INTEGRATOR
Create Block Design
Open Block Design
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Run Simulation
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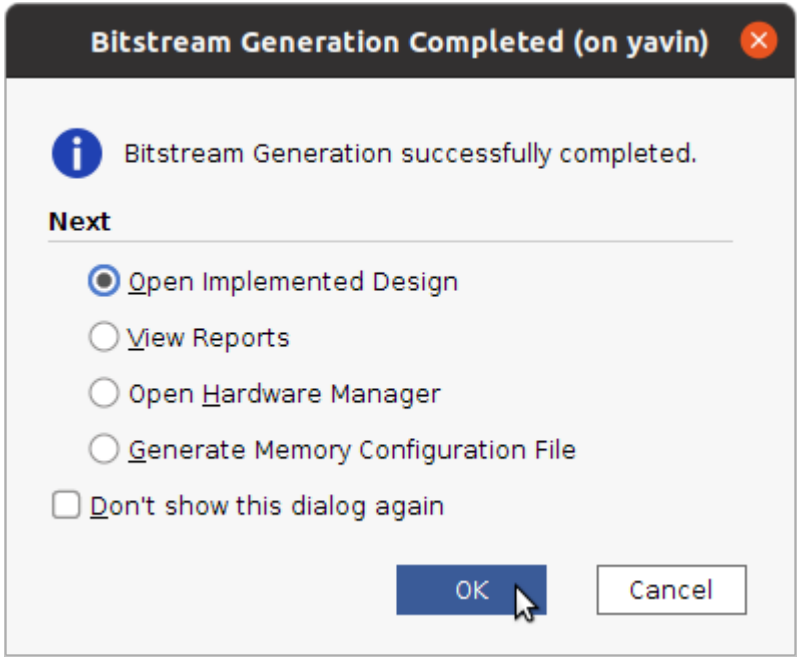
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - design_1
Sources
Design
Signals
Board
Design Sources (1)
design_1_wrapper(STRUCTURE) (design_1_wrapper.
Constraints
Simulation Sources (1)
sim_1 (1)
Utility Sources
Hierarchy
IP Sources
Libraries
Compile Order
Block Interface Properties
s_axi_AXILiteS
Name: s_axi_AXILiteS
Mode: SLAVE
Connection ps7_0_axi_periph_M00_AXI
Associated clock: ap_clk
General
Properties
Diagram
Address Editor
Default View
rst_ps7_0_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
ps7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
myproject_axi_0
s_axi_AXILiteS
ap_clk
ap_rst_n
Myproject_axi (Pre-Production)
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
USBIND_0
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
DDR
FIXED_IO
Tcl Console
Messages
Log
Reports
Design Runs
design_1_myproject_axi_0_0_synth_1
synth_1
Out-of-Context Module Runs
design_1
design_1_myproject_axi_0_0_synth_1
design_1_processing_sys
design_1_rst_ps7_0_100
design_1_auto_pc_0_synt
Start Renaming Generated Instances
Finished Renaming Generated Instances : Time (s): cpu = 00:02:02 ; elapsed = 00:02:39 . Memory (MB): peak = 2548.797 ; gain = 761.910 ; free physical = 15692 ; free virtual = 50397
Report RTL Partitions:
| |RTL Partition |Replication |Instances |
Synthesis
Implementation
Simulation


Bitstream Generation Completed (on yavin)
Bitstream Generation successfully completed.
Next
Open Implemented Design
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel

project_1 - [/home/sioni/Work/hls4ml/pynq/demo/project_1/project_1.xpr] - Vivado 2019.2 (on yavin)

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Default Layout

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- Generate Block Design

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- Run Simulation

RTL ANALYSIS
- Open Elaborated Design

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
- Run Implementation
- Open Implemented Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic

IMPLEMENTED DESIGN - xc7z020clg400-1

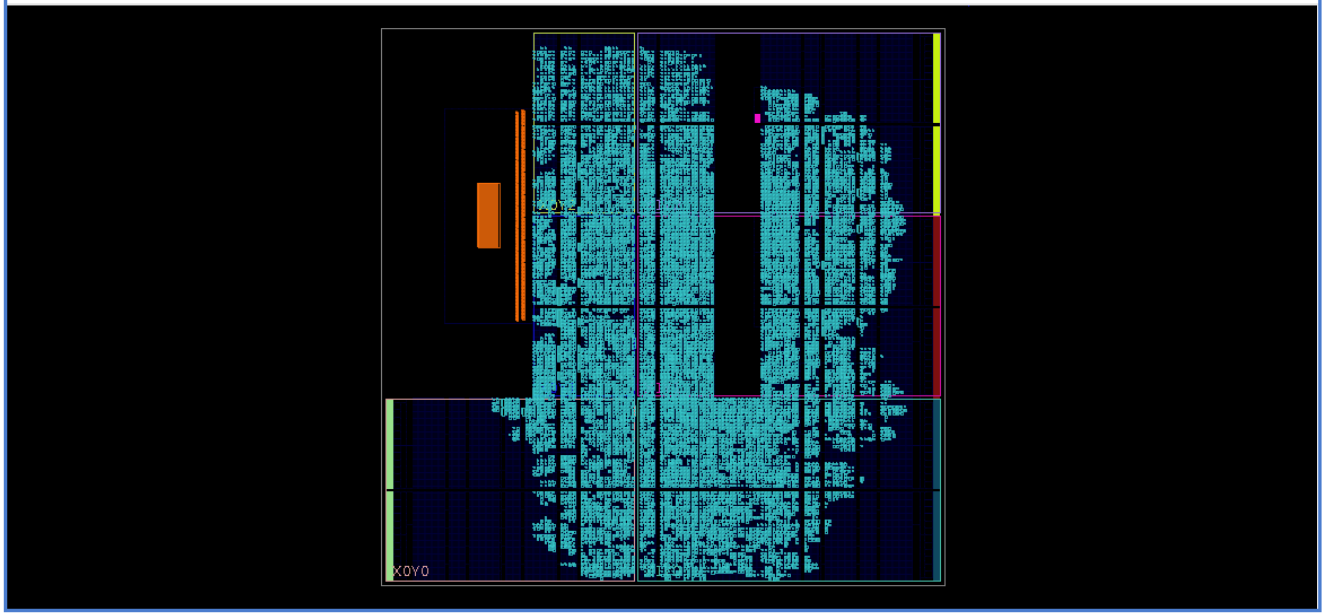
Sources | Netlist

design_1_wrapper
- Nets (130)
- design_1_i (design_1)

Block Interface Properties

Select an object to see properties

Project Summary | Device



Tcl Console | Messages | Log | Reports | Design Runs | Power | Timing

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (0)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.403 ns	Worst Hold Slack (WHS):	0.011 ns	Worst Pulse Width Slack (WPWS):	4.020 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	59258	Total Number of Endpoints:	59258	Total Number of Endpoints:	25807

All user specified timing constraints are met.

Timing Summary - impl_1 (saved)