INJECTION TEST:
BUILDING A DATA INJECTOR FOR THE ATLAS LIQUID ARGON SIGNAL PROCESSOR

2021 CAP VIRTUAL CONGRESS

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ATLAS & THE ROAD TO HIGH LUMINOSITY LHC

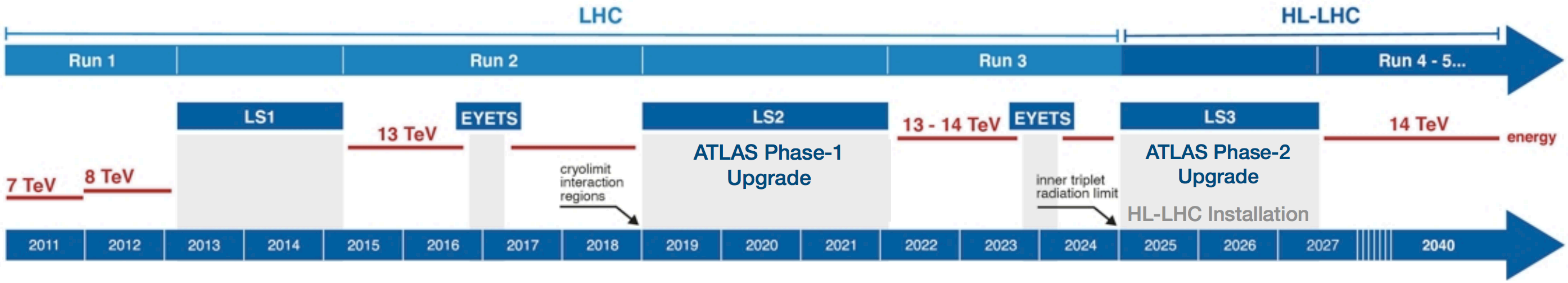


FIG 1: PROJECT SCHEDULE OF LHC/HL-LHC PLAN [1]

- The Large Hadron Collider is due to undergo major design changes with the goal of colliding protons at $\sqrt{s} =$ **14** TeV and with a peak luminosity of $7.5 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$.
- As a result, detectors in the LHC ring like ATLAS need to undergo upgrades necessary to maintain good physics performance in the HL-LHC environment.
- One of these upgrades deals with the LAr calorimeter system carried out in 2 phases:
  - ✦ **Trigger**: A more discriminating trigger† (and hence a readout system‡) is needed in a higher pileup environment.
  - ✦ **Radiation**: Planned radiation dose exceeds capacity of existing readout system

† Planned for Phase I upgrade

‡ Planned for Phase II upgrade

LAr ELECTRONIC UPGRADES

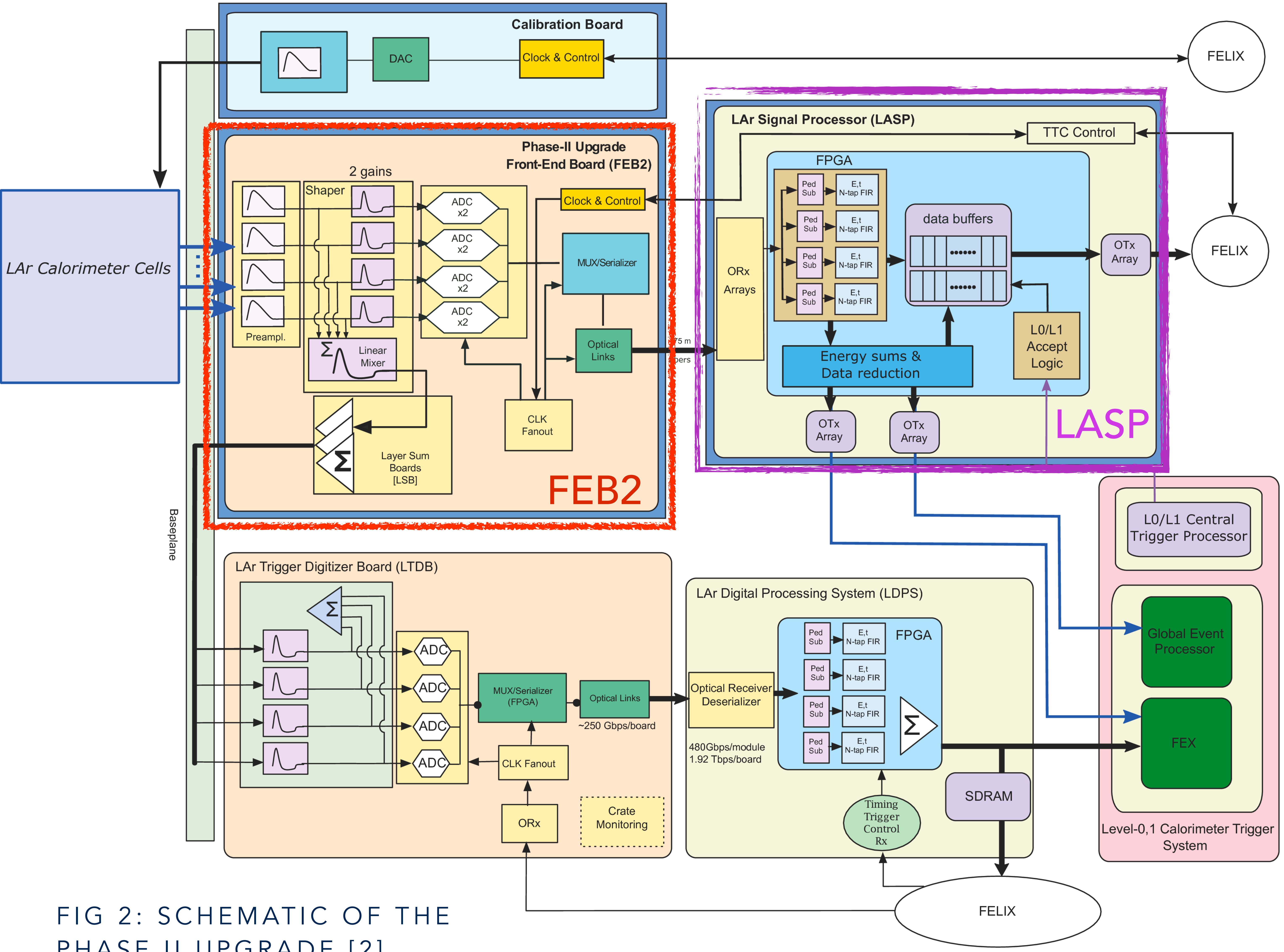


FIG 2: SCHEMATIC OF THE PHASE II UPGRADE [2]

Two major changes are planned for Phase II LAr Electronics upgrade

1 . FEB2 (Front End Board 2)

Signals passed through an analogue filter shaper for two different gains (high & low gain)

↓

ADC digitize this into 16-bit words

↓

A serialized stream is sent to the LASP at 10.24Gbps using CERN-based lpGBT chips.

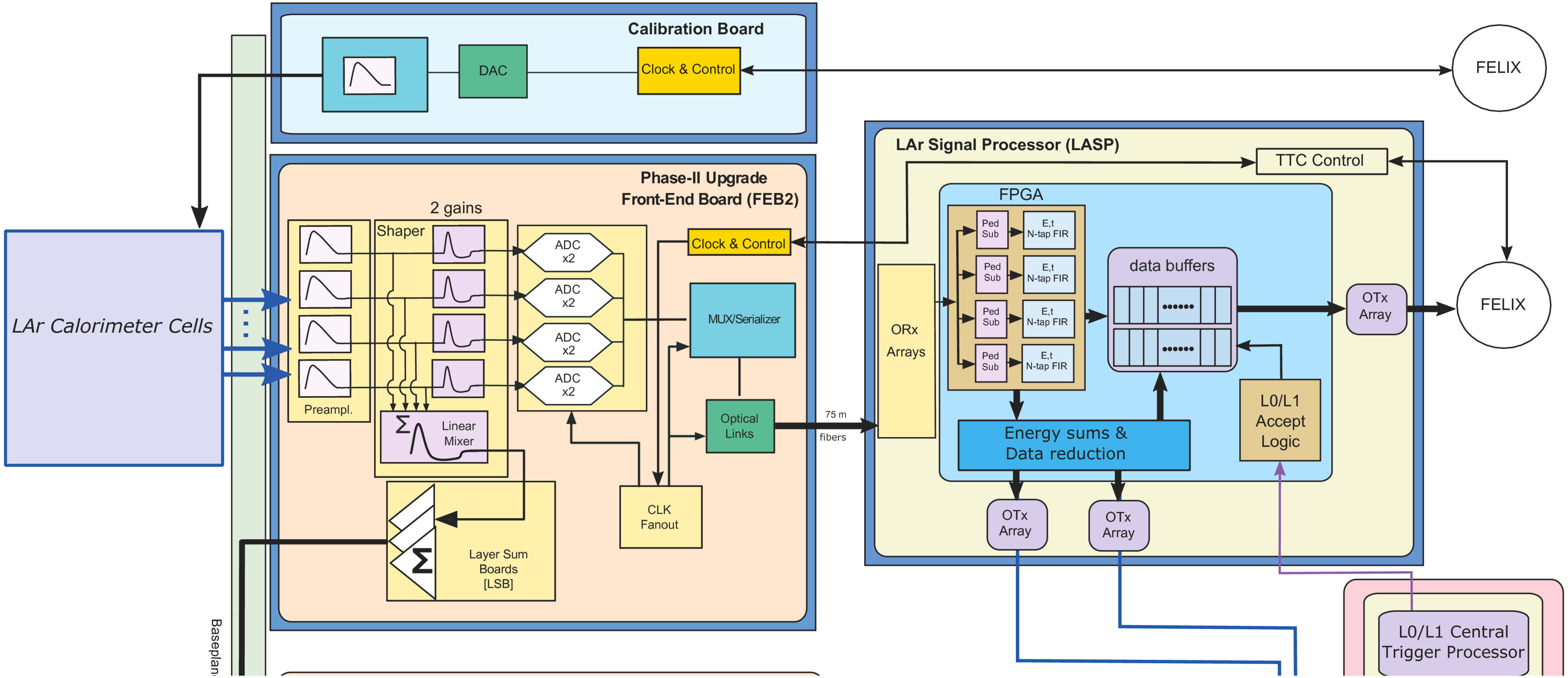
2. LASP (LAr Signal Processor)

LASP, **built on an FPGA,** will then

- ✴ calculate energy/time of pulses
- ✴ transmit data to the trigger & DAQ
- ✴ Buffer data until trigger decision

THE NEED FOR AN INJECTOR

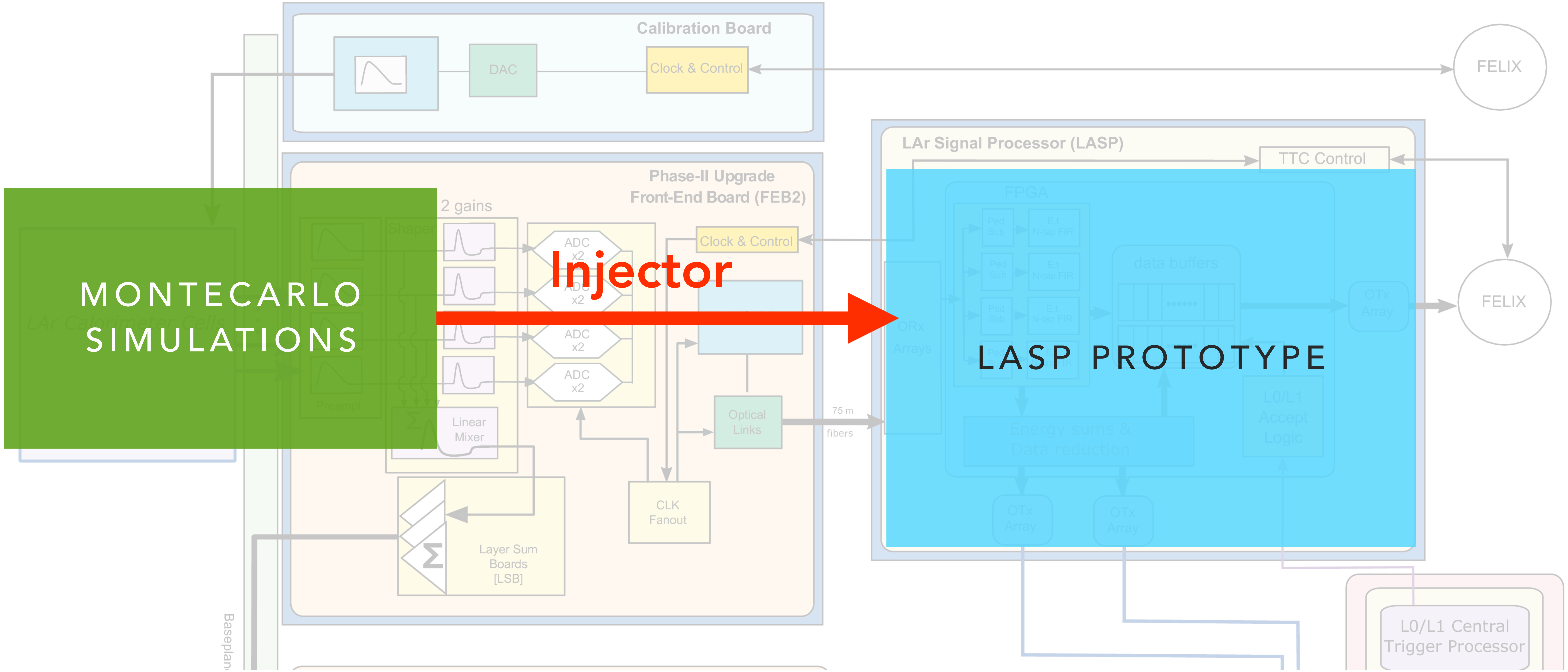
FIG 3: SCHEMATIC OF THE PHASE II UPGRADE (**CROPPED**) [2]



- Signals from the calorimeter and the FEB2 will not be available as the LASP is developed
- Montecarlo simulations can mimic FEB2 pulses for different physics events
- As the LASP is being developed, it needs to be tested with external test cases to verify operation.

THE NEED FOR AN INJECTOR

FIG 3: SCHEMATIC OF THE PHASE II UPGRADE **(CROPPED)** [2]



- As the LASP is being developed, it needs to be tested by external test cases to verify operation.
- Thus, we need a data injector that will input pulses similar to those expected from the FEB2s

REQUIREMENTS FOR THE INJECTOR

- The Injector project is an integral part of the LASP test-bench.

SPECIFICATION (SUMMARIZED)

"The data injector shall provide, with the **highest fidelity**, **22 channels** of **lpGBT payloads** transmitted at **10.24 Gbps** every **40 MHz**. The payload should be **user-controlled** which can help test the LASP for different cases. Data injection should occur for **as long as possible**"

➡ **Highest fidelity:** Ability to maintain transmission accuracy

➡ **22 channels**: 22 independent streams of data

➡ **lpGBT payloads**: payload structure as transmitted by FEB2s i.e. 12 ADCs + 2 BCIDs

➡ **10.24 Gpbs**: lpGBT transmission speed

➡ **40 MHz:** Bunch crossing frequency of LHC

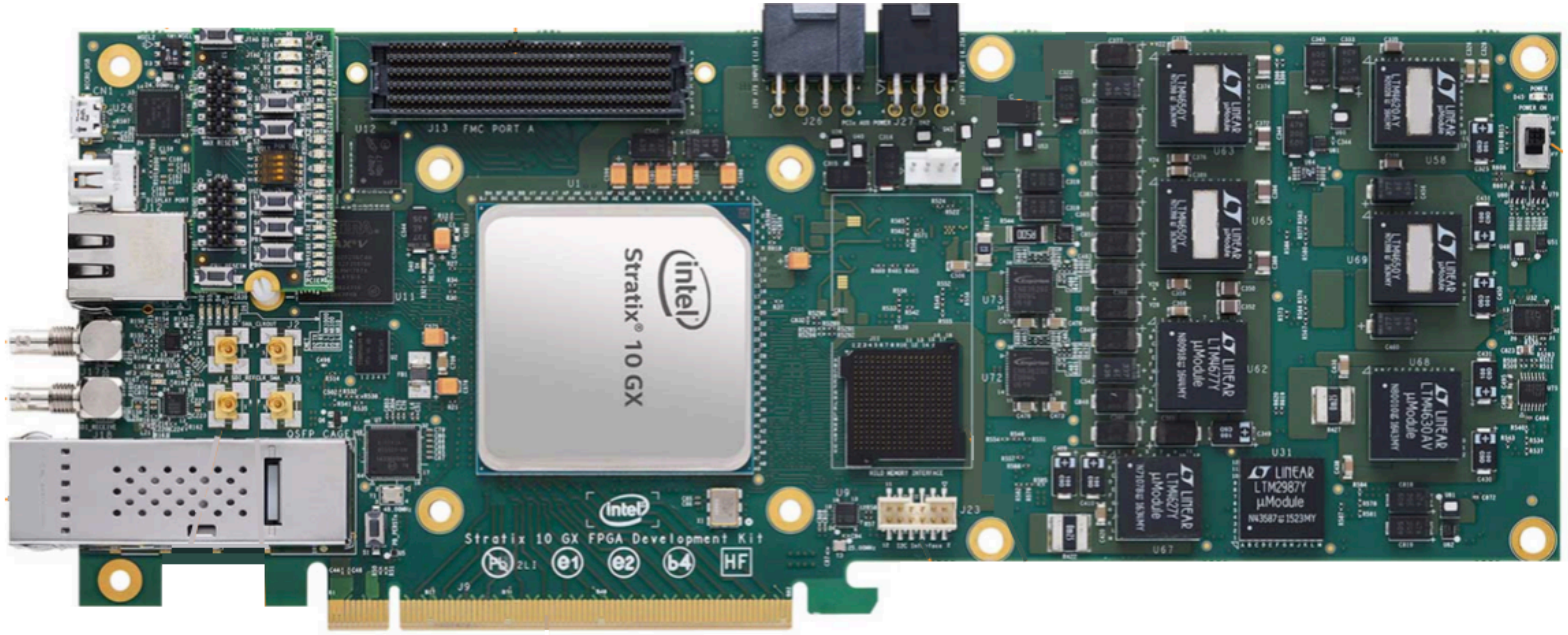
➡ **User-controlled**: user having the ability to manipulate the values

➡ **As long as possible**: duration of injection

FPGAs

- The Injector (and the LASP) is built on a firmware programmable integrated circuit called an **FPGA** (Field Programmable Gate Array)
- FPGA devices contain logic cells and programmable switches. Logic cells can be programmed to perform functions, while the programmable switches can be customized to provide interconnections between logic cells.
- The Injector is implemented on an Intel Stratix 10 GX FPGA board

FIG 4: FRONTAL IMAGE OF THE INTEL STRATIX 10 GX BOARD [3]



The Stratix 10 board has the following capabilities which are exploited for the Injector project

✓ **40 Gbps QSFP transceivers**

✓ **1 Gbps Ethernet connector**

✓ **2 GB external memory device**

DESIGN SCHEME & IMPLEMENTATION

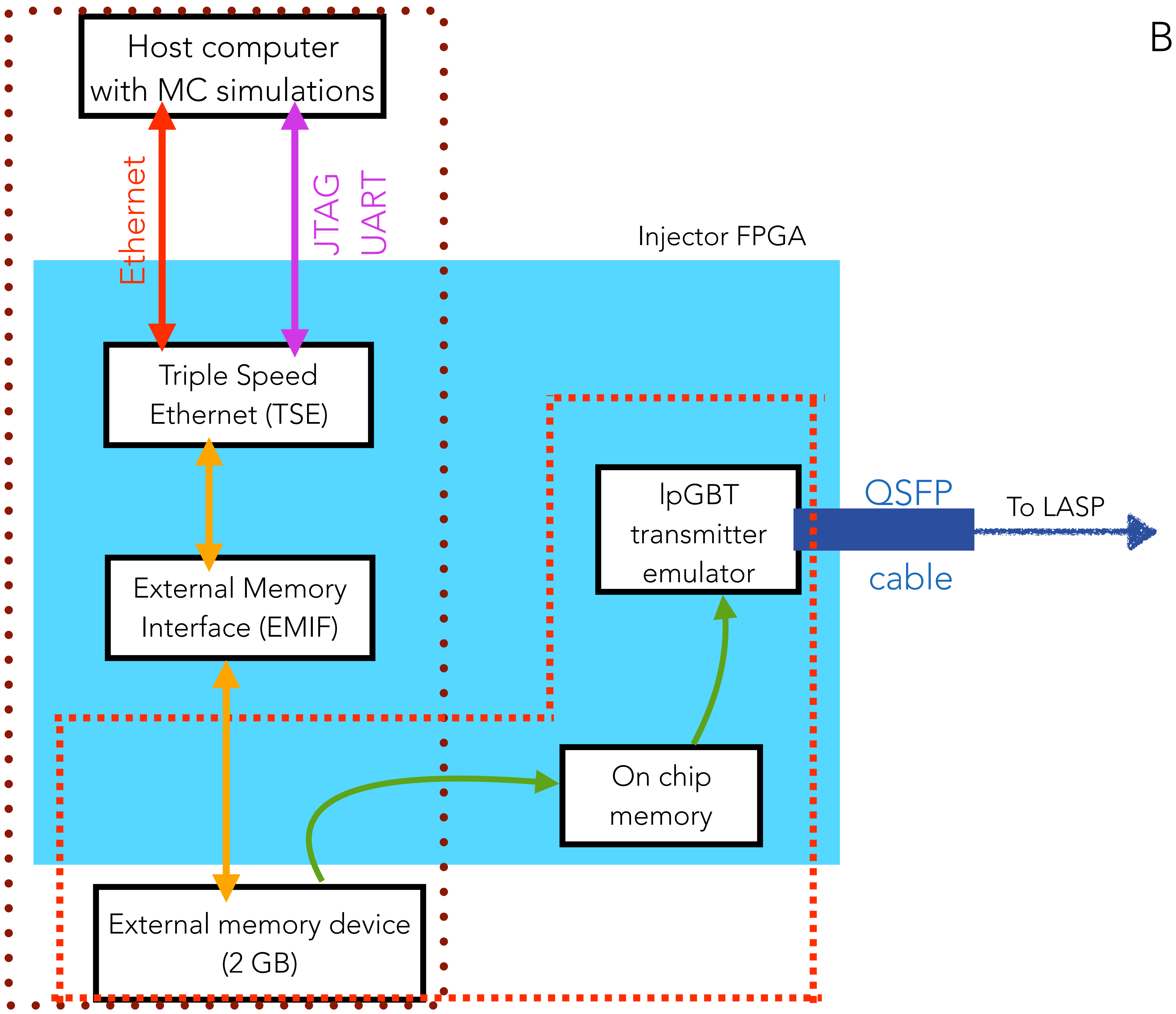


FIG 5: OVERVIEW OF INJECTOR DESIGN

Broken down into two stages:

1. Transfer data from PC into storage via Ethernet using the UDP/IP protocol
2. Retrieval of data from storage. Packaging of data in a format that replicates the FEB2 payload

- ☑ The injector monitors incoming Ethernet frames and strips it down to provide a UDP payload only
- ☑ As a consequence, the Injector "lives" inside an Ethernet network
- ☑ Data sent from the Ethernet is then stored in a 2GB External memory device.
- ☑ Once all 2GB of data is stored, the contents are retrieved, packaged and are sent to the LASP
- ☑ Injection of contents can also be done manually
- ☑ Injection of contents continues until user intervention

ETHERNET DATA TRANSFER

- Using a packet sniffer (e.g. Wireshark), one can intercept and monitor the traffic across a particular network.
- The injector is tested by connecting it to a moderately busy campus network switch. The workstation sending the data is connected to the *same* network switch.
- Dumping of contents received by the injector show that all the ethernet packets are transferred correctly

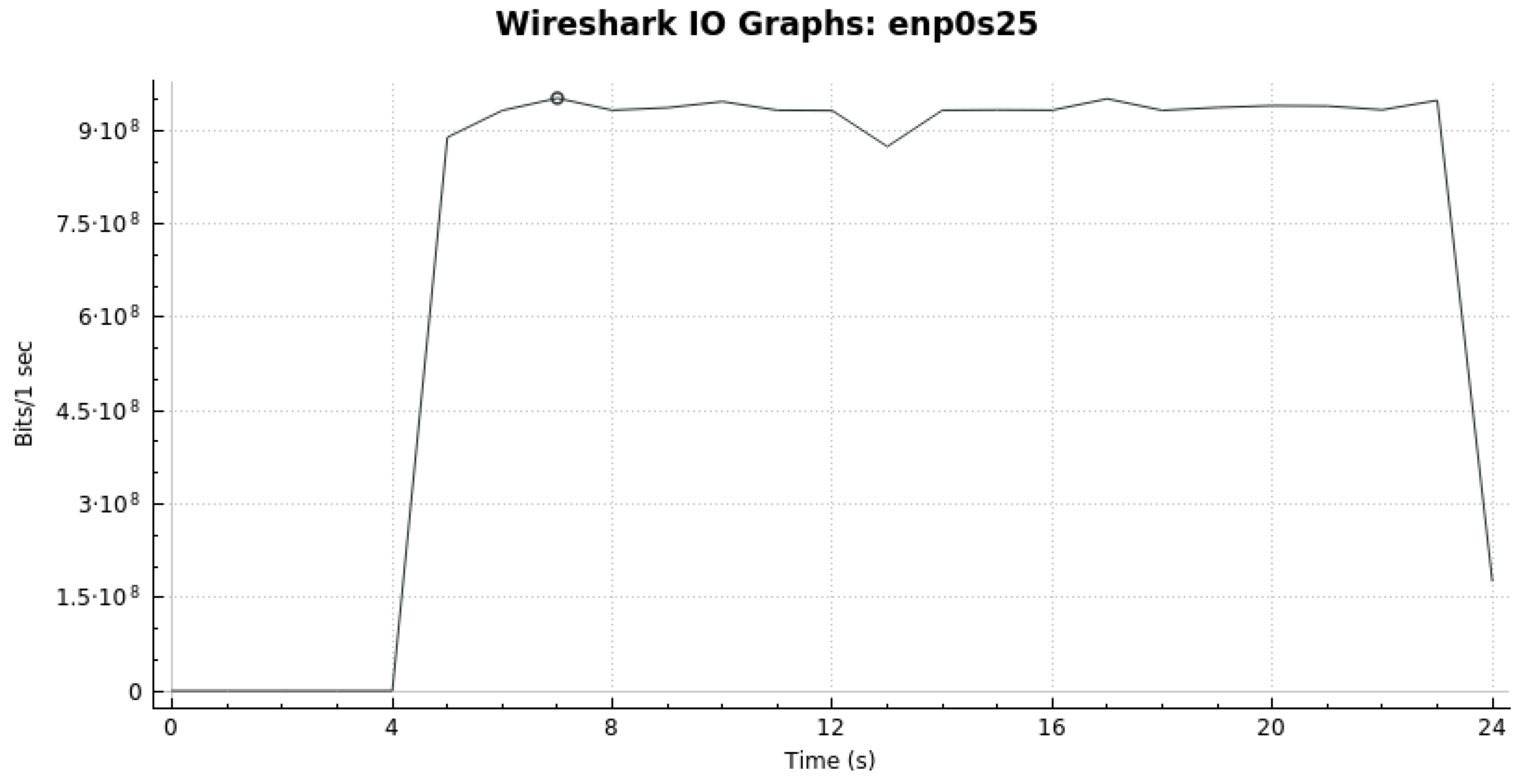


FIG 6: DATA TRANSMISSION SPEED AS MONITORED BY AN ETHERNET PACKET SNIFFER

The Ethernet throughput is measured @ ~930Mbps **i.e. takes ~18s to send 2GB**

This is at the limit of the GbE protocol.

DATA INJECTION TO LASP

- Signals inside the FPGA can be probed and measured - somewhat like an oscilloscope.
- To verify the injection, the signals received by the LASP are monitored and are confirmed to be the same as sent by the injector. Additionally, a simple checksum is sent with every payload and recalculated at the receiving end to verify transmission accuracy
- The incoming signal from the injector as well as the error counter (checksum verification) is probed continuously.

Normal sequence

Whilst looping

Last 16 bit word = FFFF

Transmission accuracy = 100%*

* The checksum will not be able to detect a flipping of an odd number of bits.
The lpGBT protocol has advanced correction features (e.g FEC) which ensures the integrity of data transmission

CONCLUSIONS

- The Injector project is designed and built and is now being used within the LASP firmware community.

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"The data injector shall provide, with the **highest fidelity**, **22 channels** of **lpGBT payloads** transmitted at **10.24 Gbps** every **40 MHz**. The payload should be **user-controlled** which can help test the LASP for different cases. Data injection should occur for **as long as possible**"

➡ **Highest fidelity:** 100% transmission accuracy

➡ **22 channels**: Only 4 channels implemented (limited by FPGA hardware)

➡ **lpGBT payloads**: 12 ADCs are extracted from the memory device …

➡ **10.24 Gpbs**: … and are transmitted at the lpGBT speeds …

➡ **40 MHz:** … every 25 ns.

➡ **User-controlled**: 2 GB of user-defined data

➡ **As long as possible**: for an indefinite period

THANK YOU!

YOUR QUESTIONS/COMMENTS ARE MOST APPRECIATED

SPECIAL MENTION 👏🙏

This work has been made possible by the very gracious help and support of the following people

- My supervisors - **Prof. R. Keeler** and **Prof. R. McPherson**
- **Dr. Sam de Jong** and the **whole LASP Firmware group**

REFERENCES

(1) Project schedule of LHC/HL-LHC plan
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(2) The ATLAS Collaboration. ATLAS Liquid Argon Calorimeter Phase-II Upgrade Technical Design Report, 2018

(3) Intel Corp. Intel Stratix 10 GX FPGA Development Kit User Guide, 2019