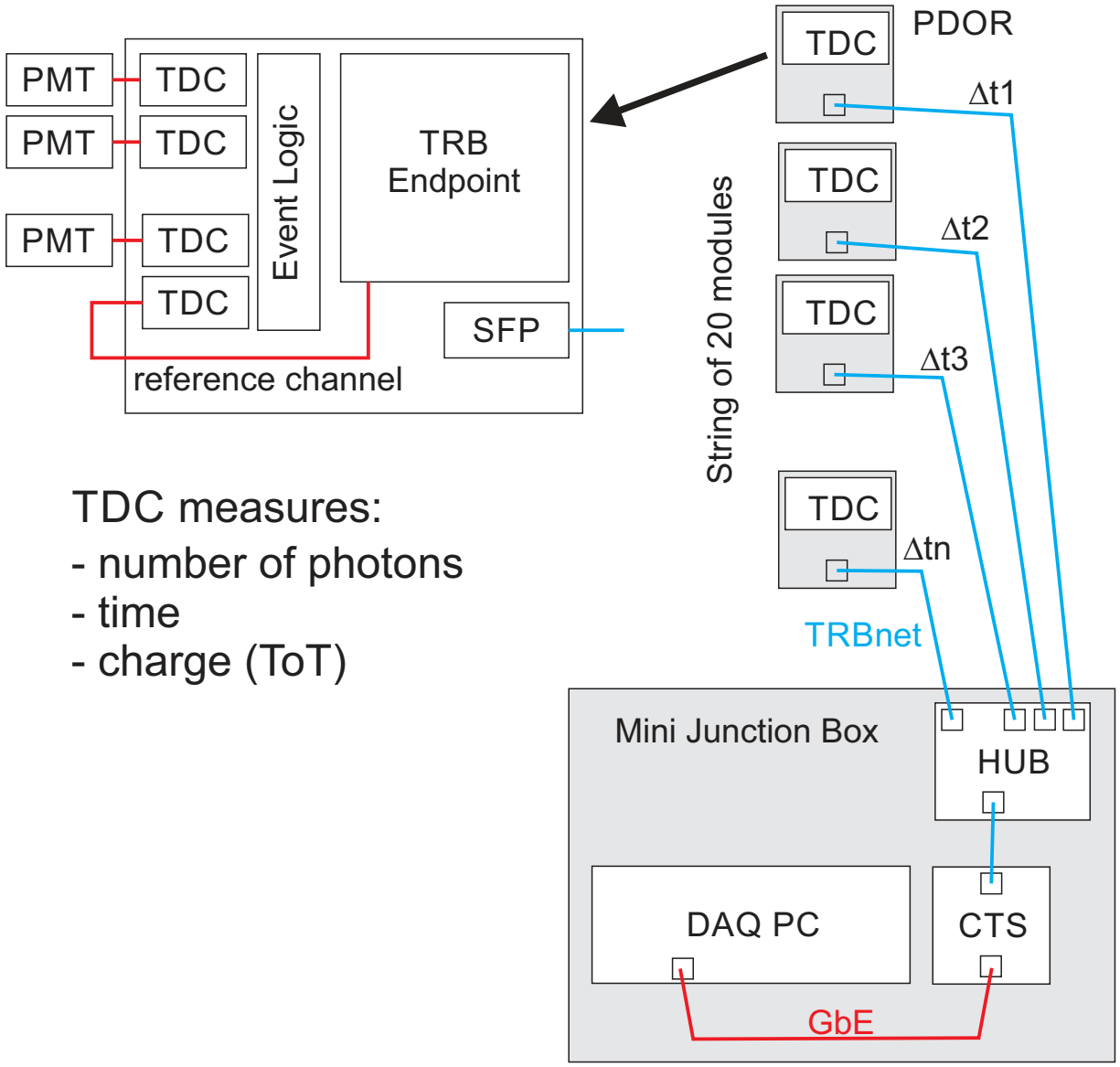
TRBnet in P-ONE

A short introduction

Contents

Structure of P-ONE



TDC measures:
- number of photons
- time
- charge (ToT)

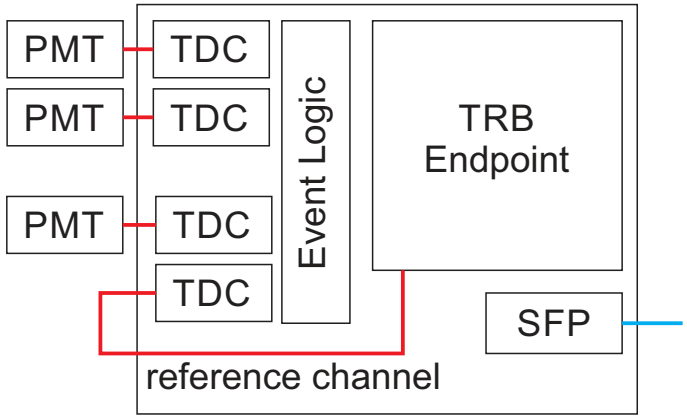
Structure
- one string
- 20 PDORs with PMTs
- one Mini Junction Box

PDOR
- FPGA with
  - several TDCs
  - TRBnet endpoint
  - event logic
- SFP for fiber comm

Reference time needed!

Different delays due to cable lengths in string to be taken care of

Syncing several TDCs

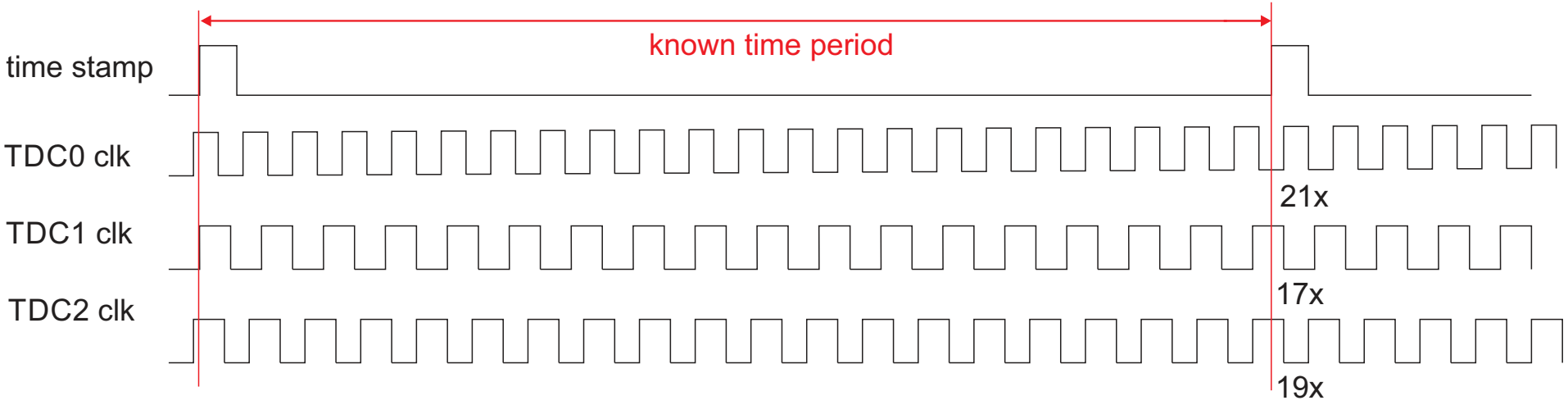


FPGA TDCs in a nutshell

- one local 200MHz clock defines timing
- this clock is different on all boards (ppm level)
- one clock cycle defines „coarse time“ unit
- TDC time bins are different on all boards

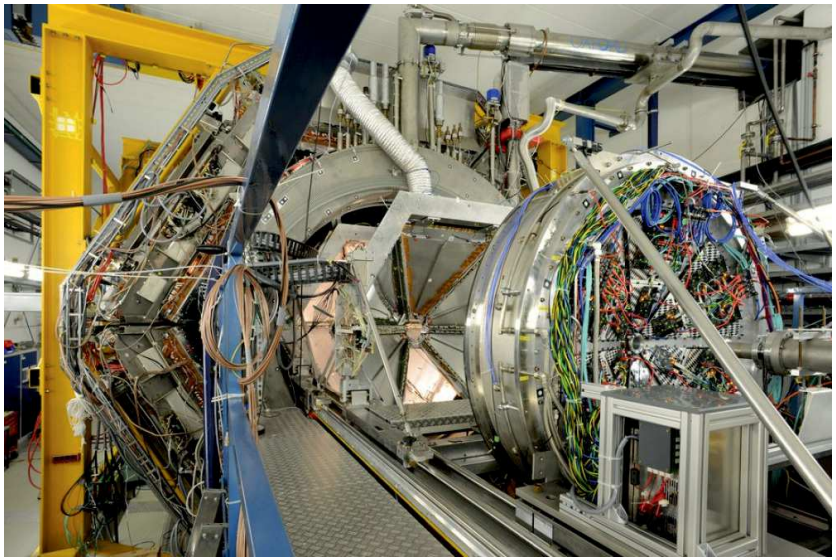
Solution

- one dedicated TDC channel as reference
- centrally distributed time stamp defines timing
- local clocks can be calibrated

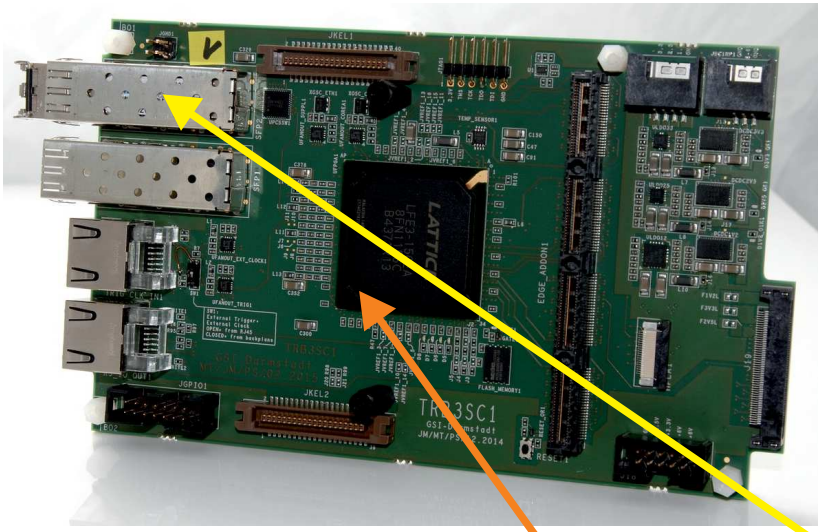


What is TRBnet?

- synchronous, fiber based protocol
- focus on low latency and defined Quality Of Service
- open source, open hardware
- development started in 2005
- successor of Gen1 HADES experiment readout
- full set of tested software available (slow control, readout, unpackers)
- online data analysis and display (DABC)
- FPGA based TDCs available
- support from GSI (Michael Traxler, boards and software)
- used in many experiments for years now (STRAWb :)
- FPGA code as „block“ for implementation
- scalable by design
- triggered system
- supports free running endpoint (like TDCs)



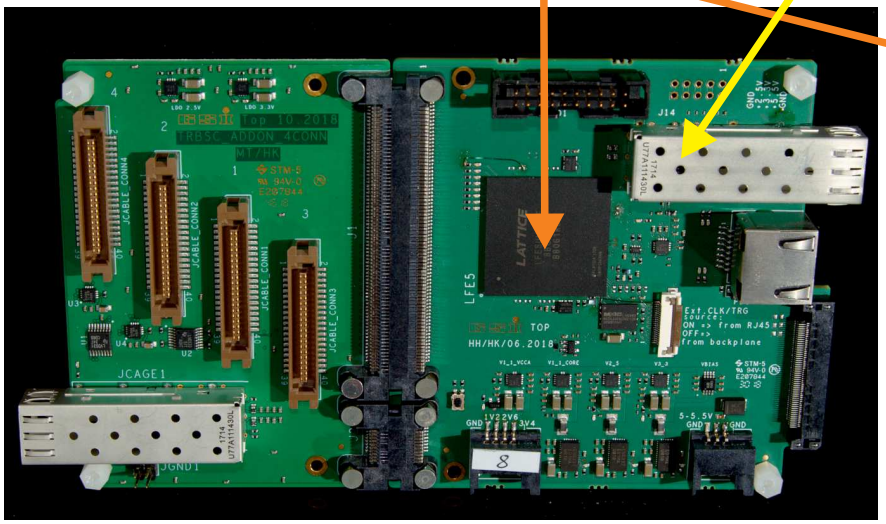
TRBnet - as hardware module

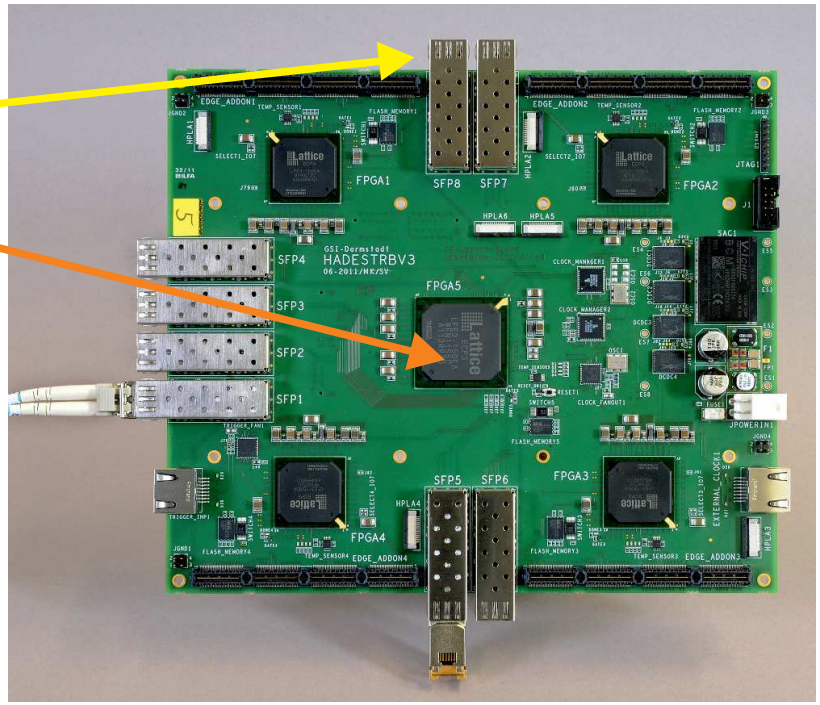


Many boards already available:

- TRB3sc used in STRAW(b)
- TRB3 as multichannel system
- TRB5sc low power version
- many addons

common to all: FPGA + SFP



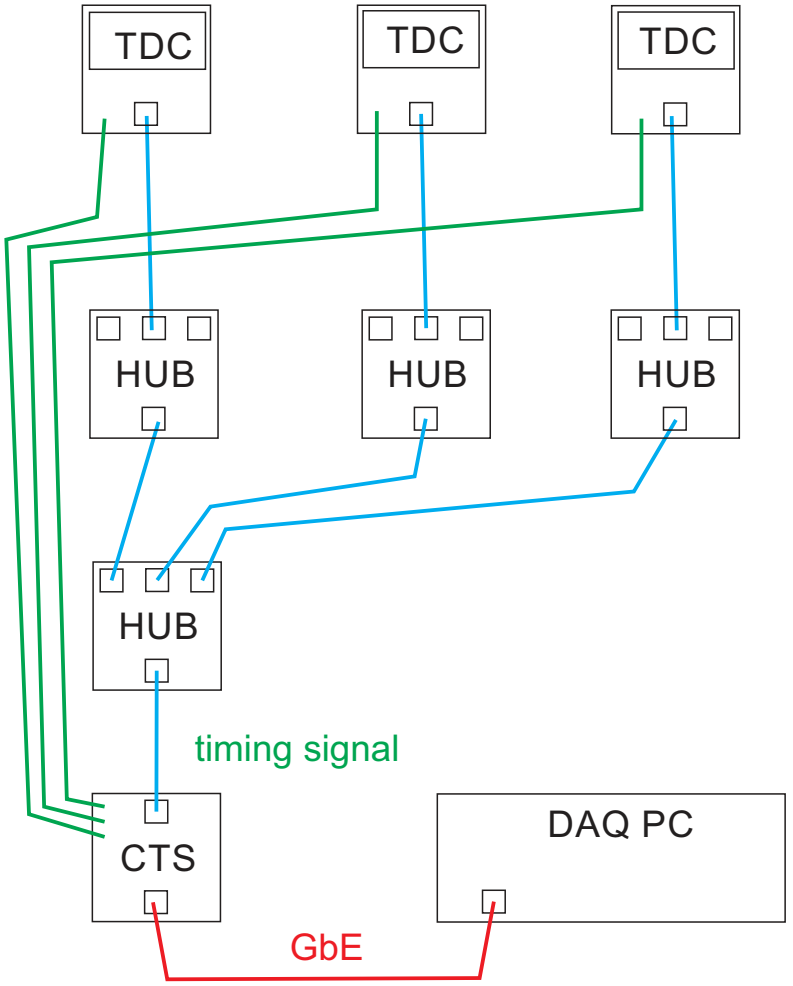


Basic features ...

- Star topology
- point-to-point connections
- four virtual channels on fiber
- request-answer on channels
- Central Trigger System (CTS)
- all action initiated by CTS
- CTS as trigger and timing distribution (reference time for TDCs)
- data transport by TRBnet
- data forwarding by GbE

Timing is done by copper!

Not feasible for P-ONE:
- length
- signal integrity
- connectors



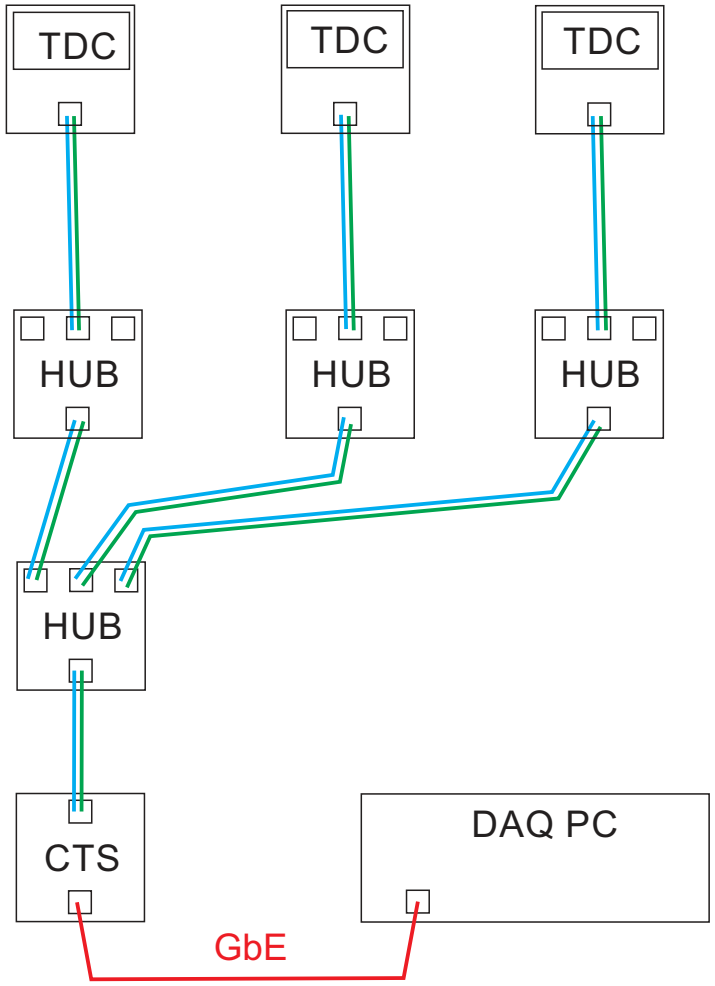
... and necessary changes

One necessary change:

integrate analog timing into digital fiber

Why not done already?

So let‘s get into the rabbit‘s hole...



The SerDes business

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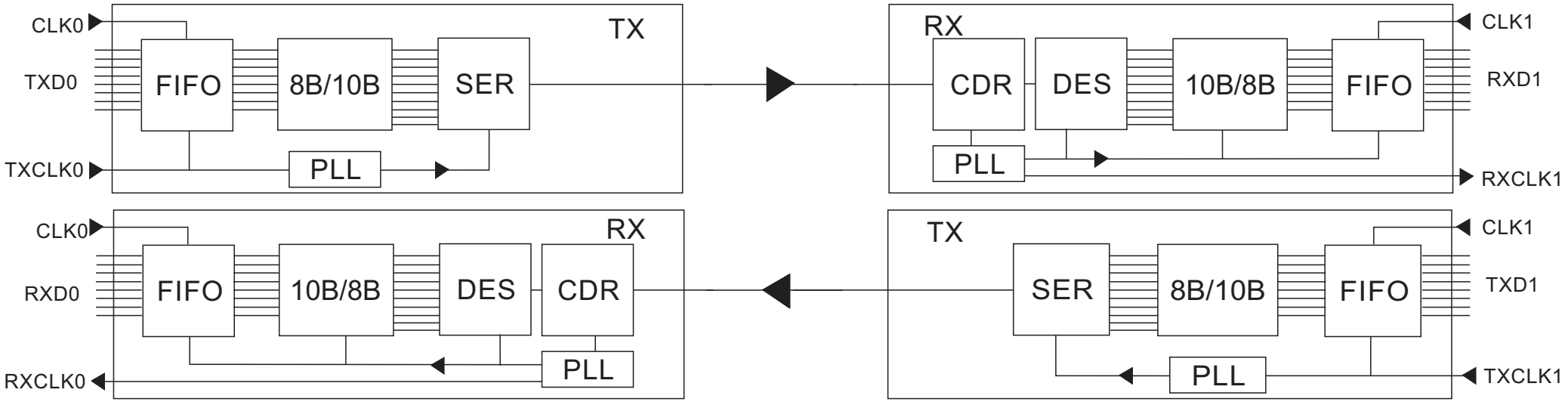
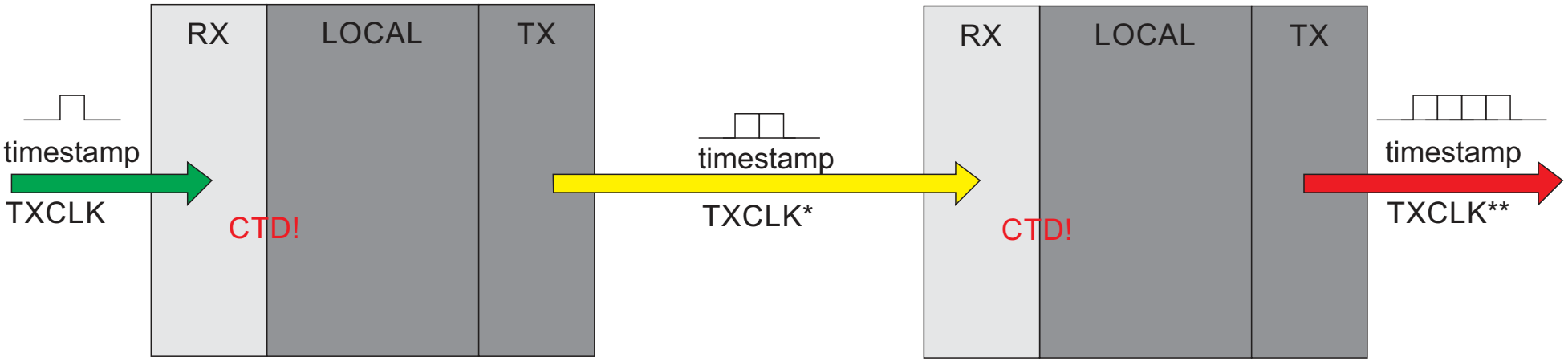


TRBnet: TXCLK = 200MHz (5ns), Fiber clock = 2GHz (500ps)

on TX: TXCLK is embedded in outgoing data stream
on RX: clock is recovered from incoming data stream
exact clock copy of TX available on RX, with unknown phase
delay on fiber media is unknown
problem: 10 possible bit positions in CDR
problem: from SerDes to SerDes, we need to do Clock Domain Transfer

result: per layer of hubs, we have one clock cycle jitter + bit jitter!

New clocks everywhere...



First FPGA

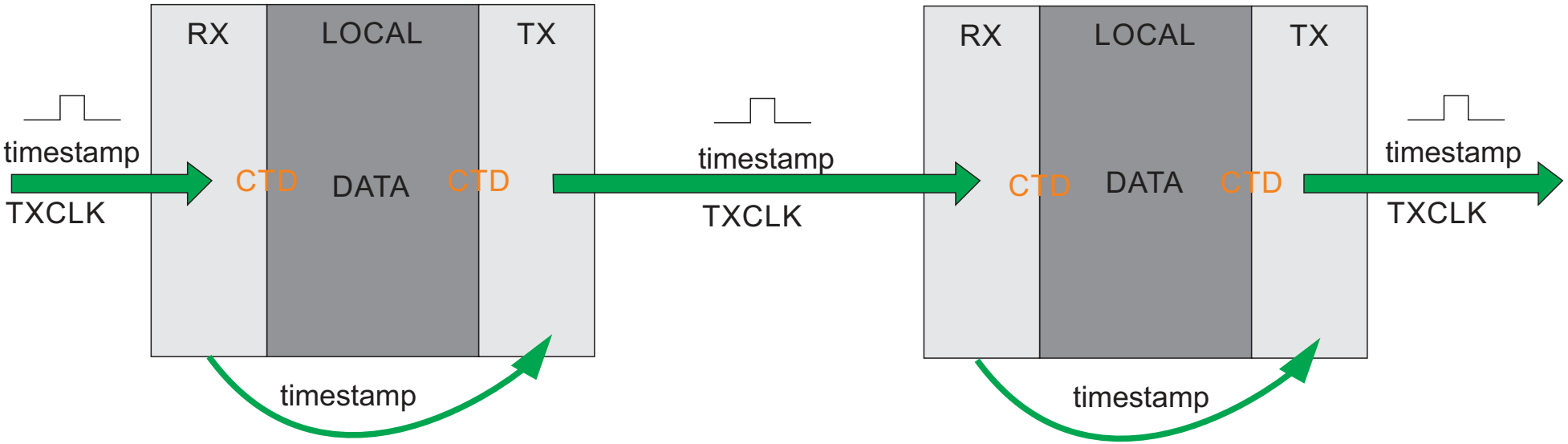
- clock domain transfer from RX to local clock
- local clock used as new TX clock
- local clock not the same as RX clock (drift, frequency, jitter)

Second FPGA

- same game...

Initial TX clock lost, replaced by new clocks + clock cycle jitter due to CTD!

Distributing the clock differently



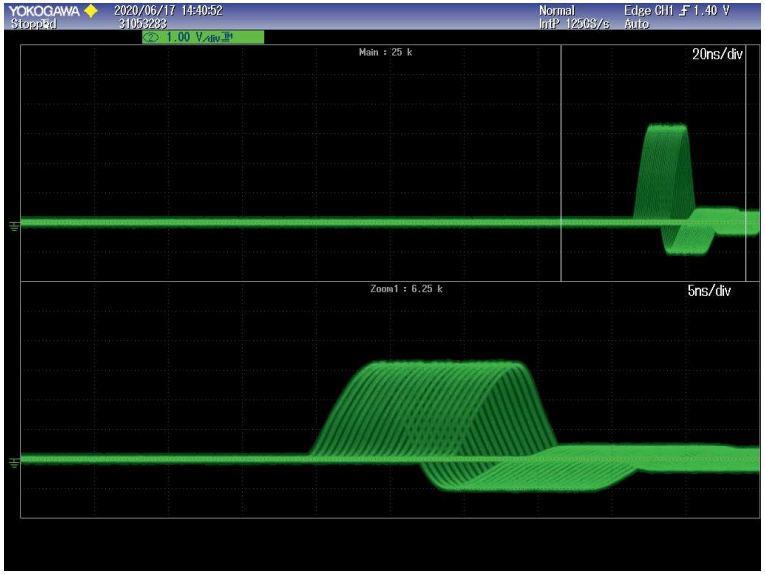
Some changes

- received clock is routed to TX part
- timestamps are routed same way
- data is routed through fabric by CTD (latency)

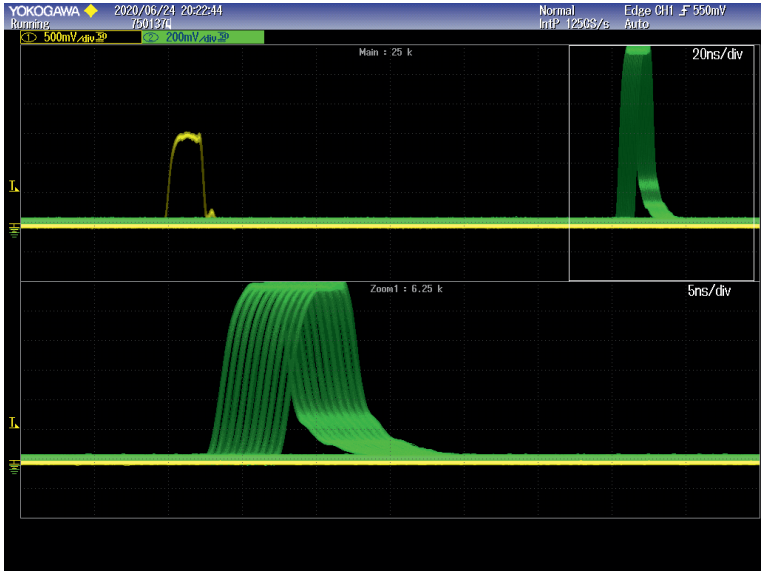
Link establishment

- from inner to outer parts
- keep links up whenever possible

... working around works :)



20x bit jitter



10x bit jitter

Test system:
- TRB3sc CTS
- 2x TRB3sc Hub
- TRB5sc endpoint

~120ps!

only clock jitter

Measuring the fiber delay (I)

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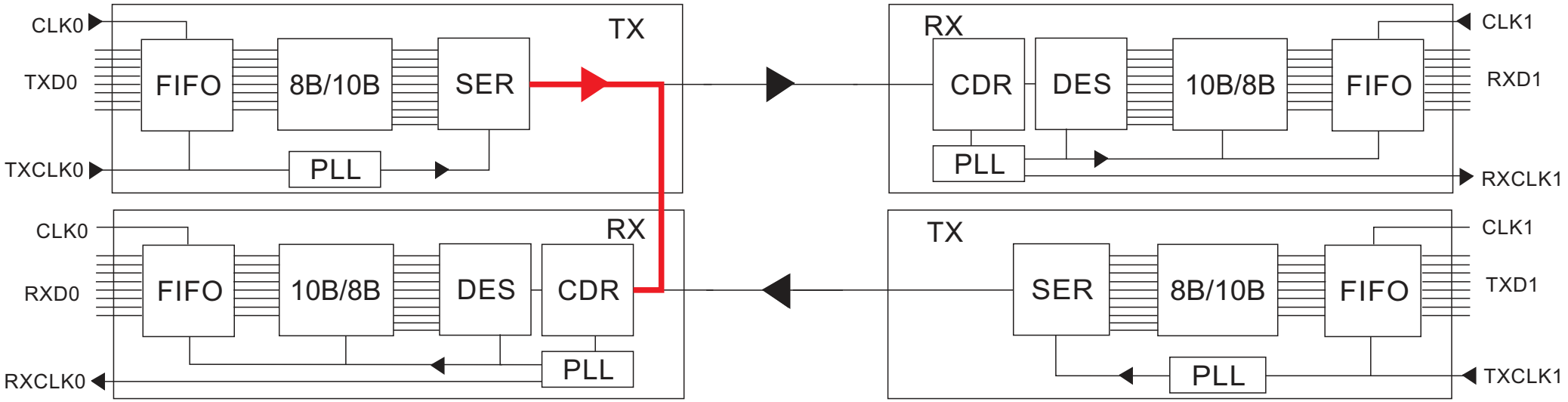
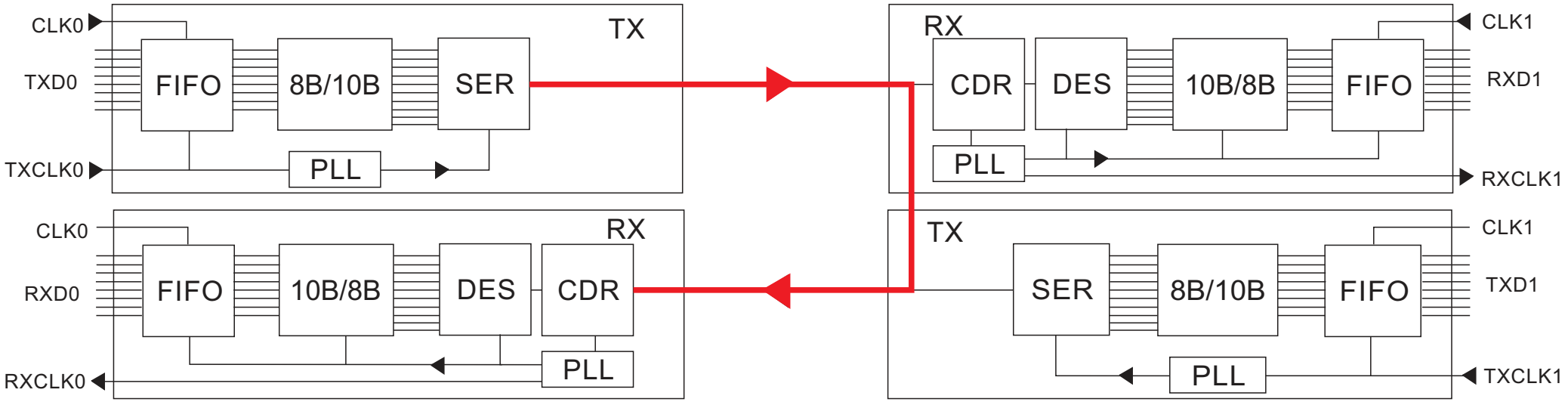


Local analog feedback in uplink SerDes
- timestamp is internally returned
- delay can be measured ($\Delta t1$)
- uplink stays intact

Measuring the fiber delay (II)



Remote analog feedback in downlink SerDes
- timestamp is externally returned
- delay can be measured ($\Delta t2$)
- uplink stays intact

(Fiber + SFP + IO) delay = 0.5 * ($\Delta t2$ - $\Delta t1$)

Can be measured online for all point-to-point connections

Summary and outlook

TRBnet was successfully operated in STRAW(b)

TRBnet can be adjusted to allow precise timing on fiber

Open system allows wide contribution for VHDL code

„Proof of concept“ has been made (quick & dirty):
isochronous operation over two hub layers

Fiber delays can be measured online