Report on Micromegas semi-DHCAL TB in SPS/H4 (11/06 – 08/07)

RD51/WG7 meeting

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Overview

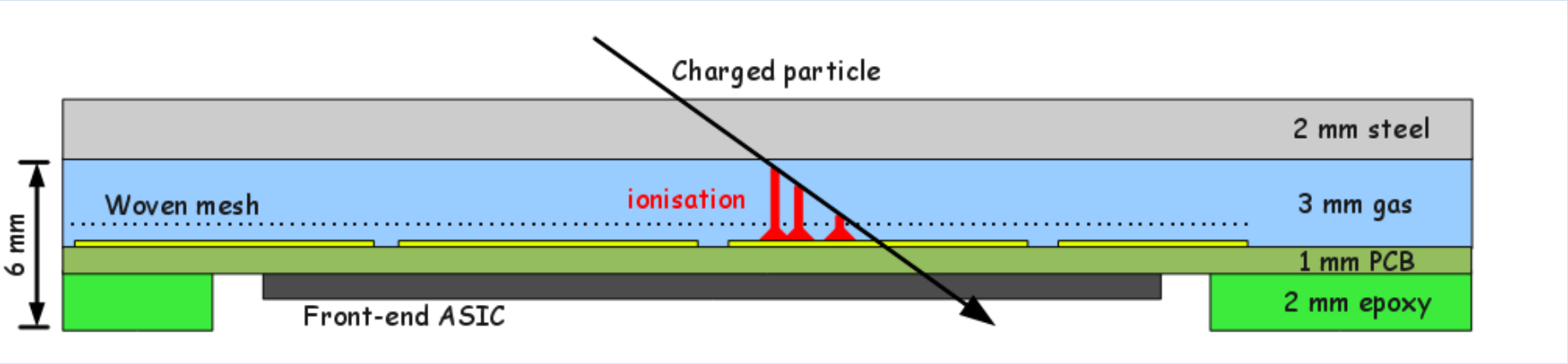
- Micromegas DHCAL project
- Design and assembly of the 1 m2 prototype

- TB plans and setup
- Preliminary results

- Future plans

Micromegas for a semi-DHCAL

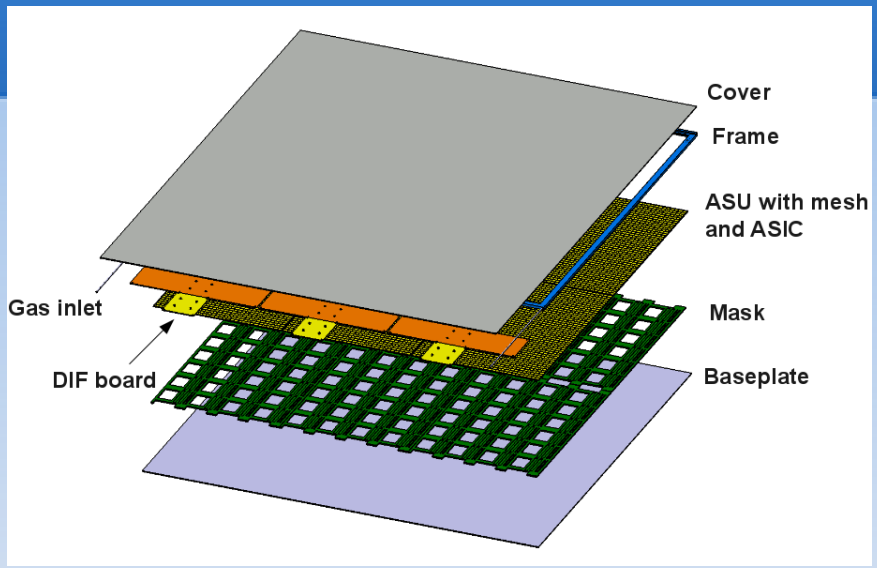
- Embedded front-end chips → thickness of 6 mm:
  2 mm steel cover, 3 mm gas, 3 mm PCB/epoxy
- 1 cm^2 readout pads for Particle Flow Calorimetry
- Proportional amplification mode: semi-digital readout
- Large area (Bulk), ”low” voltages (500 V max), standard gas mix. ...



Micromegas prototypes

- 1st prototypes: 6x16 cm^2 & 12x32 cm^2 with analog readout (GASSIPLEX)
- 2nd prototypes: 8x8 cm^2 & 8x32 cm^2 with embbeded digital chips (DIRAC/HR)
- **3rd prototypes: 32x48 cm^2**
- **4th prototype: 1 m^2**

x 3

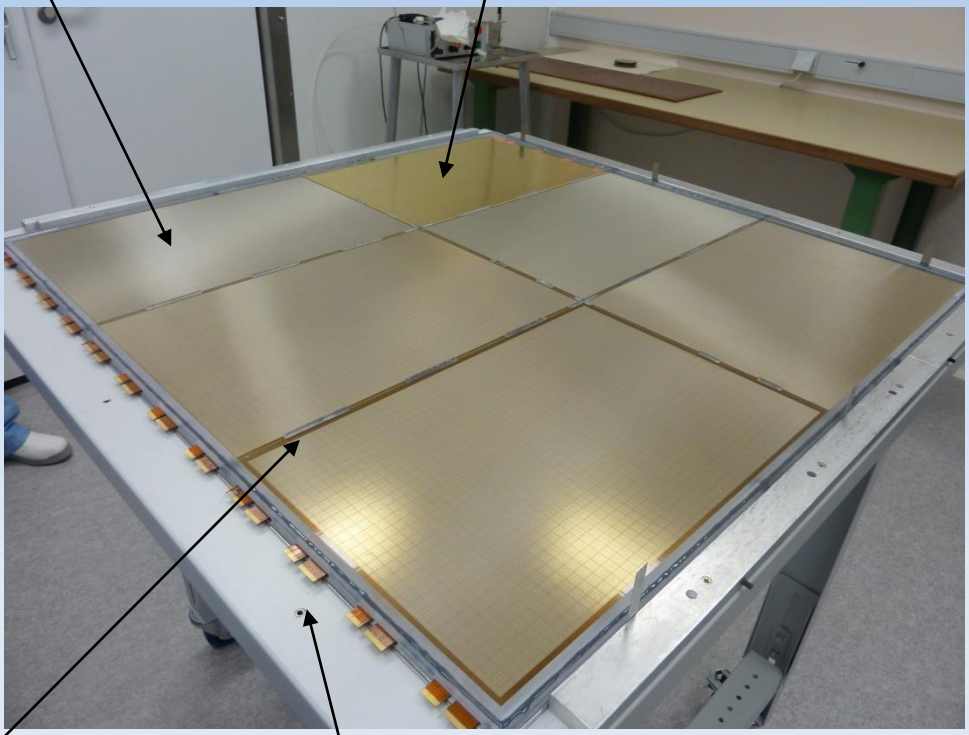


2 chained ASU of 32x48 cm^2 with 24 HARDROCv2 each

Assembly of the 1 m2 prototype

32x48 cm2 ASU pre-tested in gas box

dummy ASU



3 mm thick spacers
dead zone between ASU
= 5 mm (1.6 % in total)

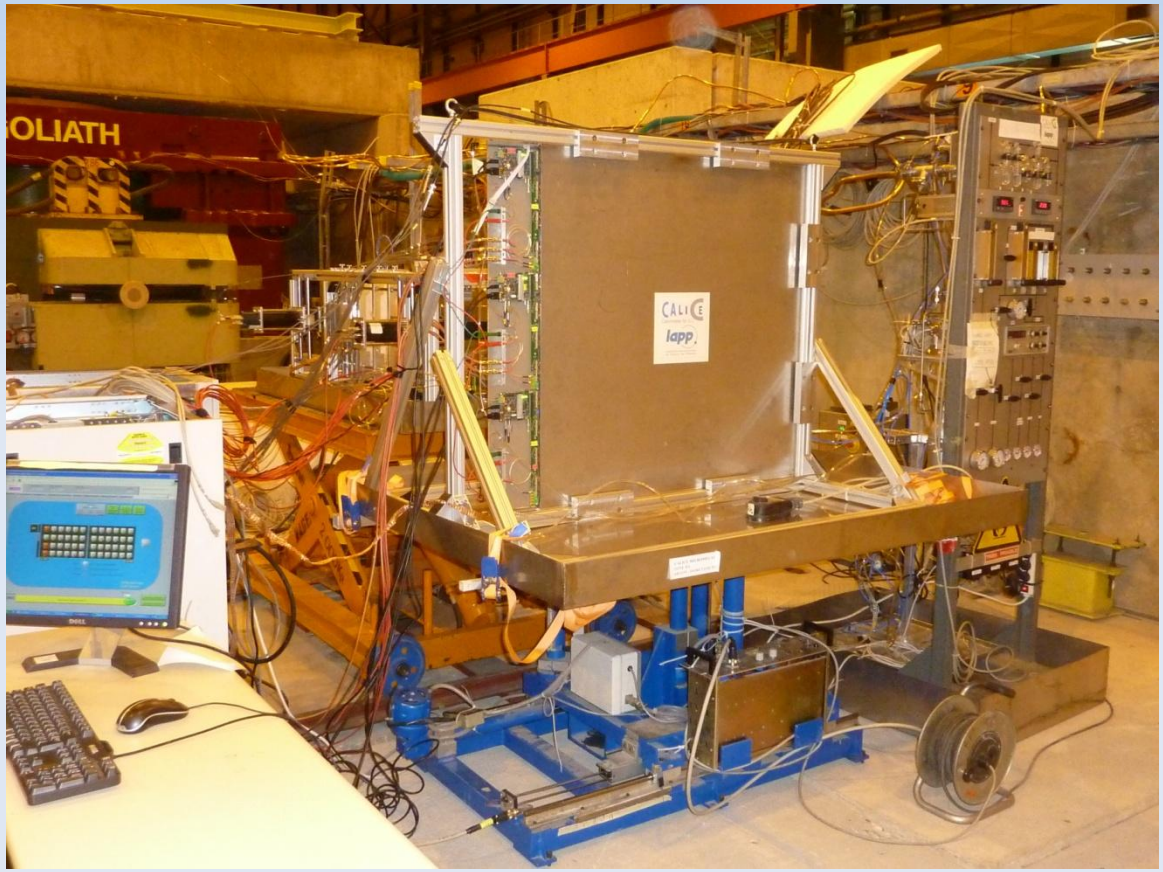
flex cables for readout,
chip config. and mesh HV

TB goals

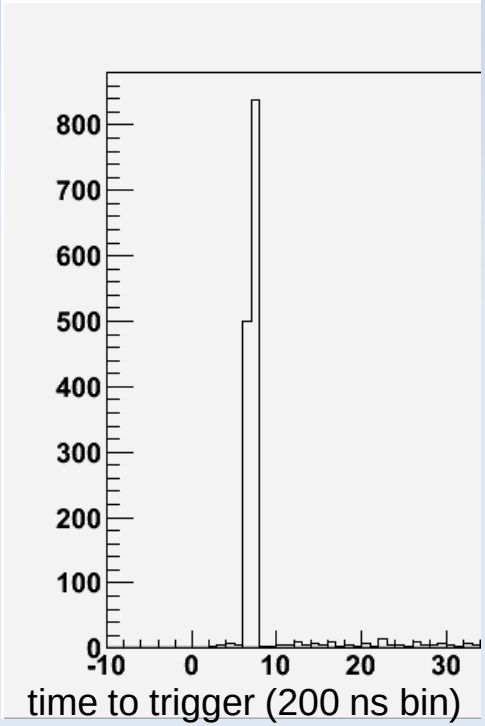
- HARDROC2 circuitry (64 channels, power-pulsing capability)
  - current preamplifier → fast shaper → discri. → memory
  - Shaping time short w.r.t. Micromegas signals
- The m2 prototype efficiency will be low, nevertheless, several technological choices can be validated and unforeseen problems can be found before the next prototype with an optimised electronics (MICROROC)
- TB program
  - Test overall functionality of the detector
  - Reach high gas gains and the lowest detection threshold on chips
  - Measure efficiency and multiplicity uniformity
  - Validate/rule out assembly and technological choices
  - Compare performance with and without power-pulsing of chips

TB setup

- Telescope with 4 Gassiplex chambers and scintillators
- 1 m2 prototype (continuous time-stamping of hits, 128 event depth memory
- Delay of ~1 us between trigger and readout → time to trigger info used to find particle hits
- Use trigger number from 2 acquisitions for merging of events
- Muon beam (150 GeV/c) at an intensity between 100-1000 Hz

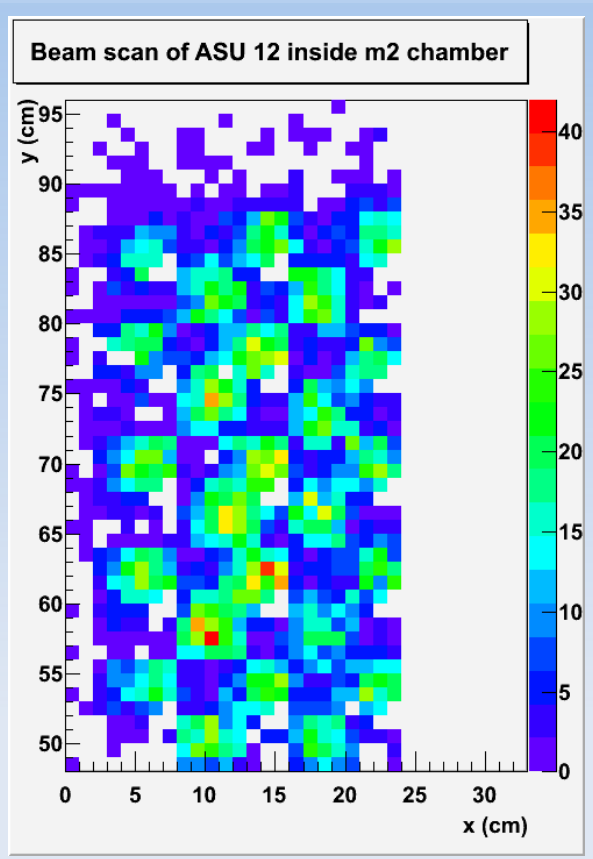


Find hits in m2 chamber with time to trigger distribution

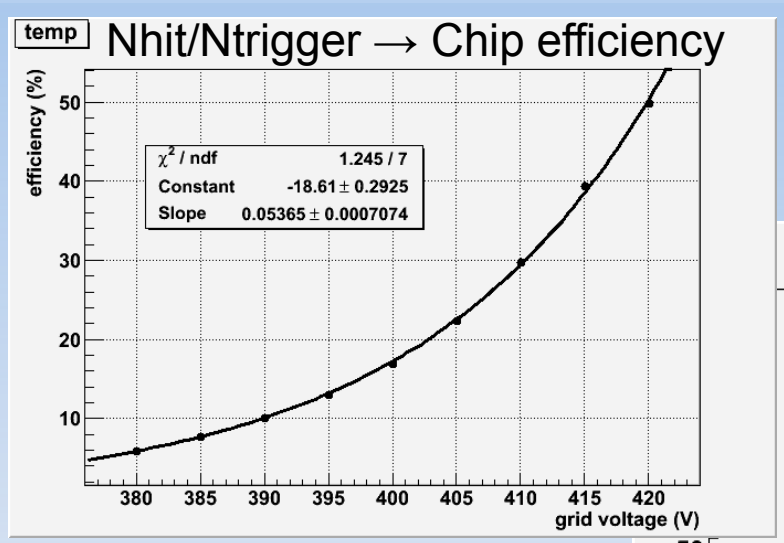


Preliminary plots

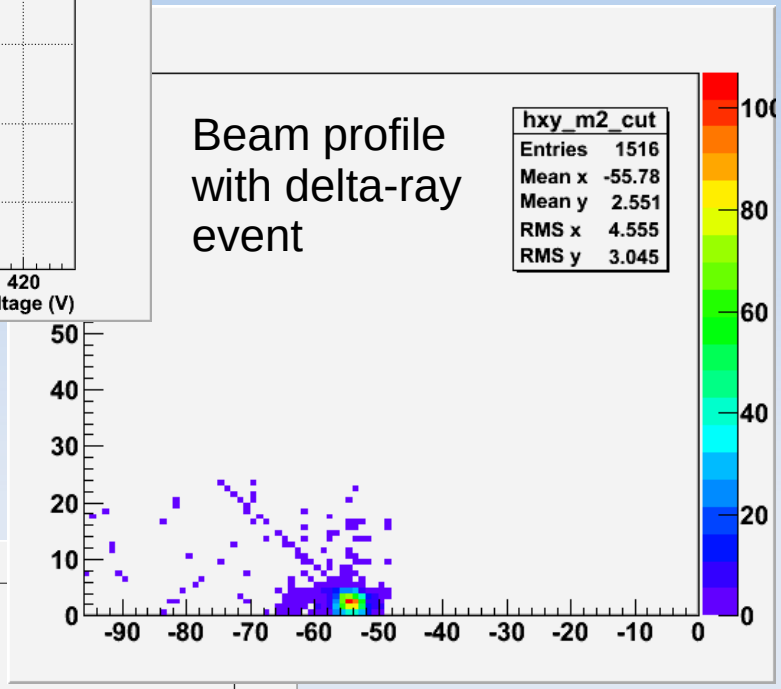
Scan on each chip of 1 ASU

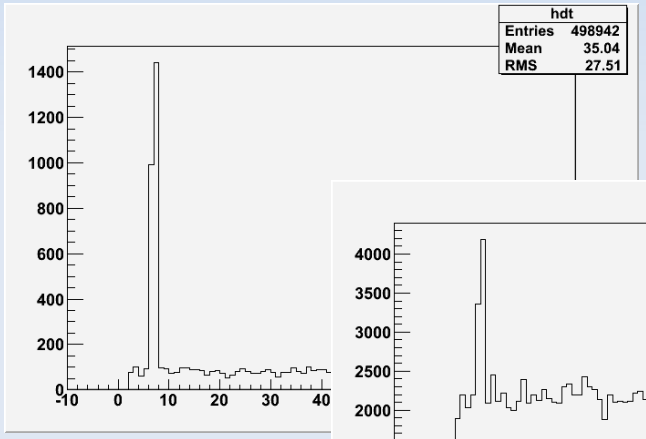


HV study

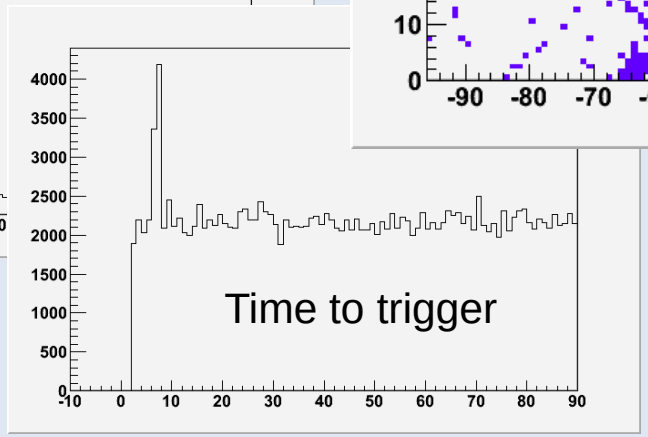


Combined runs with Gassiplex telescope for efficiency scan



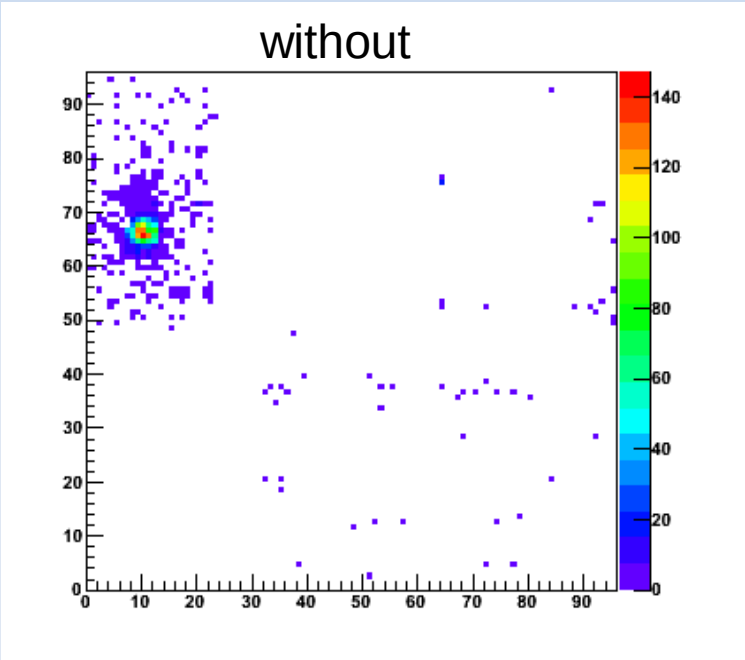


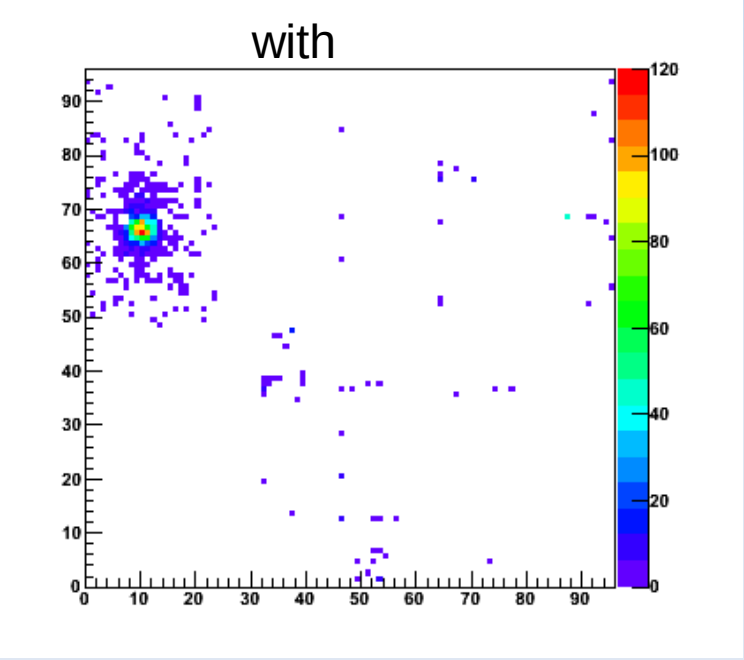
Noise hit rate study



Power pulsing

- Switch ON/OFF the analog part of all chips during SPS spill.
  - this corresponds to a current of ~ 3 A
  - t(ON) = 2 ms and t(OFF) = 10 ms
- S/N ratio are similar
  Quantitative analysis to be done





Conclusion & future plans

- Goal of the 1 m2 prototype TB reached:
  - assembly procedure validated
  - stable running during 1 month (few HV trips)
  - first test of power pulsing realised
  - chip detection threshold minimized
- Data analysis will be focused on uniformity of efficiency and multiplicity
- Precious informations obtained for the next prototypes
- New front-end chip with shaping time matching the detector signal duration (MICROROC) and same digital part as HARDROC (same DAQ): first batch of chips available in September
- Next TB with actual prototype in November in W-CLIC structure