RD53A CALIBRATION

MARCH 2021

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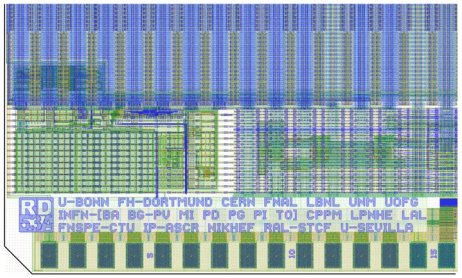
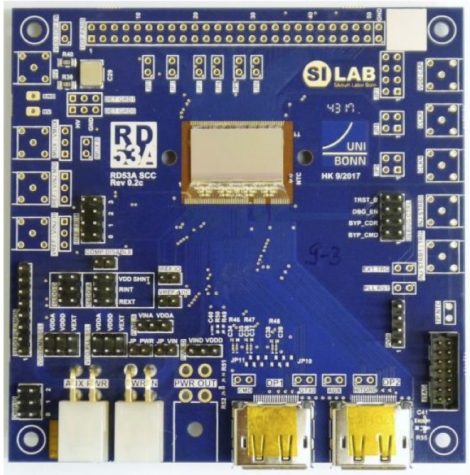
RD53A PIXEL CHIP

RD53A Specifications	
Technology	TSMC 65 nm CMOS
Pixel size	50 × 50 µm²
Chip size	20 × 11.8 mm² Half size of the final CMS chip
Number of pixels	400 × 192 = 76800 Final CMS chip: 432 × 336 = 145152
Detector capacitance	< 100 fF
Leakage current	< 10 nA
(In-time) threshold	(1200e^-) 600e^-
Noise hits	< 10^{-6}
Radiation tolerance	500 Mrad at -12°C
Temperature	[- 40°C; +40°C]





FLOORPLAN

Top test pad

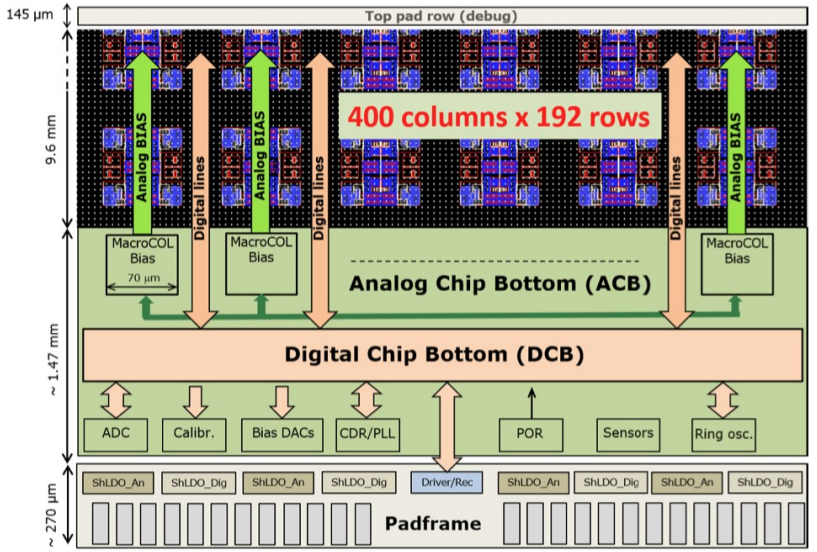
- Row of test pads for debugging purposes
- Will be removed in the production chip

Pixel matrix

- 192 x 400 = 76 800 pixels

Chip Bottom

- all global analog and digital circuitry needed to bias, configure, monitor and readout the chip



RD53A manual:
https://cds.cern.ch/record/2287593/files/%20RD53A_Manual_V3-42.pdf

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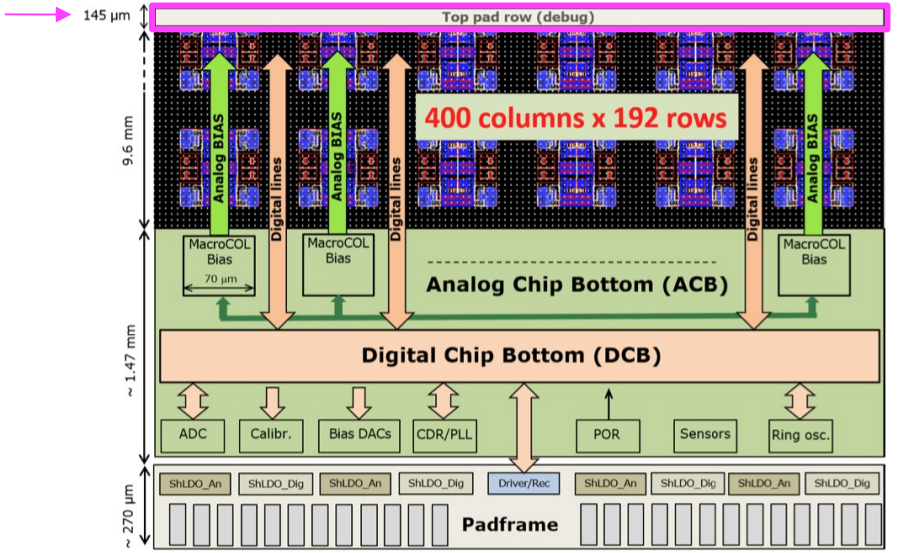

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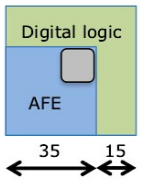

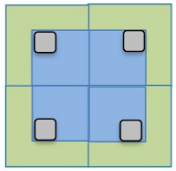

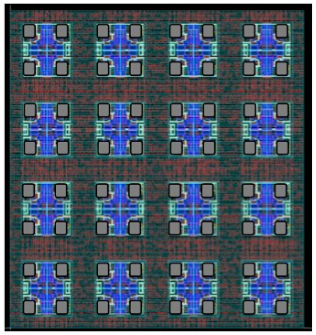

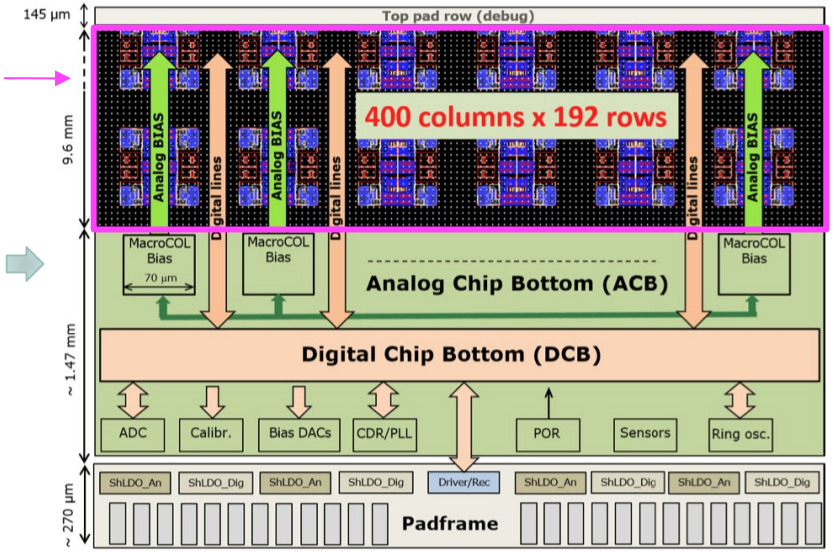

Pixel

50% Analog

50% Digital

+ Bump pad

Analog island

2×2 pixel quad

Pixel core

16 analog islands in a fully synthetized digital sea

Pixel matrix

All cores the same

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FLOORPLAN

Power distribution

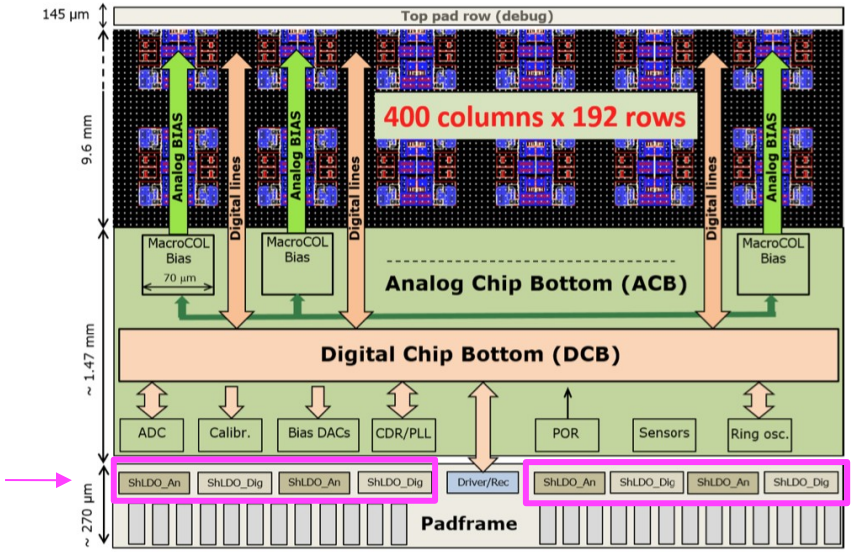
- Power lines distributed from the bottom to the whole chip

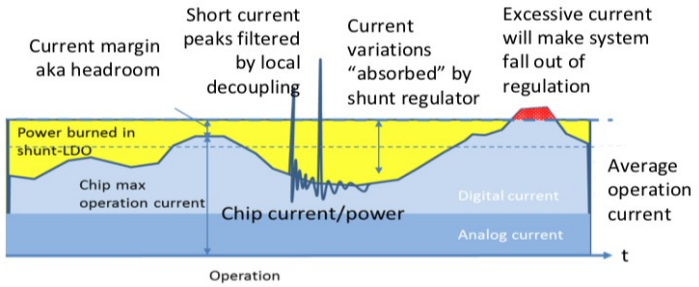
Serial powering

- Baseline powering scheme for CMS and ATLAS
  HL-LHC pixel detectors
- Pixel modules powered in series
  (chips in a module powered in parallel)

Shunt-LDO regulator

- 2 Shunt-LDO regulators
  (1 analog + 1 digital)
- supply **constant input current independent of the load**
- **excess current is shunted to ground** (headroom)





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FLOORPLAN

Analog chip bottom (ACB)

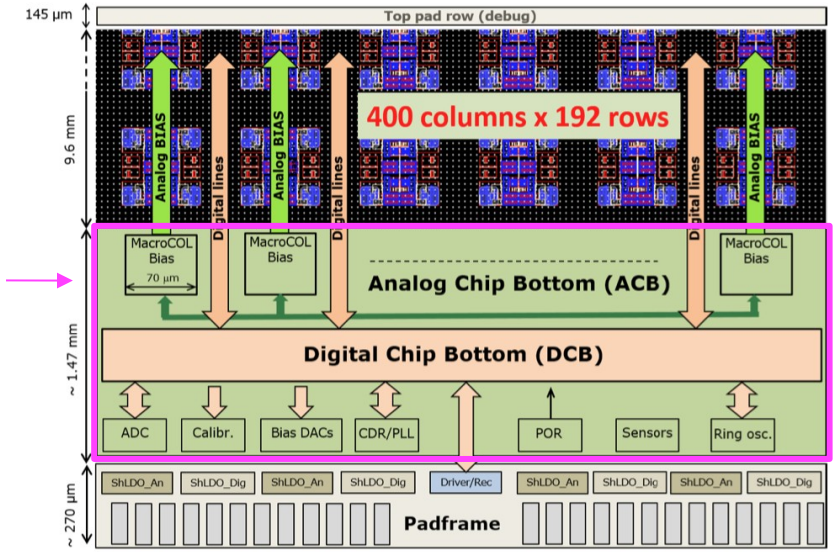
- Providing current reference DACs (I_{ref}) and voltage levels to the calibration injection circuit
- Monitoring: temperature, radiation, currents, voltages
- CDR/PLL recovers data and clock from input stream at 160 Mbps

Digital chip bottom (DCB)

- Control and processing functionalities
- Input, Output and Configuration digital logic

Output Serializer & CML cable drivers

- 4 Aurora lanes at 1.28 Gbps
- CML output driver with programmable pre-emphasis



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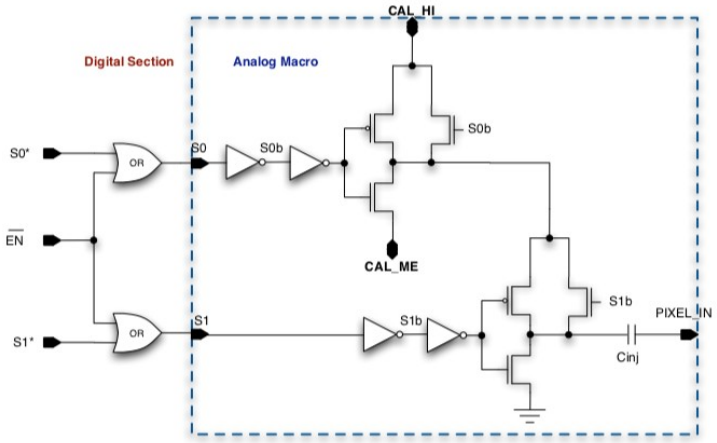
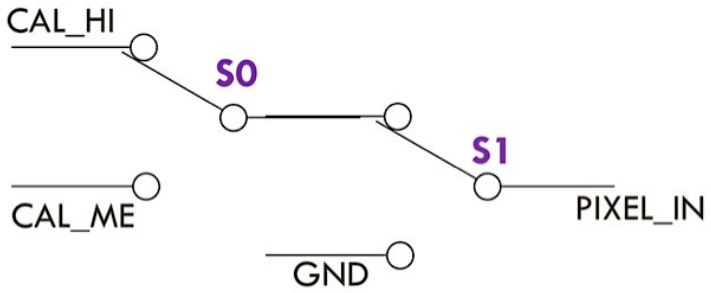
CALIBRATION INJECTION CIRCUIT

Calibration injection circuit

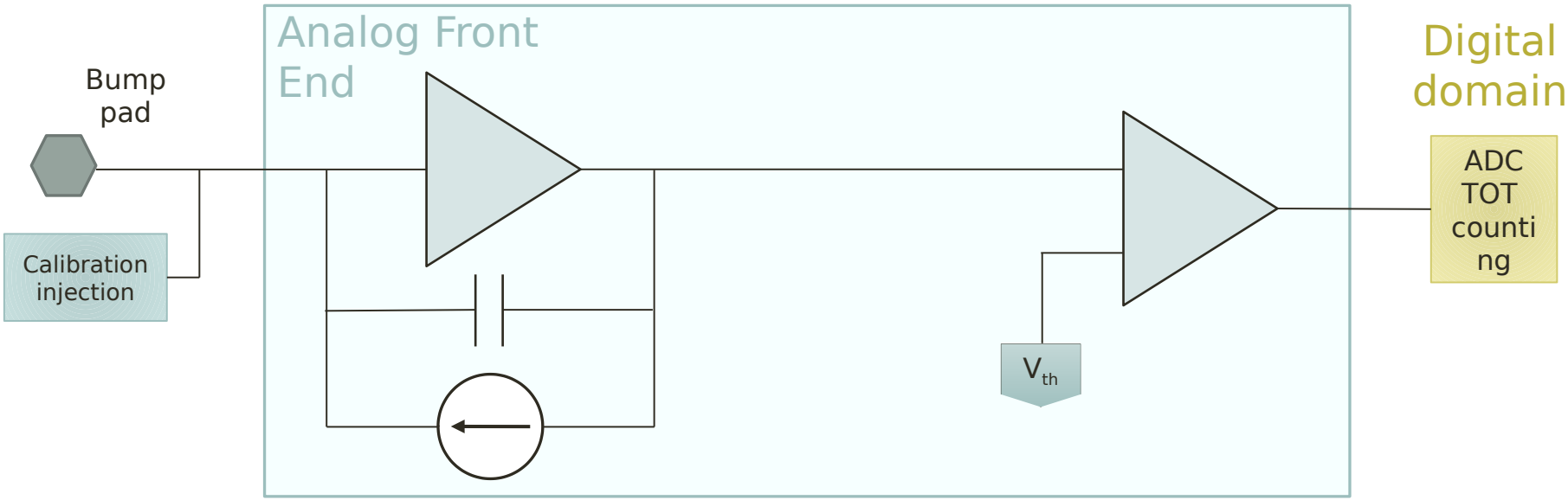
- Present in each pixel, picks charge from global voltage sources
- Same across the whole chip
- Equivalent to 2 switches
  - controlled by 2 control signals (S0 and S1)
  - switching between 3 voltage levels (CAL_HIGH, CAL_MED and GND)

⟶ injection of a known charge to pixels





ANALOG FRONT-END BASICS



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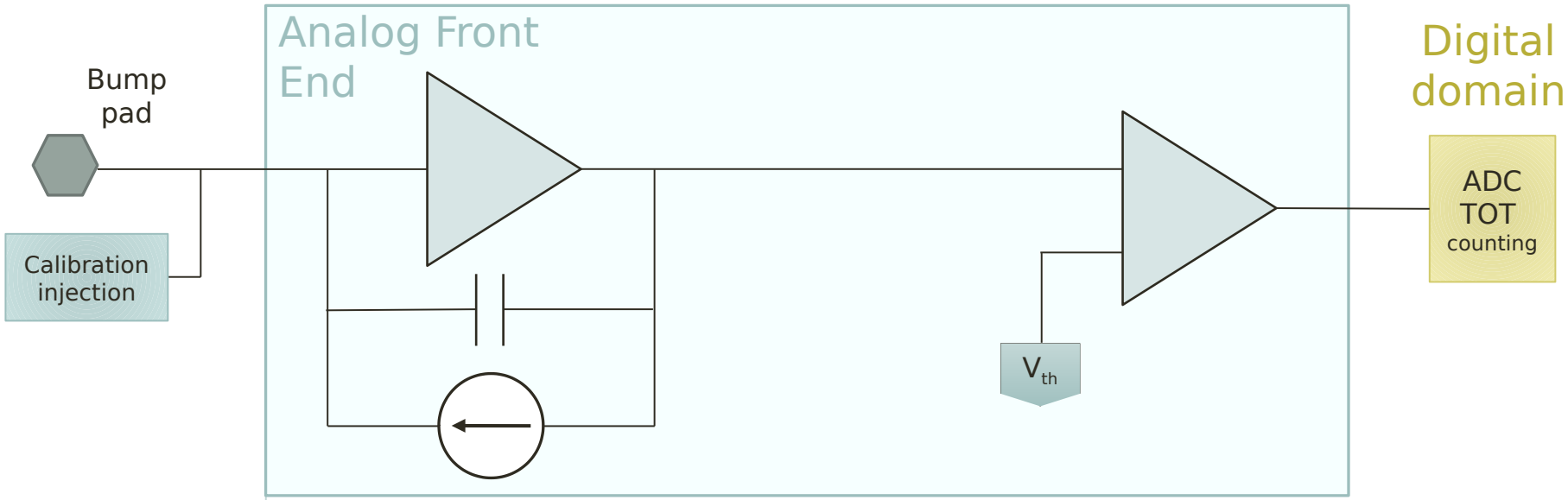
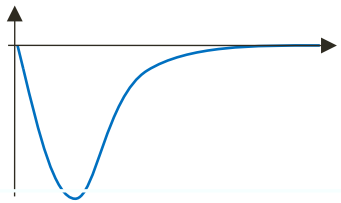


Signal collection

Negative signal arriving from the sensor or from injection circuit



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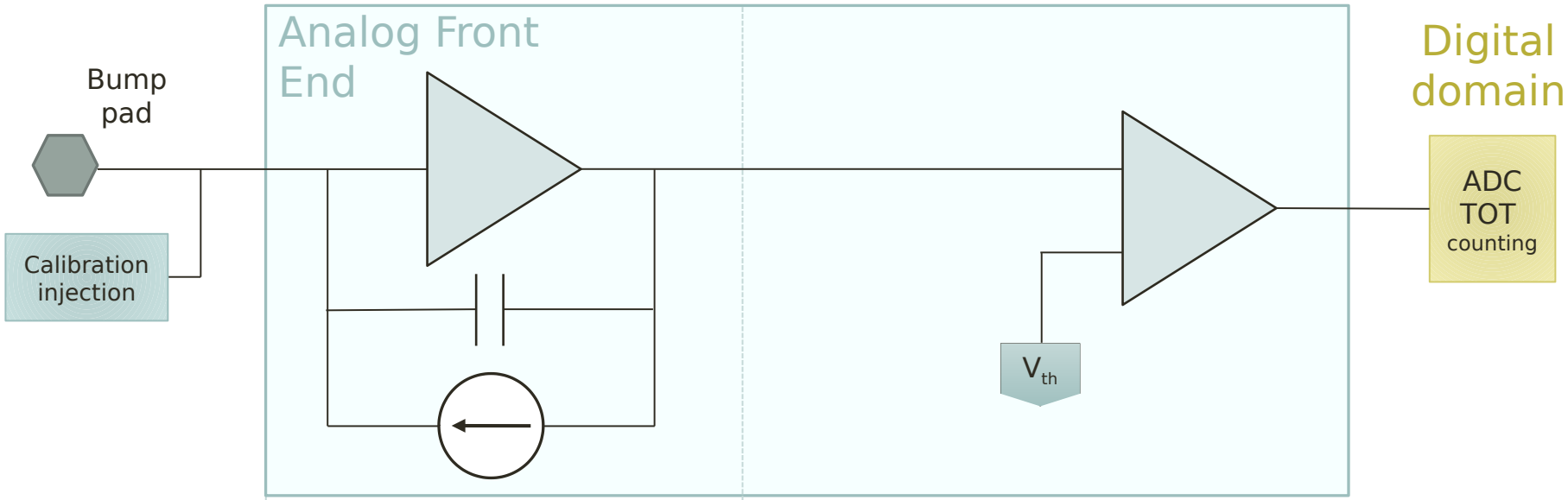

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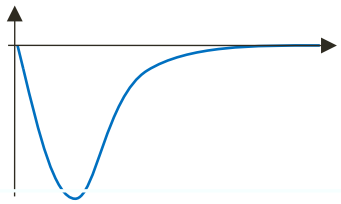
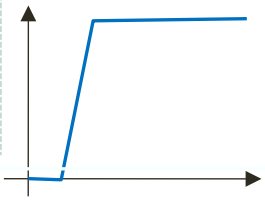


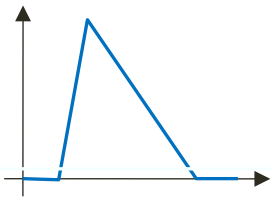
Pre-amplifier

Converts arriving signal in a voltage step



Feedback loop

Discharges the preamplifier after signal rise



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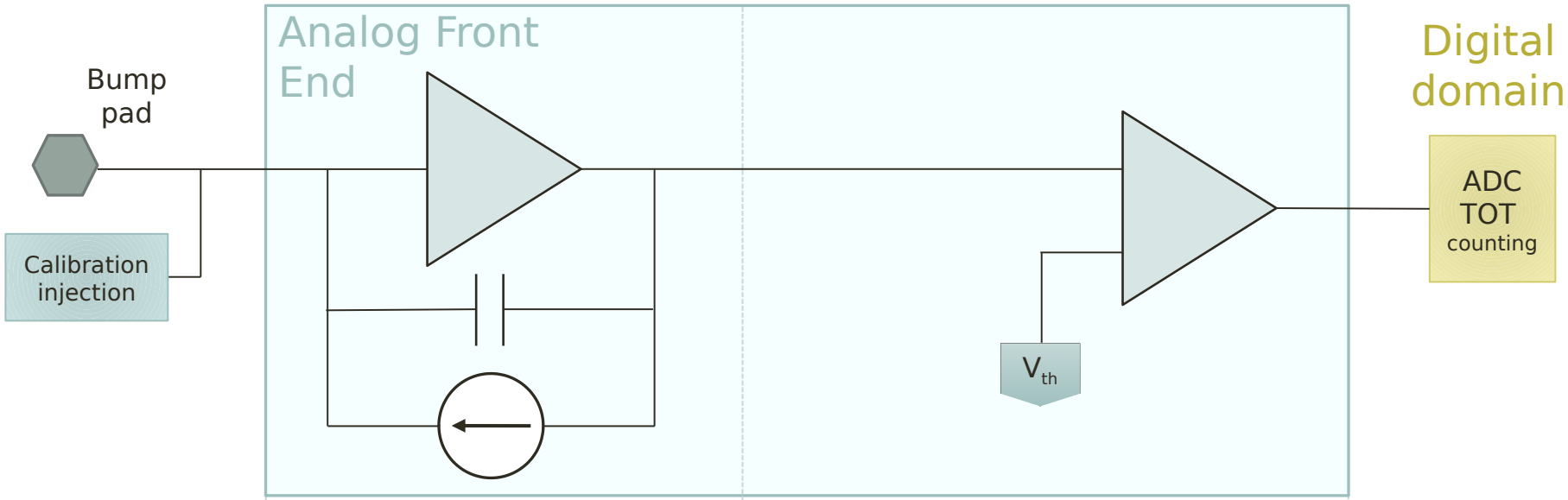

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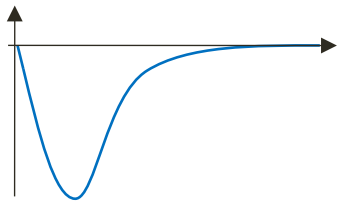

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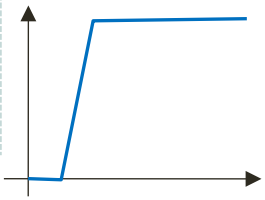

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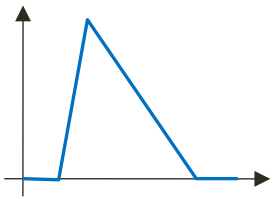
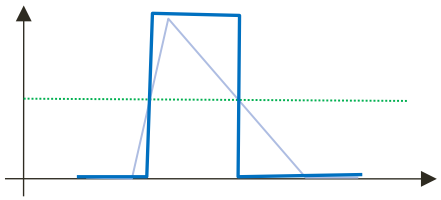


Comparator

Compares the signal with the threshold to determine if there was a hit



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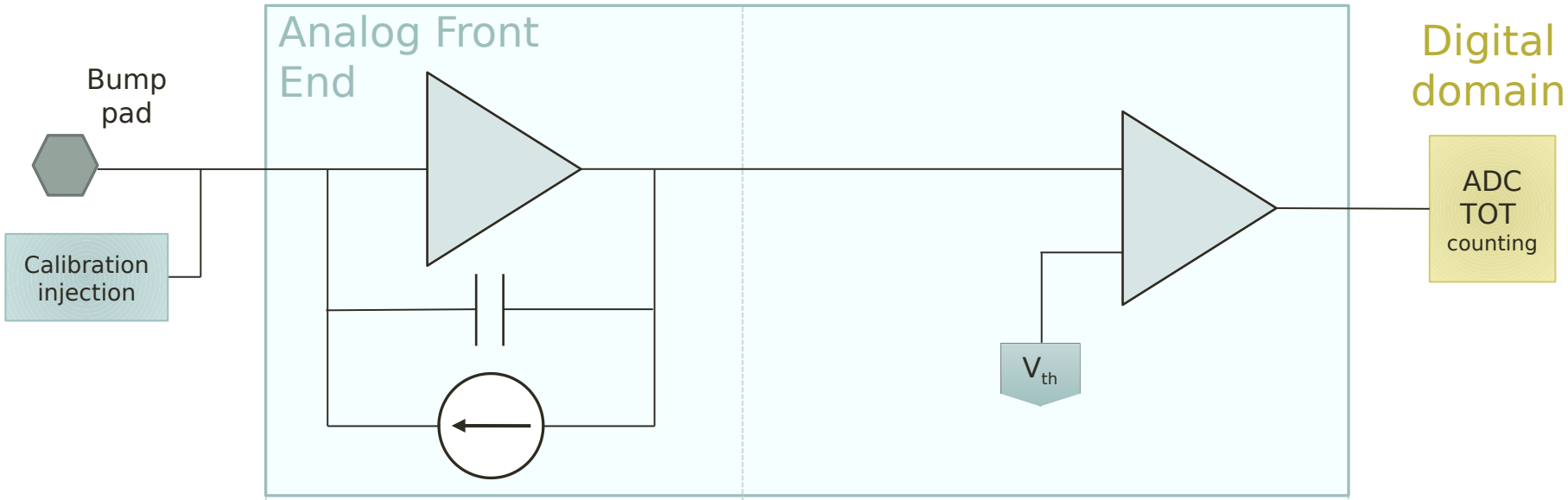

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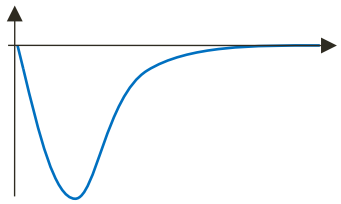

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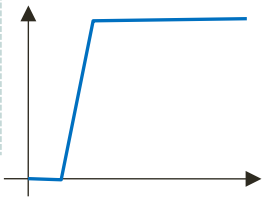

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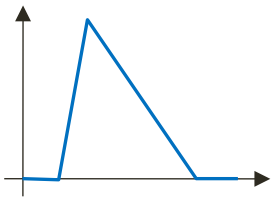

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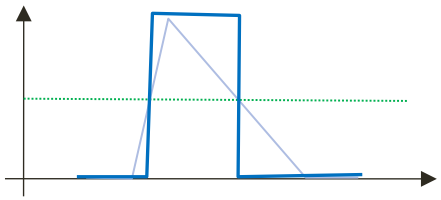
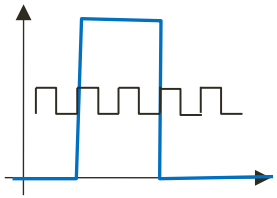


TOT

Time over threshold counting in clock cycles



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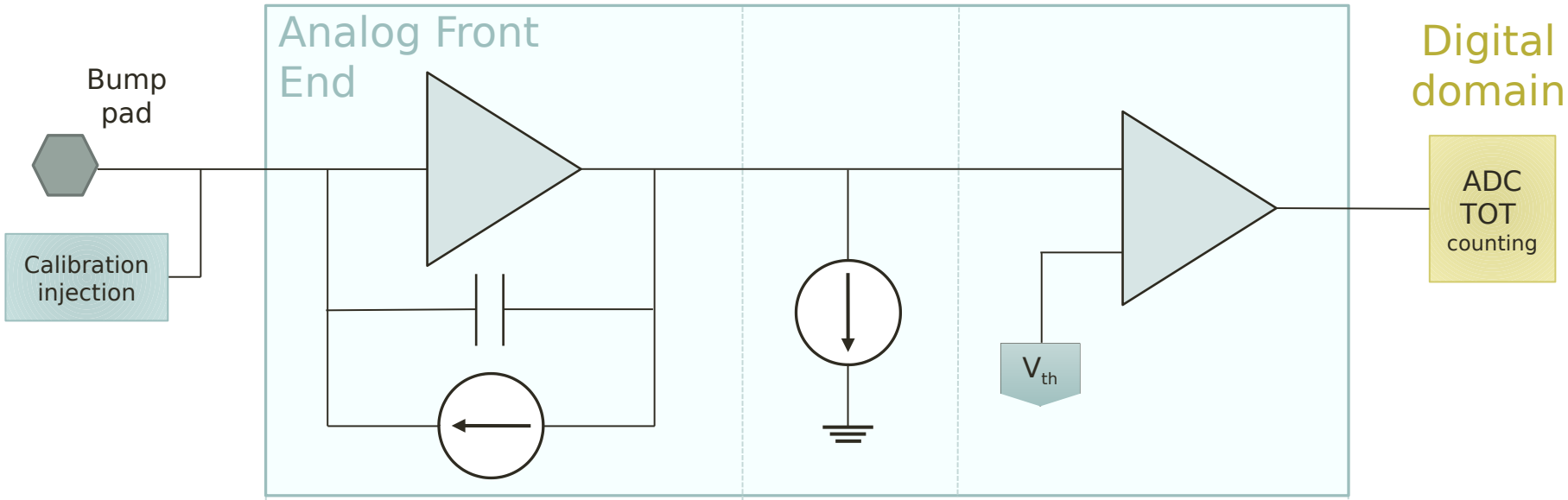

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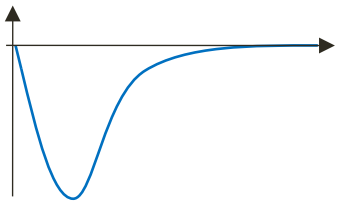

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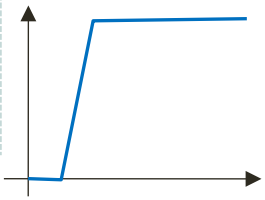

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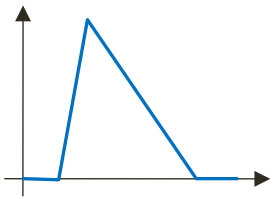
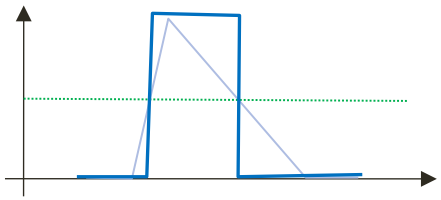


Trimming

Local adjustment of the threshold with the trim bits



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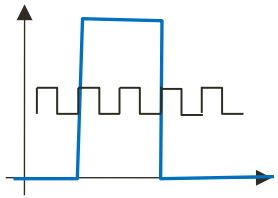
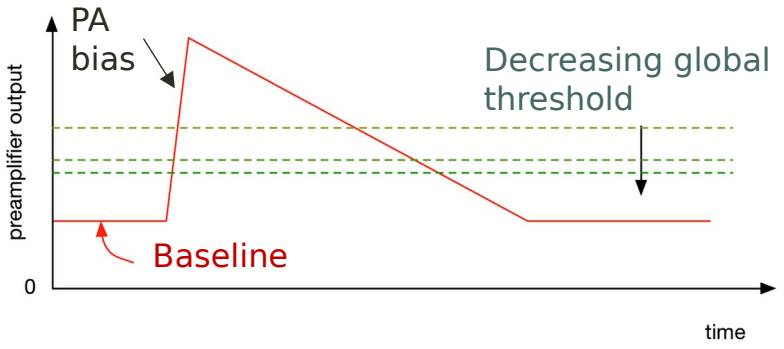
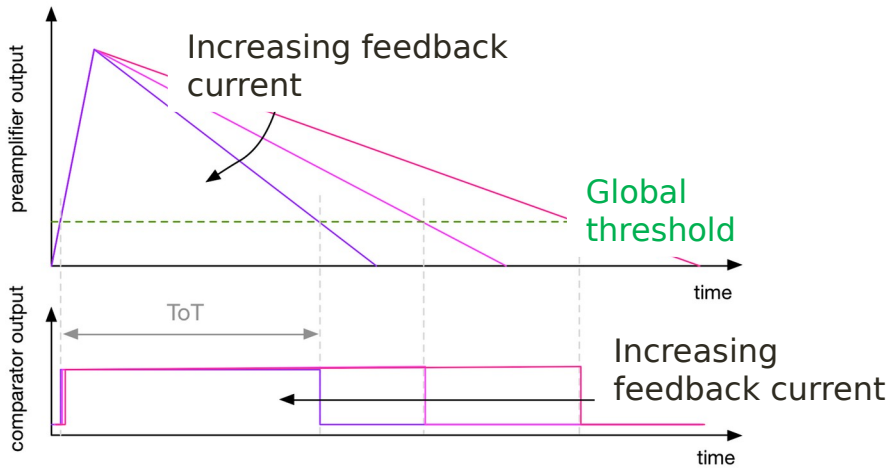


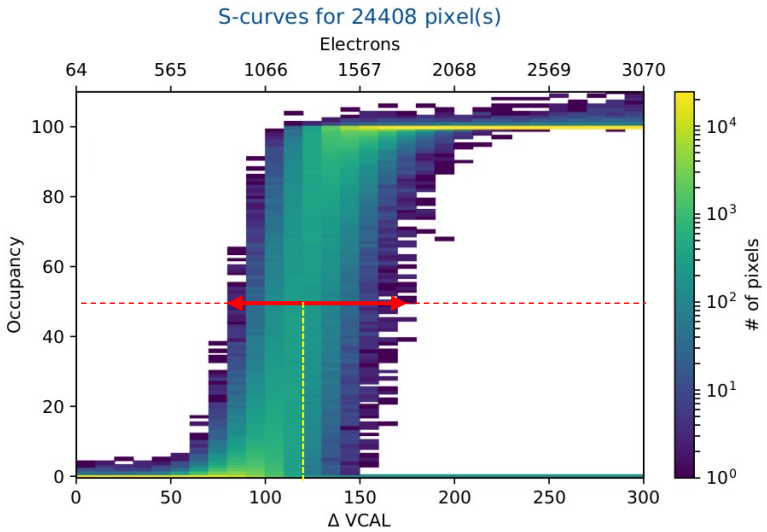
ANALOG FRONT-END PARAMETERS

Global threshold	*Sets the global threshold of the comparator*
Baseline voltage	*Sets the preamplifier output DC baseline*
Preamplifier bias	*Determines the speed of rise of the signal, main contribution to the power consumption, influence on the noise*
Feedback current	*Determines the speed of the preamplifier return to baseline and therefore the time over threshold*



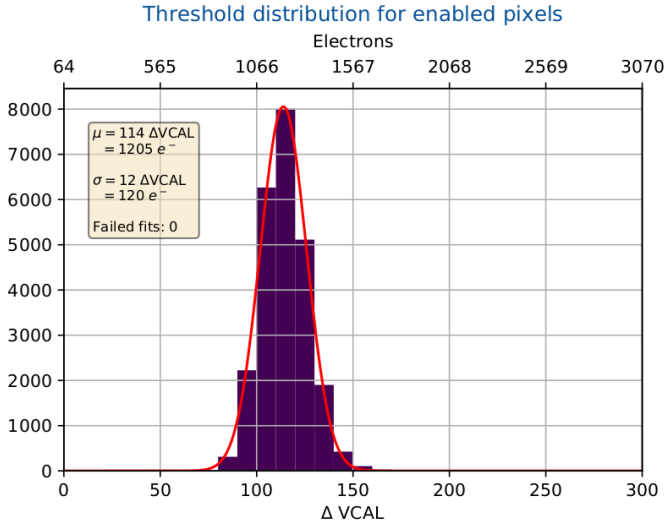


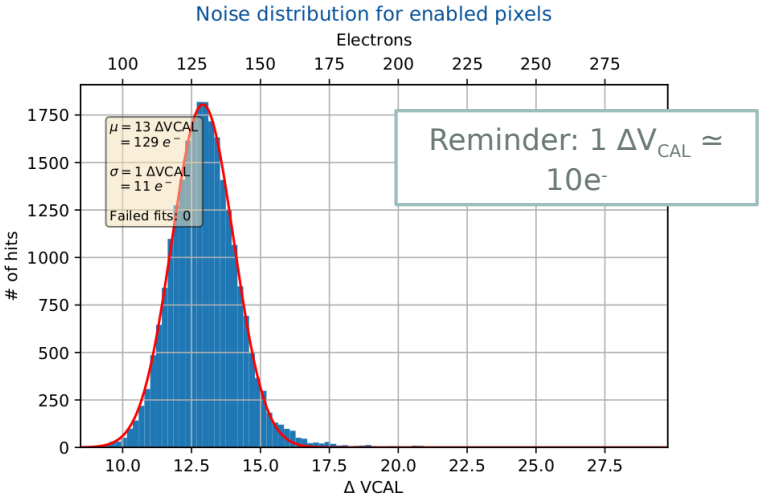
TUNING PROCEDURES



50% occupancy

slope





Reminder: 1 $\Delta V_{CAL} \simeq 10e^-$

Threshold scan

Inject different charges, 100x to every pixel and check number of hits ⟶ occupancy

S-curves

Occupancy vs. injected charge, for every pixel

Threshold

Charge at which 50% occupancy is reached, for every pixel

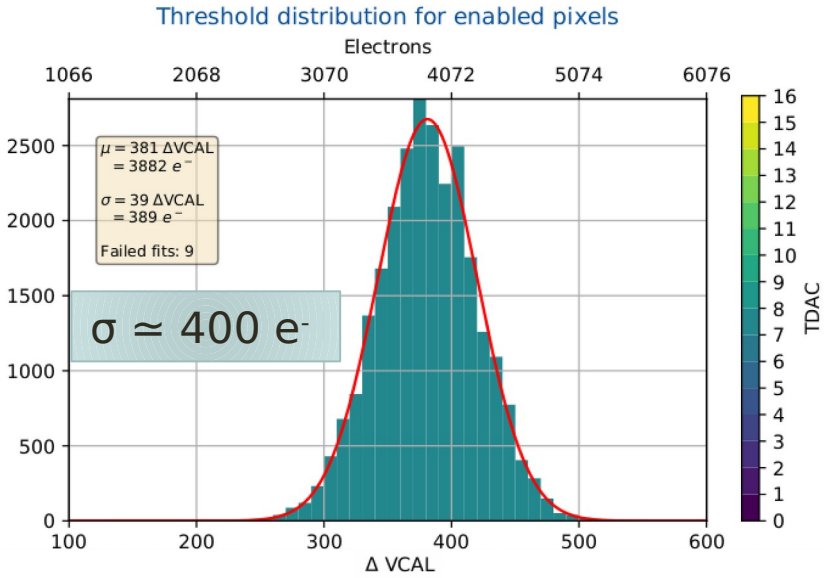
Equivalent noise charge (ENC)

Slope of the s-curve, for each pixel

THRESHOLD TRIMMING

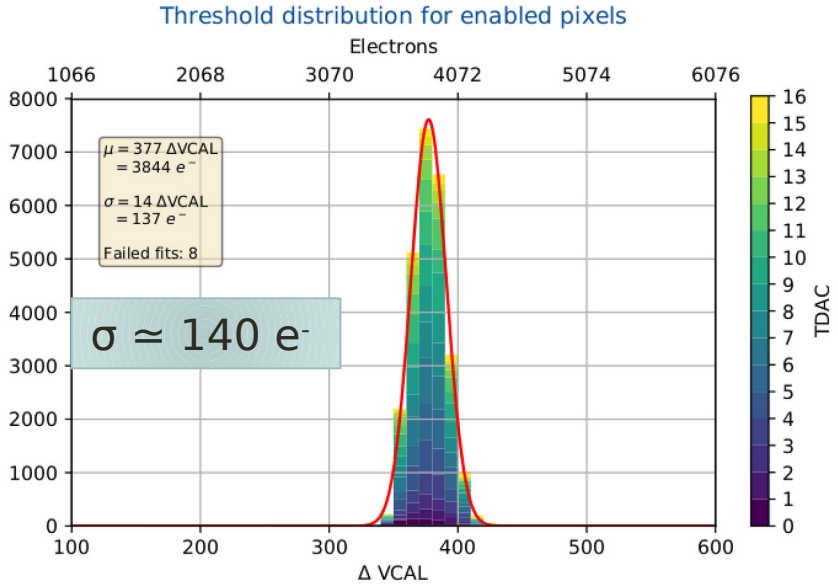
FE Tuning

- per pixel local compensation of comparator threshold dispersion
- set a register in each pixel with a number of **trimming bits** needed to bring local threshold as close as possible to the mean threshold



Before tuning

- All trim bits set to 7
- Wide threshold distribution



After tuning

- Each pixel with a different trim bit (7 as average trim)
- Narrow threshold distribution

Tuning Manual: https://twiki.cern.ch/twiki/pub/RD53/RD53ATesting/LIN_AFE_tuning_example.pdf