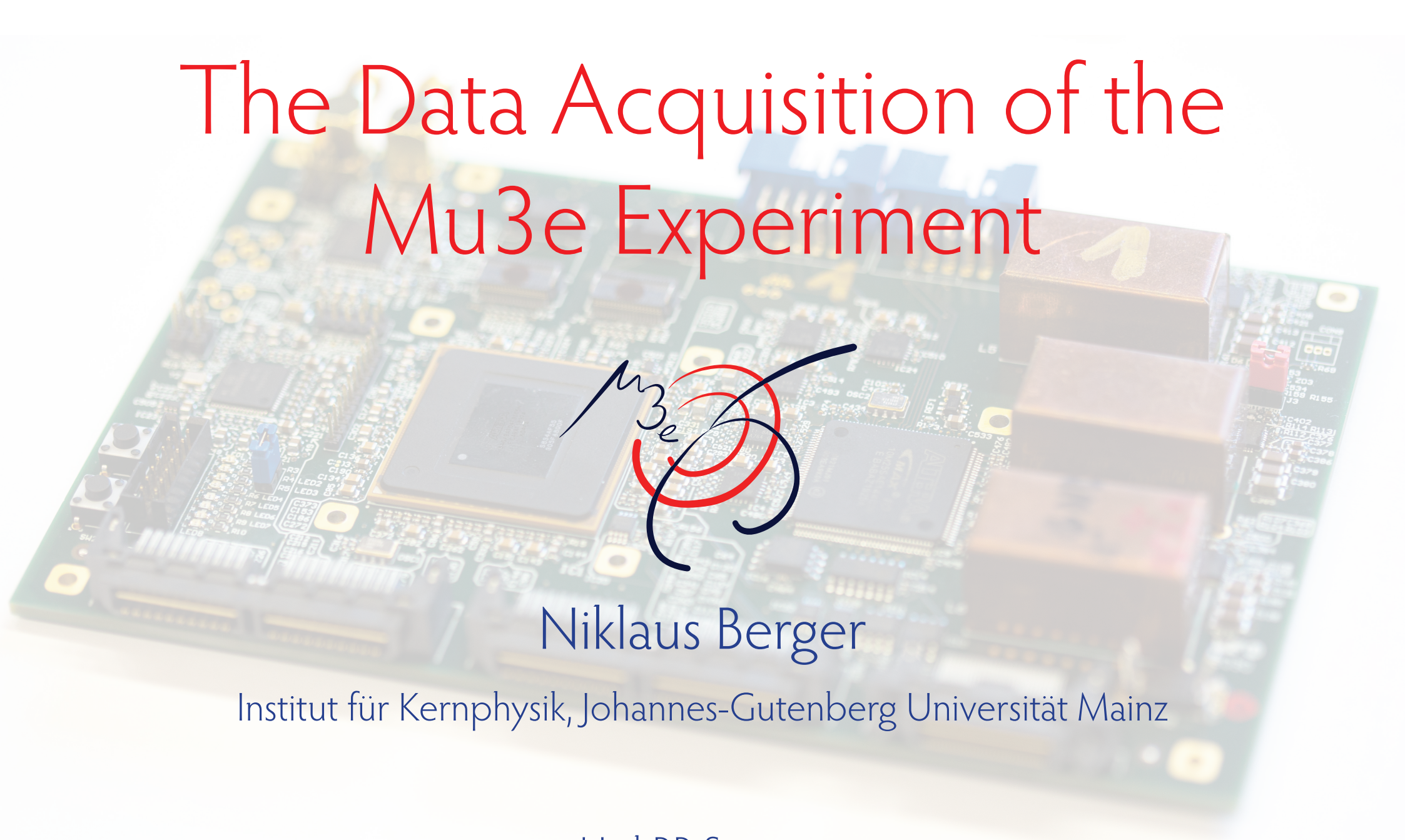
The Data Acquisition of the Mu3e Experiment

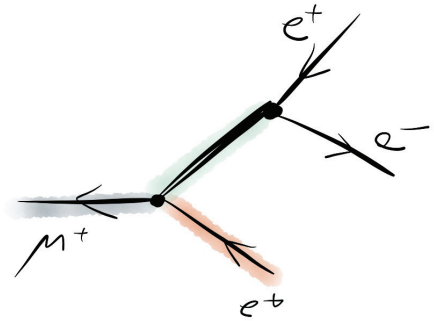


Niklaus Berger

Institut für Kernphysik, Johannes-Gutenberg Universität Mainz

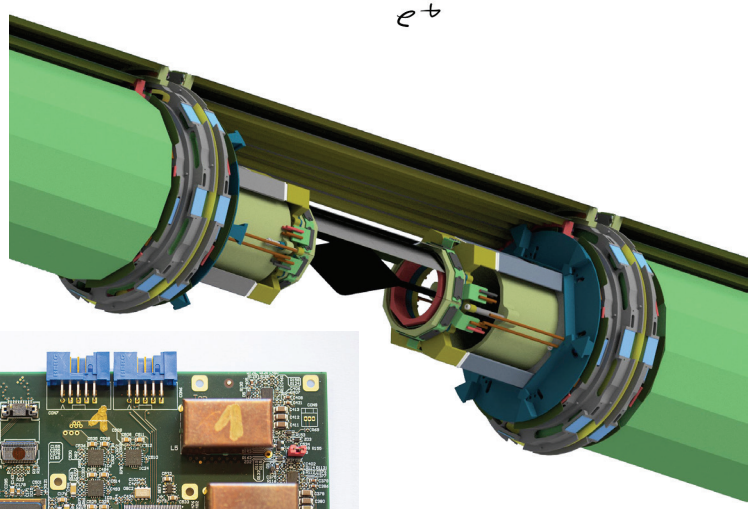
HighRR Seminar
April 2021

Overview



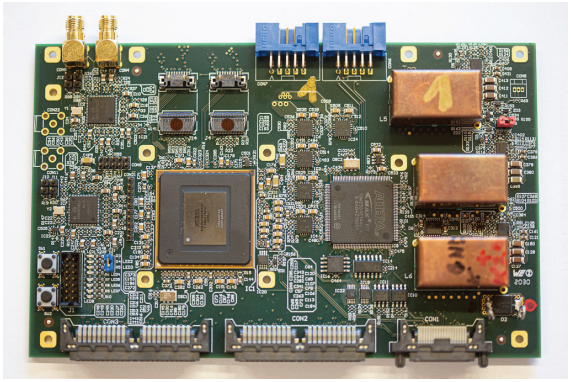
Searching for charged lepton flavour violation:

- The Mu3e experiment



100 Gbit/s streaming readout:

- The Mu3e data acquisition



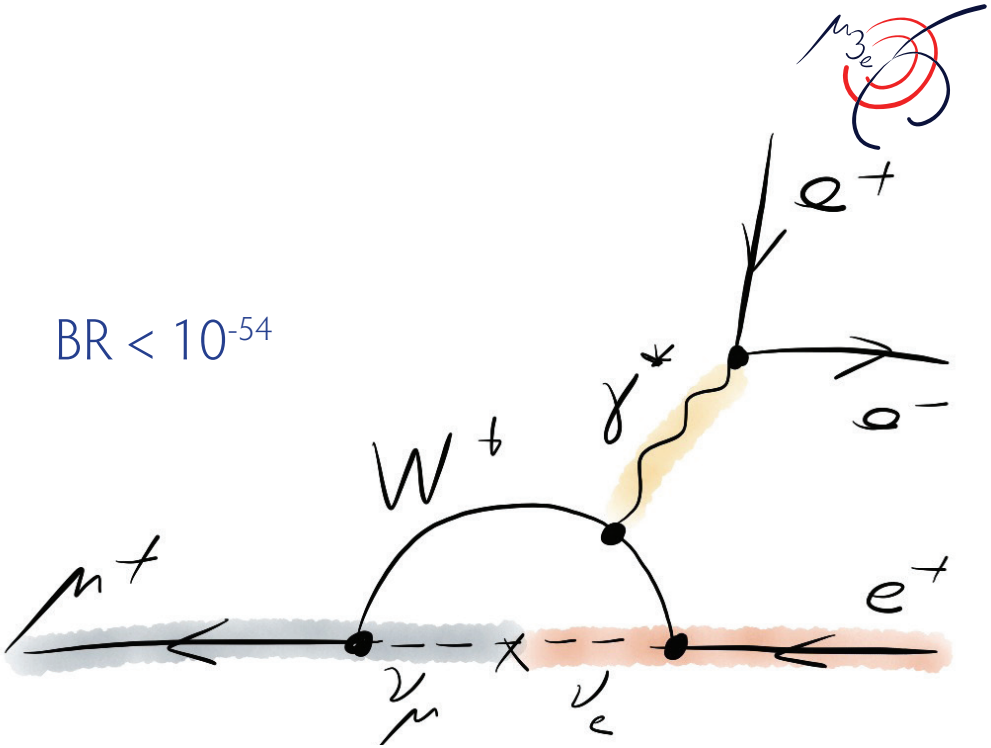
> 10^9 track fits/s on GPUs:

- The Mu3e filter farm

Searching for $\mu^+ \to e^+e^-e^+$

- Lepton flavour violating muon decays
- Extremely low branching fractions in the Standard Model
- Excellent probes for new physics
- $BR(\mu^+ \to e^+e^-e^+) < 10^{-12}$ (SINDRUM, 1988)

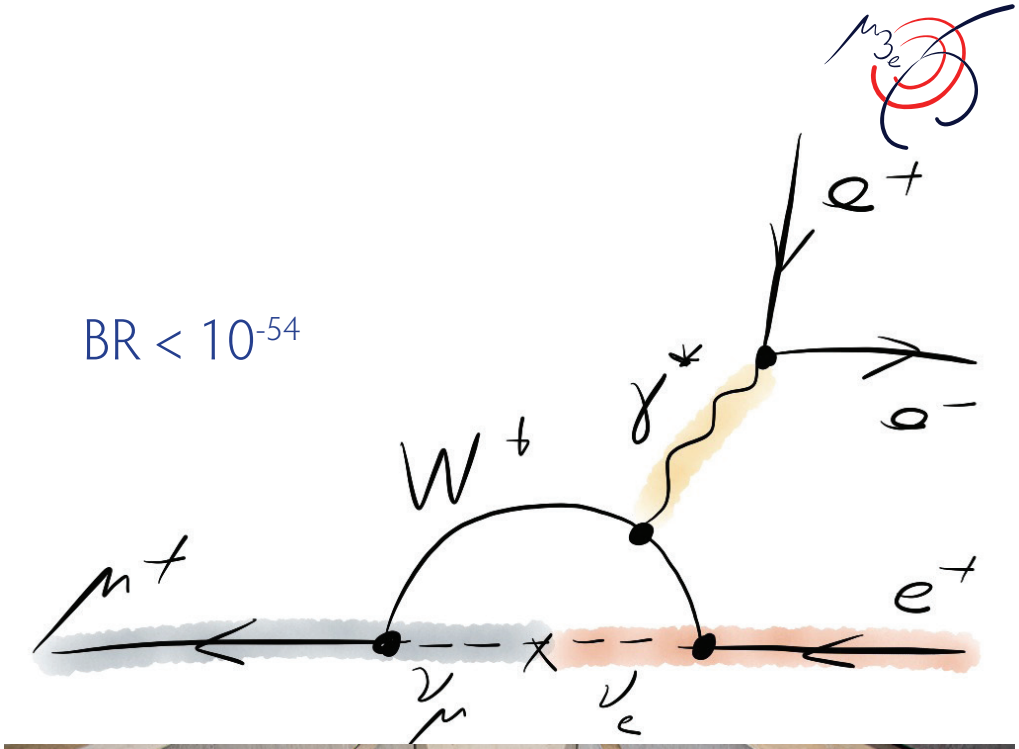
$BR < 10^{-54}$

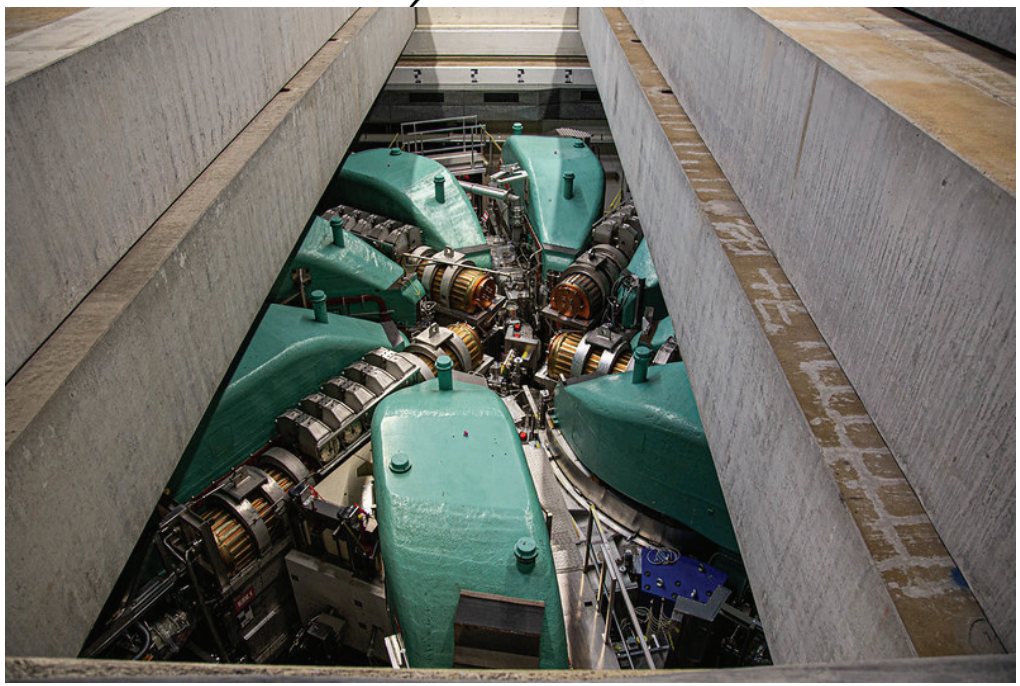


Searching for $\mu^+ \rightarrow e^+e^-e^+$

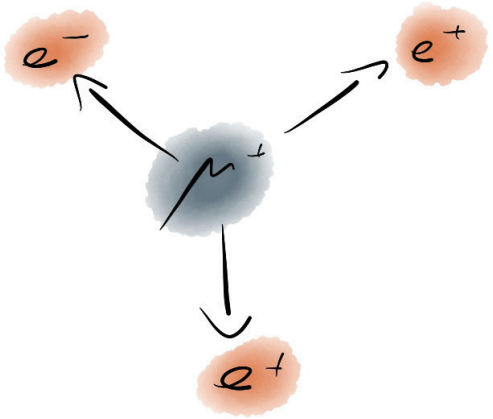
- Lepton flavour violating muon decays
- Extremely low branching fractions in the Standard Model
- Excellent probes for new physics
- BR($\mu^+ \rightarrow e^+e^-e^+$) < 10^{-12} (SINDRUM, 1988)

- Mu3e aims for a sensitivity of 1 in 10^{16}
- Very intense muon beam: Paul Scherrer Institute (PSI), Villigen, Switzerland
- $2 \cdot 10^{-15}$ in a first phase at an existing beam line with 10^8 muons/s - this talk
- Plans for new high-intensity muon beam line (HiMB) with > 10^9 muons/s





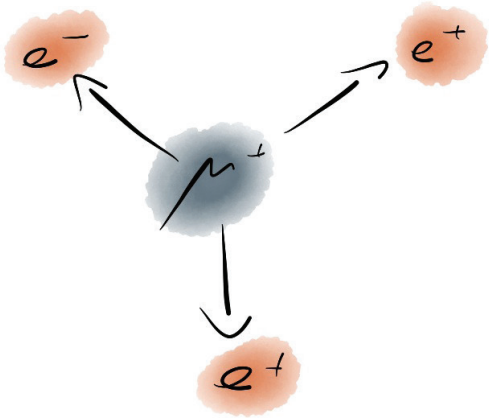
Signal and Background

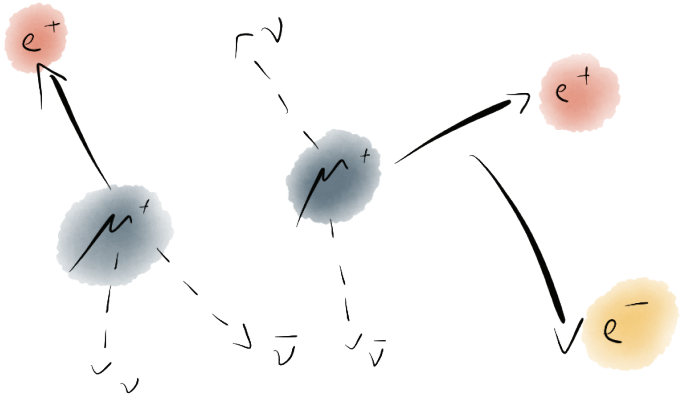


Signal

- $\mu^+ \rightarrow e^+e^-e^+$ at rest
- Two positrons, one electron
- From same vertex
- Same time
- $\Sigma\, p_e = m_\mu$
- Maximum momentum:
  $\frac{1}{2}\, m_\mu = 53$ MeV/c

Signal and Background





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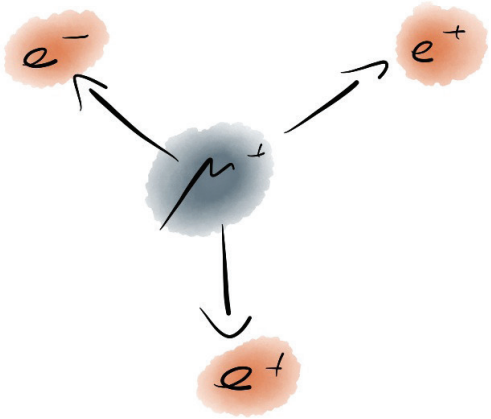
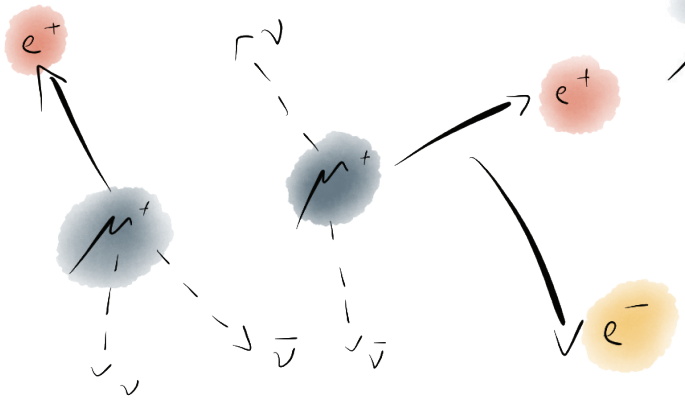
Accidental Background

- Several muon decays
- Plus an electron
- Need good vertexing
- Need good timing

Signal and Background





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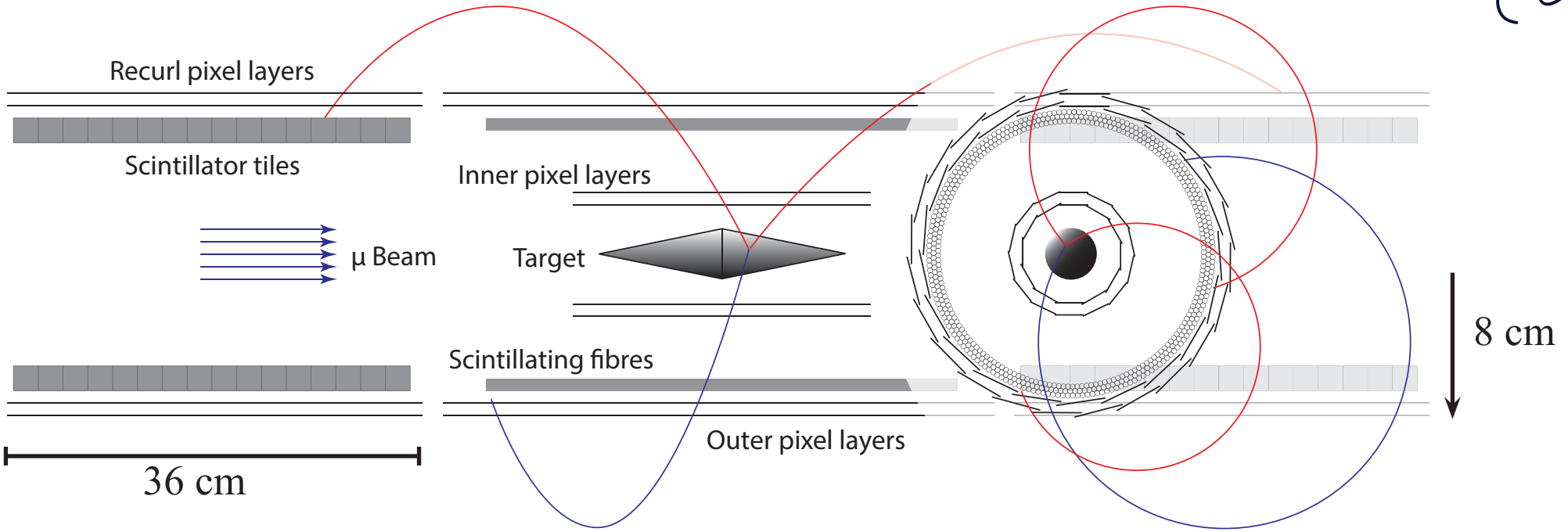
Internal conversion decay

- Allowed rare decay
- $\mu^+ \rightarrow e^+e^-e^+\nu\bar{\nu}$
- Detect missing energy carried by neutrinos
- Need excellent momentum reconstruction

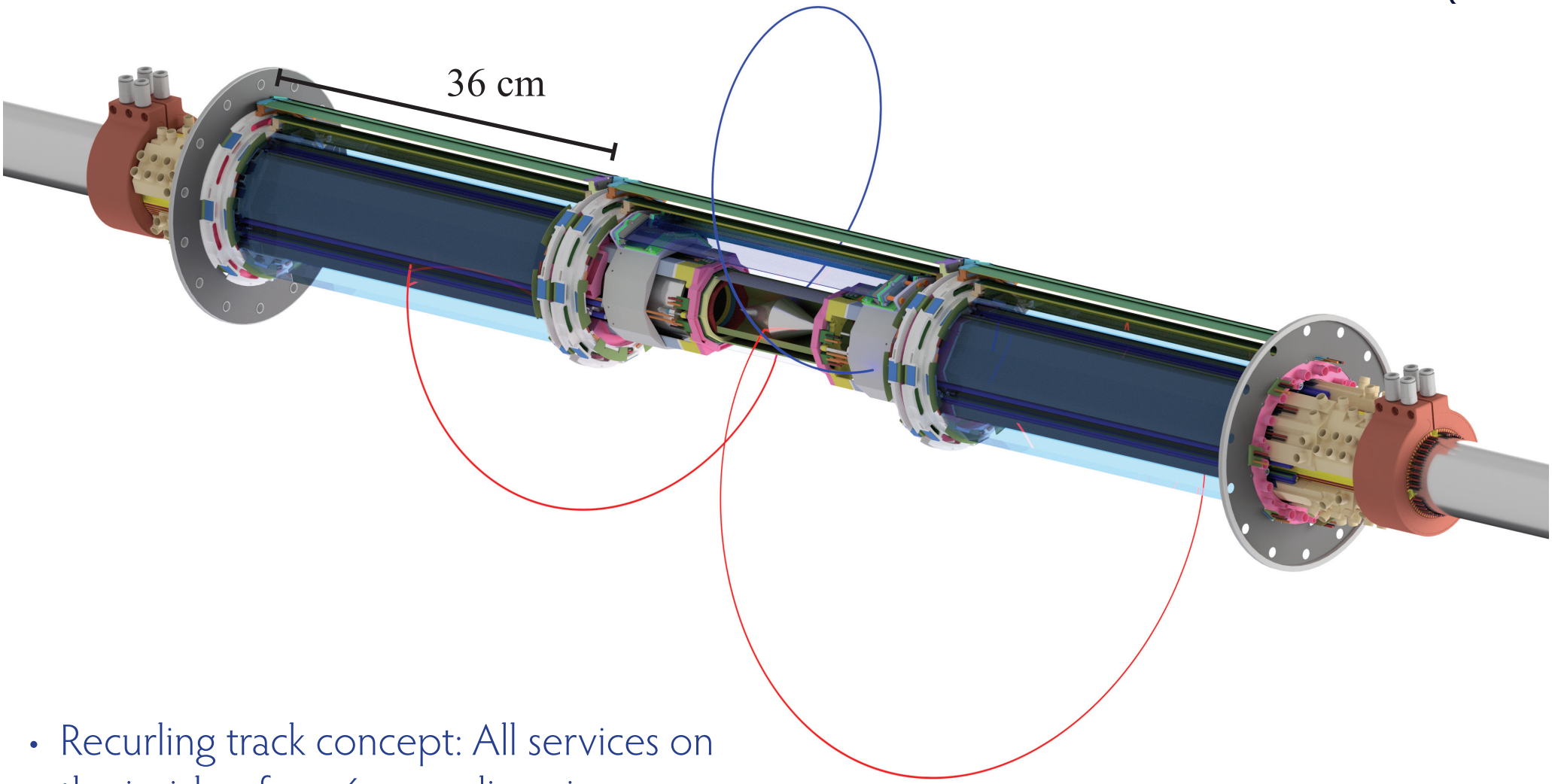
The Mu3e Detector



- 1 T solenoid field
- Helium atmosphere to reduce scattering and for cooling
- Minimize material to minimize scattering

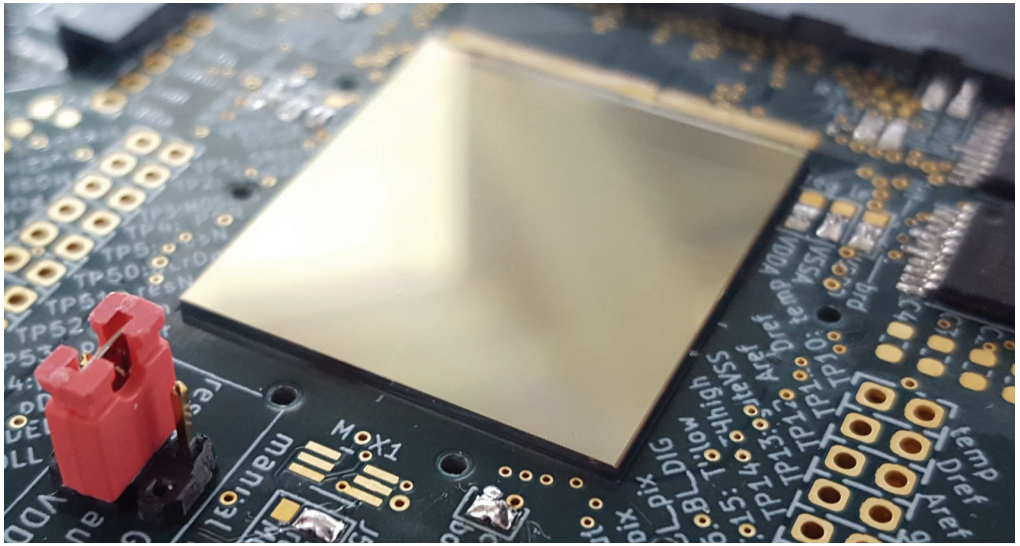
- Ultra-thin layers of high-voltage monolithic active pixel sensors (HV-MAPS)
- Scintillating fibres and tiles for improved timing measurements
- Long lever arm of recurling tracks gives precise momentum measurement

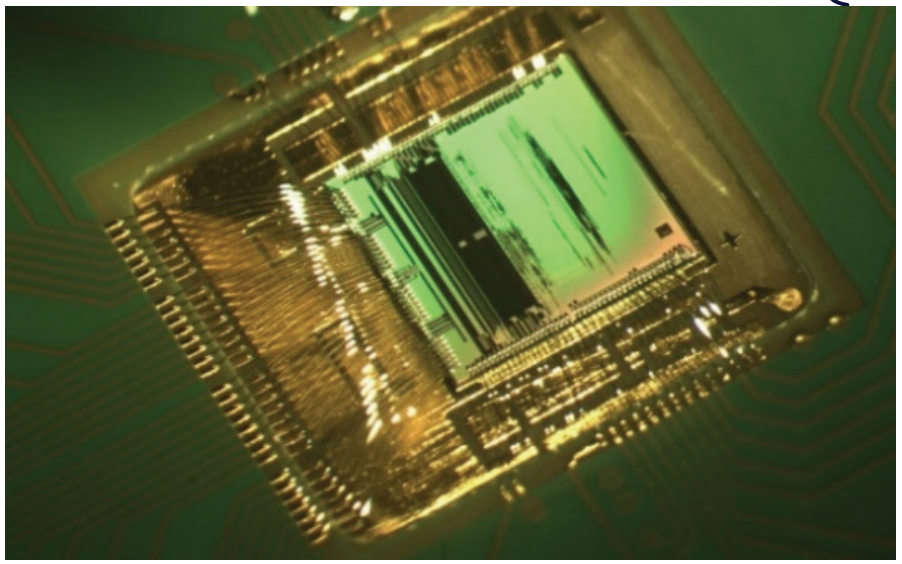
Geometry



- Recurling track concept: All services on the inside of a ~ 6 cm radius pipe
- (together with the beam)

Detector ASICs





MuPix High-Voltage Monolithic Active Pixel Sensor (TSI 180 nm HV-CMOS process)

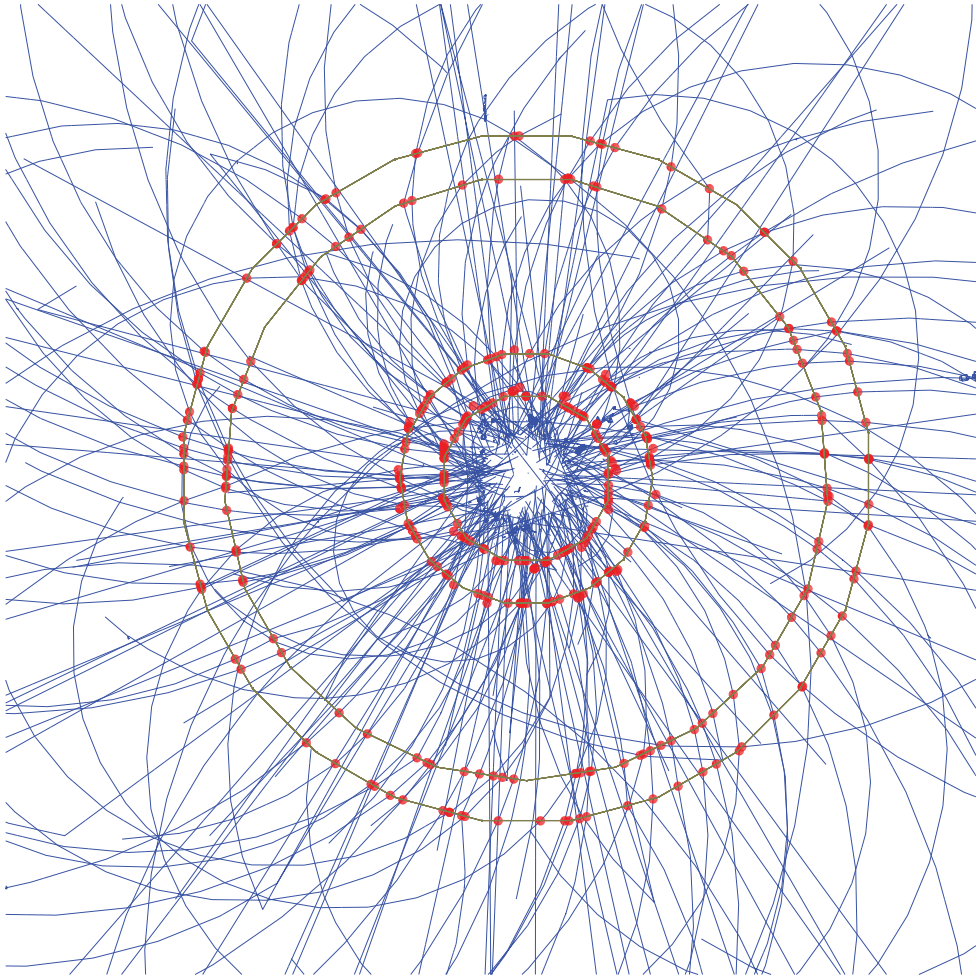
- 2 x 2 cm^2, 80 x 80 μm^2 pixels, 50 µm thin
- Discriminator, address generation and time-stamping for each pixel
- Readout state-machine, serializer
- 1.25 Gbit/s LVDS 8bit/10bit encoded output

MuTrig TDC for Silicon Photomultiplier readout (UMC 180 nm CMOS process)

- 32 channels, 50 ps time bins
- Bias adjustment for the SiPMs
- Readout state-machine, serializer
- 1.25 Gbit/s LVDS 8bit/10bit encoded output

Requirements for the data acquisition

- Up to 10^8 muon decays/s
- 2844 MuPix sensors with 182 million pixels
- 8896 SiPM readout channels
  - 278 MuTrig TDC ASICs
- ~ 100 Gbit/s data after zero suppression on ASICs
- Highly non-local signal signature
- Can write about 100 MB/s to mass storage



Challenges

- Number of channels is larger than in a typical LHC experiment
- Mu3e is a small collaboration with limited budget and manpower as well as an ambitious schedule
- Space is extremely tight everywhere: in the detector, around the detector, in the counting house
- What we do now is also a demonstration for going to a 20 times higher rate

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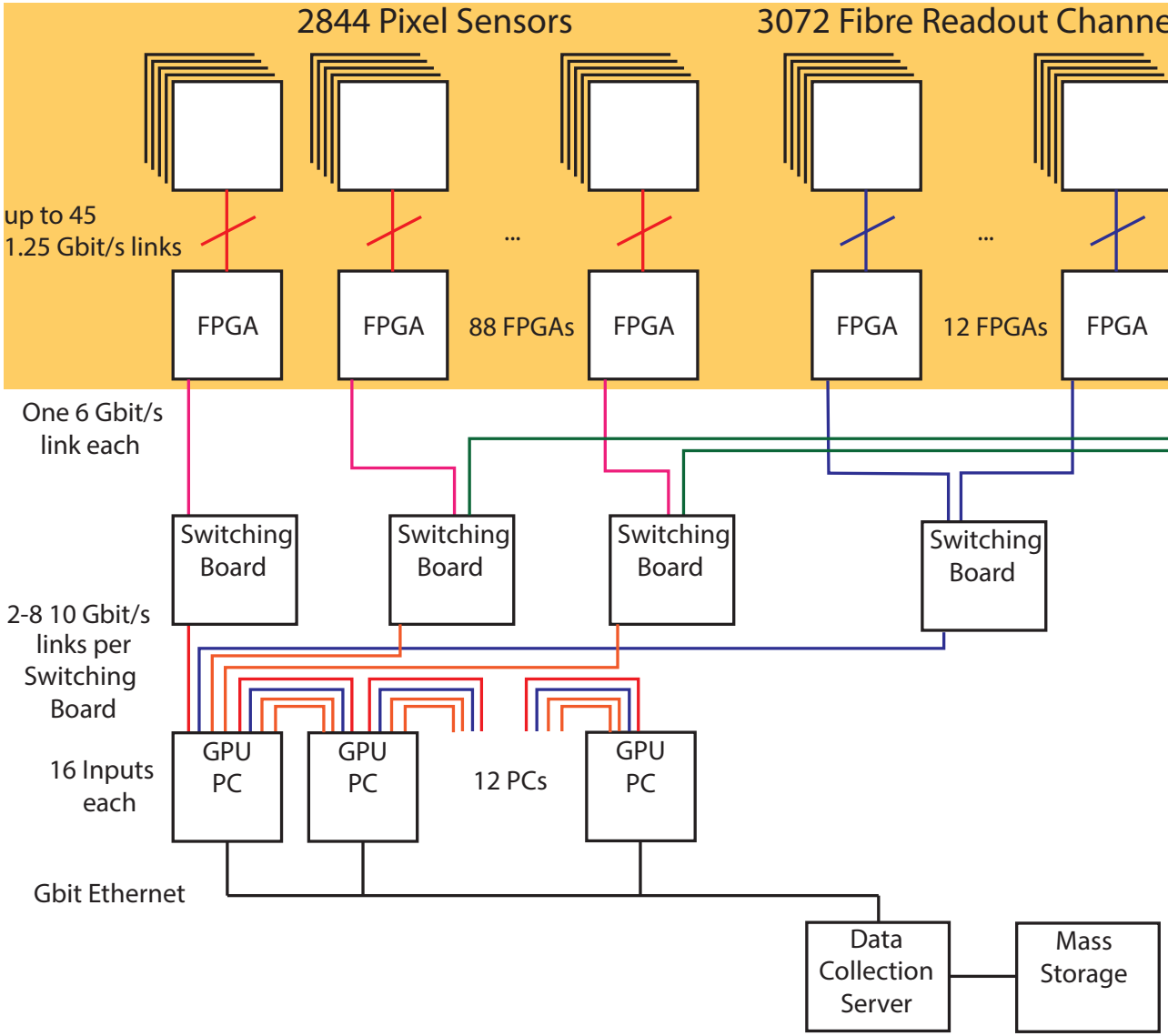
How to handle

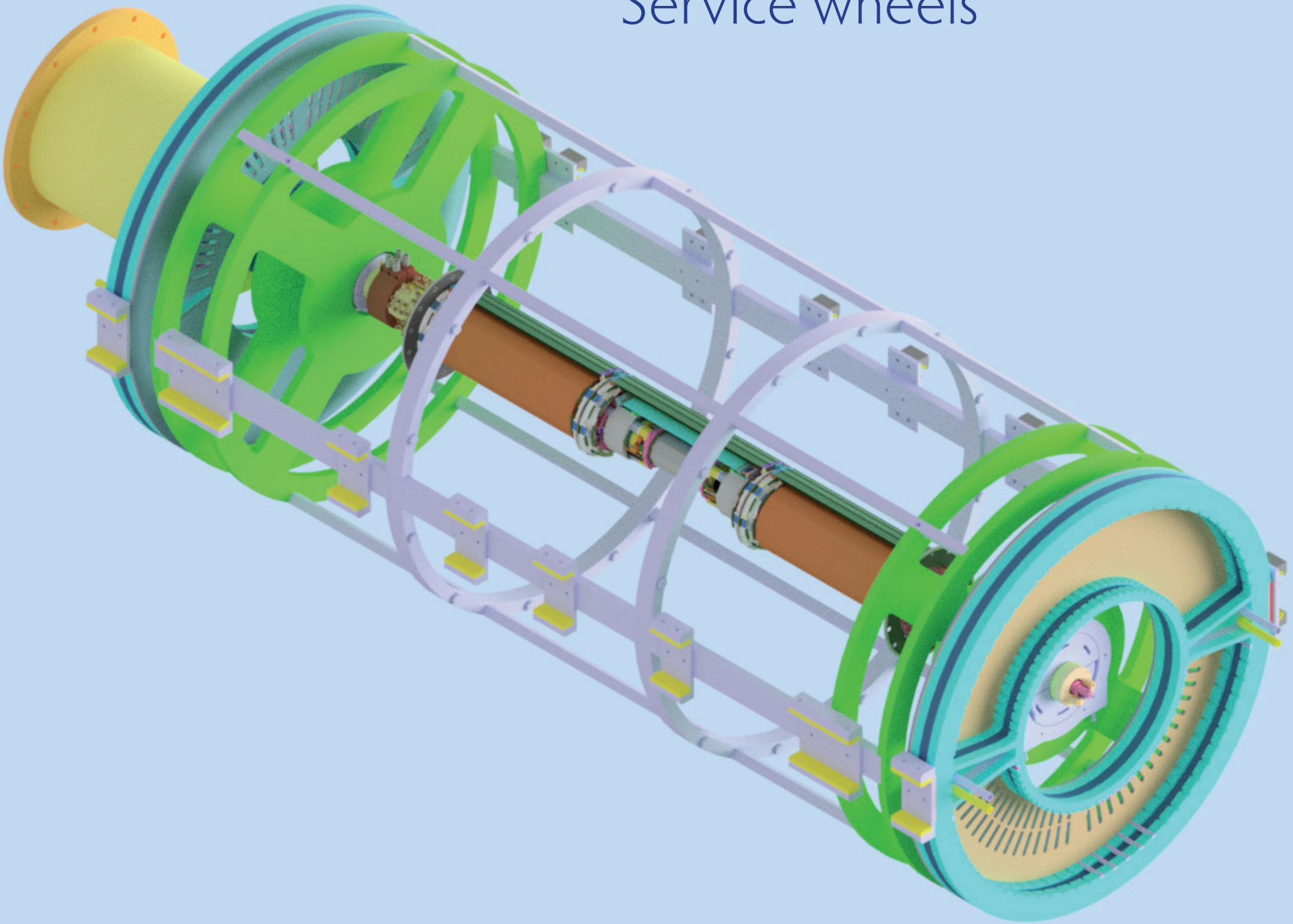
- Full digitization, zero-suppression and multiplexing in the front-end ASICs
- Use commercial/existing components whenever possible
  Write and test firmware early
- Go for small components, high speed optical links, try clever over brute force where possible
- Try to be scalable

DAQ Design

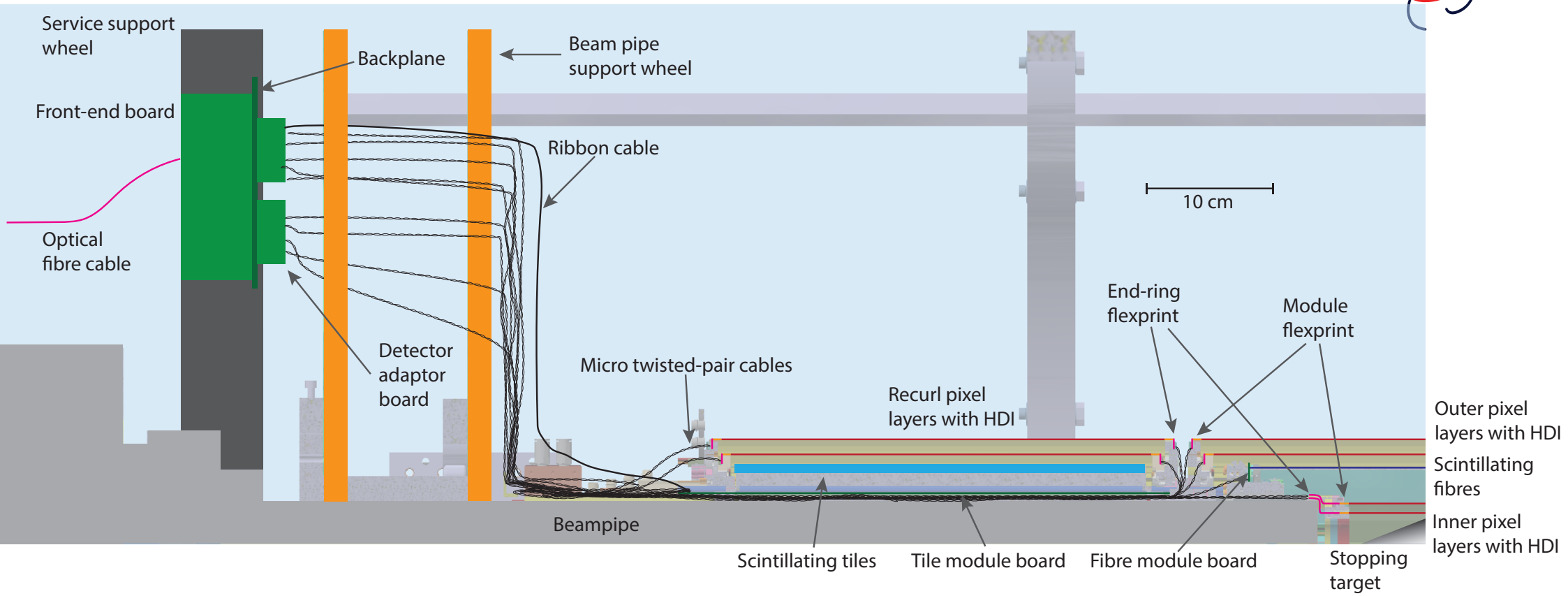


- Fully streaming DAQ
- Network of FPGAs and optical links
- Collect all data of a time slice on one PC
- Reconstruct tracks, then vertices on a GPU
- Write interesting events to disk

Service wheels

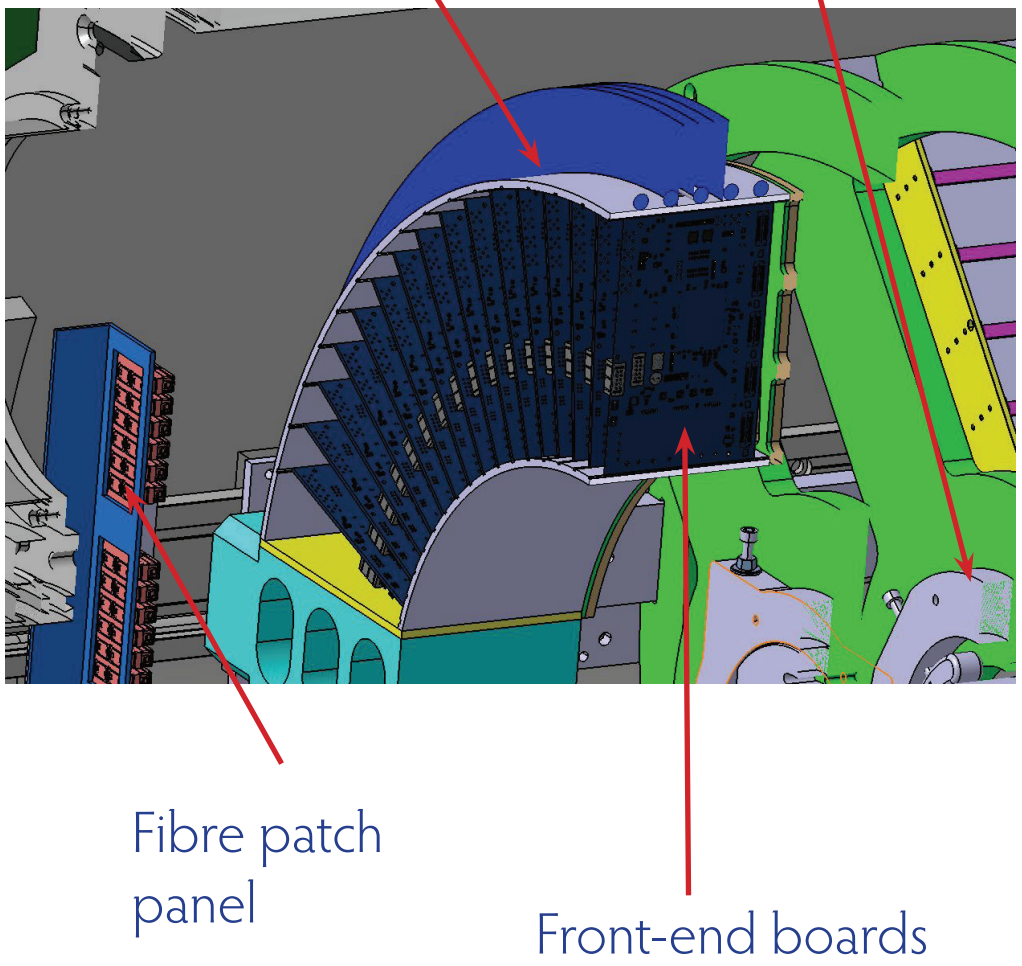


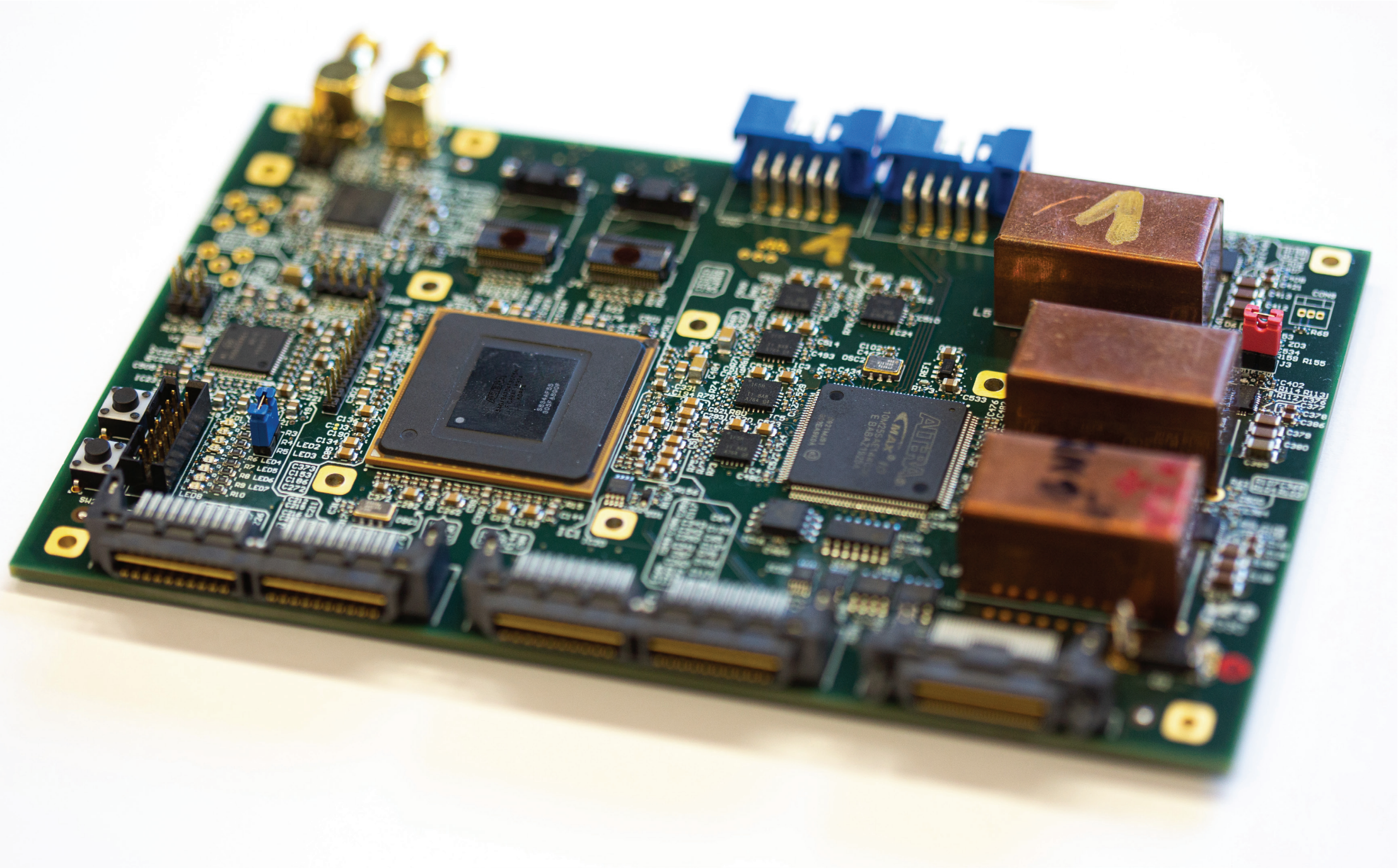
Front-end cabling



Front-end board

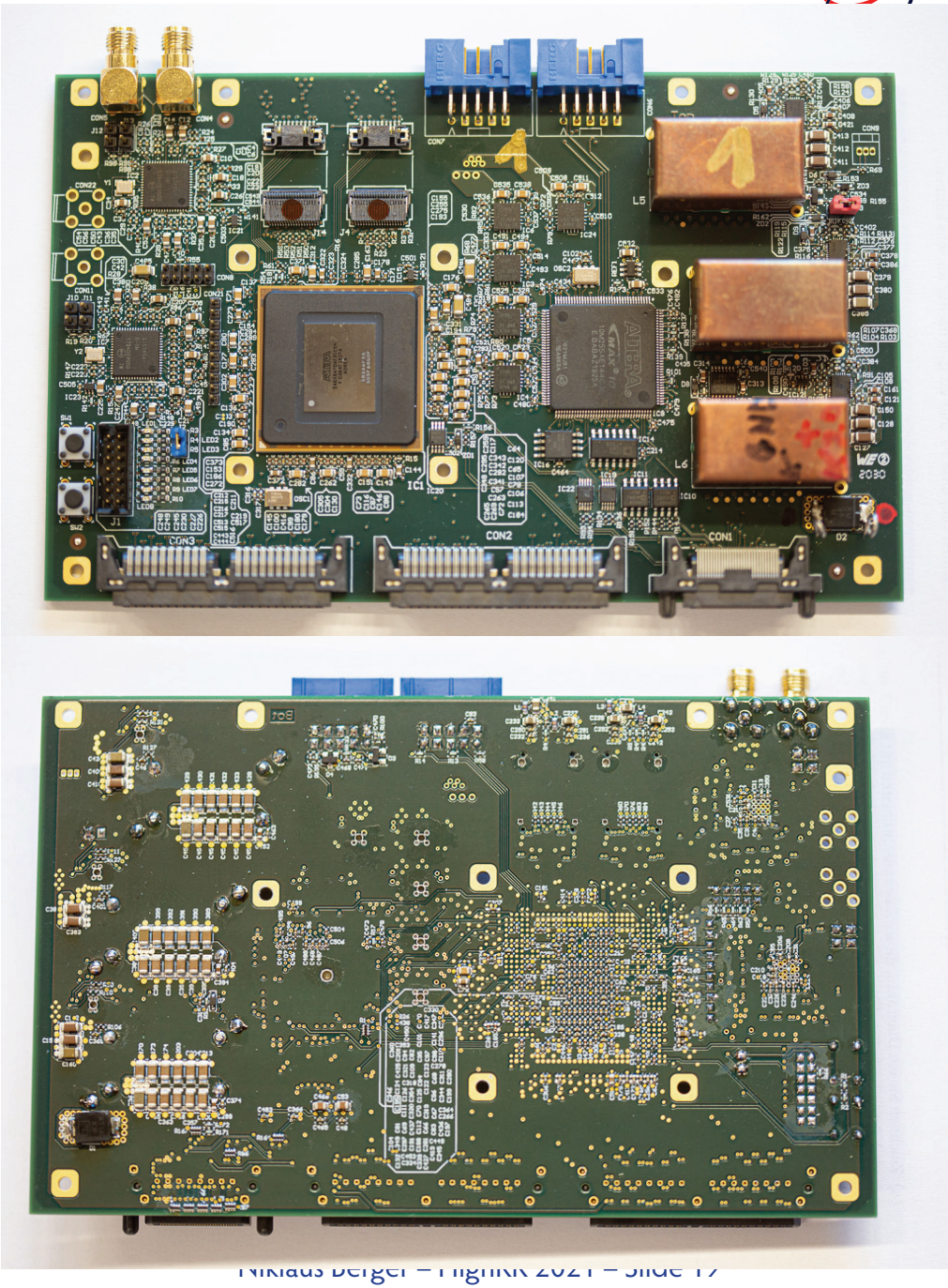
- Mounted in quarter-circular crates inside the 1 m diameter solenoid
- Backplane for control connections and connection to detector
- Adaptors on back of backplane for detector specific cabling
- Aluminium cooling plates connected to water-cooled crate with heat pipes
- ~ 1000 multi-mode optical fibres to the outside world



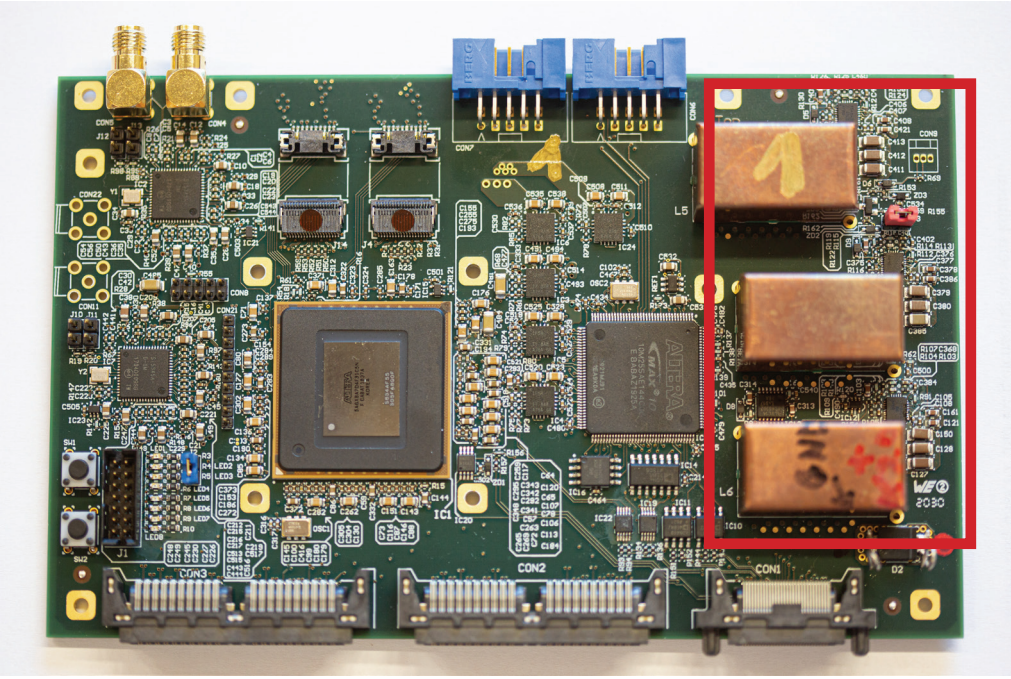


Front-end board

- Fully featured version for operation in helium and magnet, final form factor etc.
- Intel Arria V FPGA, big enough for up to 45 incoming MuPix links
- Designed by Dirk Gottschalk in Heidelberg
- So far: Twenty pieces produced in three iterations, all usable

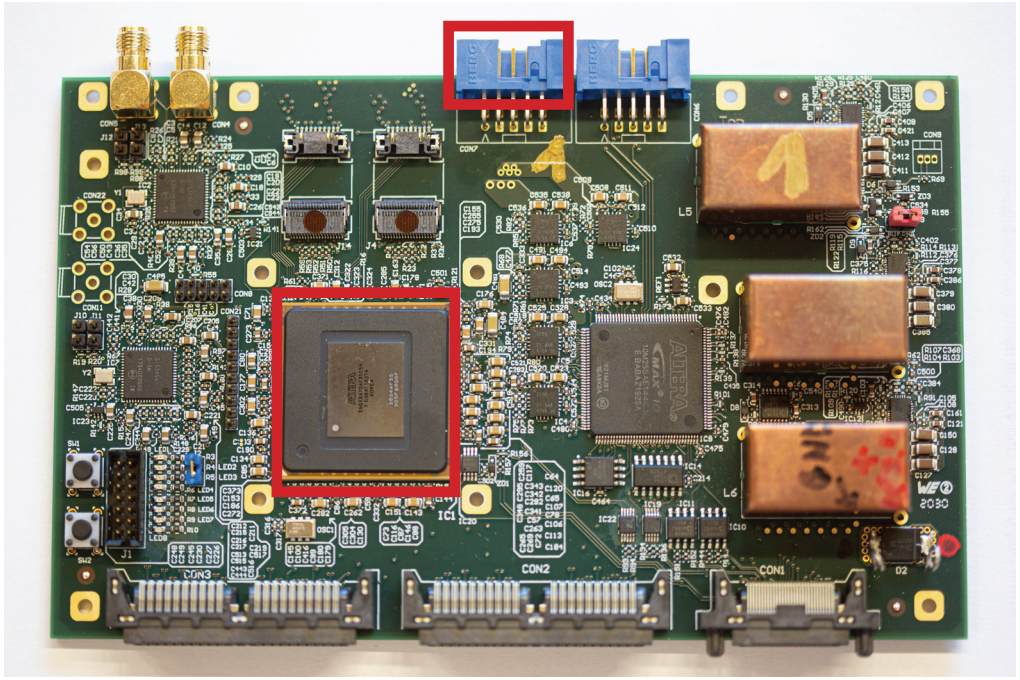


Powering:



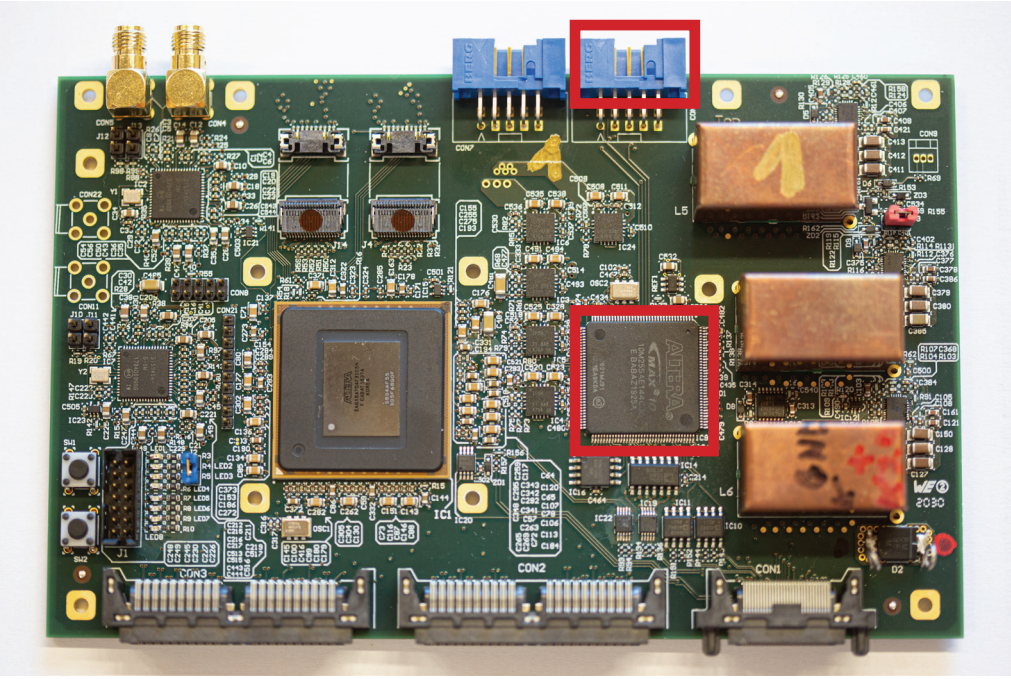
- Powering with three switching regulators with shielded air coils (plus some LDOs)
- Works fine for the ~15 W total consumption

Programming I:



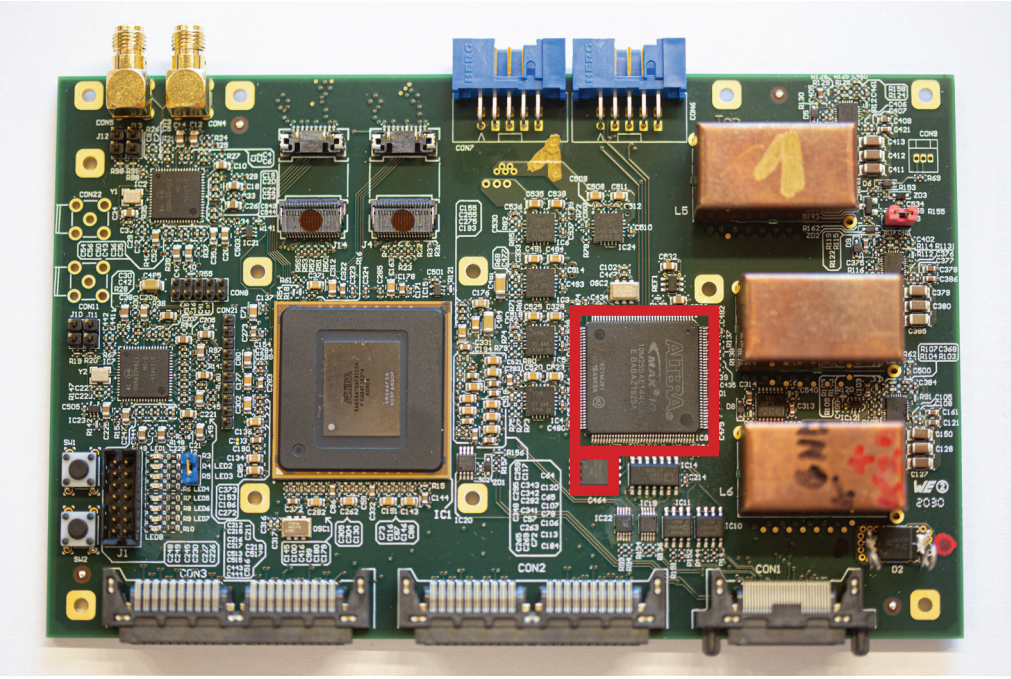
- The Arria V FPGA can be programmed via JTAG

Programming II:



- The MAX10 CPLD can be programmed via JTAG
- Both transient (SRAM) and permanent (Flash)

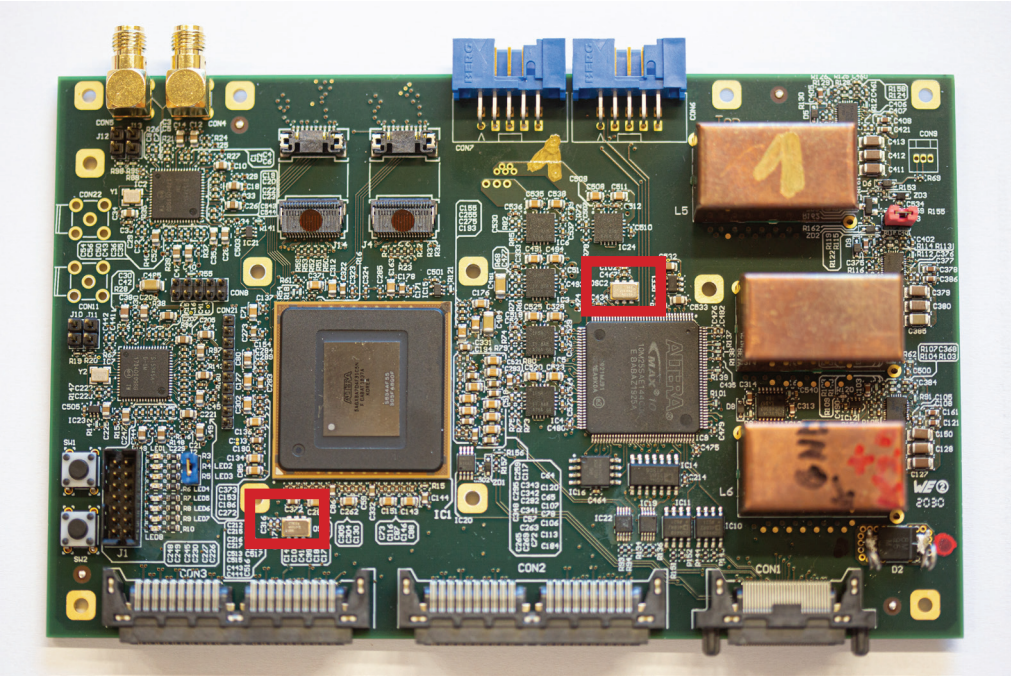
Programming III:



- The Arria controls the MAX to write configuration images to the SPI flash via optical input
- We can write to the SPI flash from the backplane via the MAX
- The MAX programs the Arria on startup using the image on the SPI flash

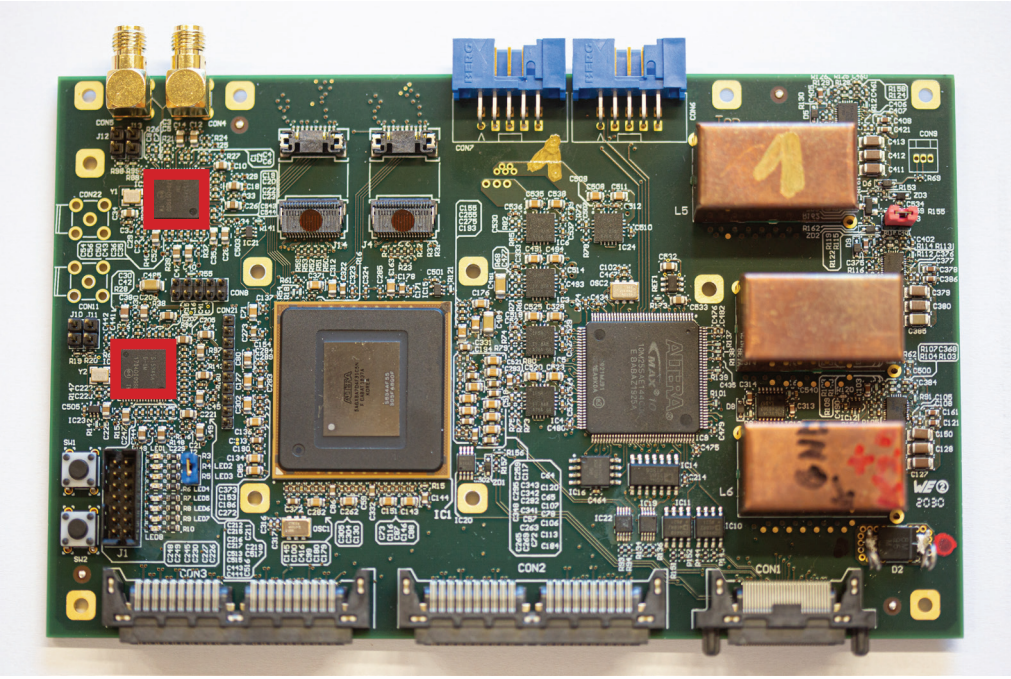
- Quad-SPI flash memory attached to the MAX10

Clocking I:



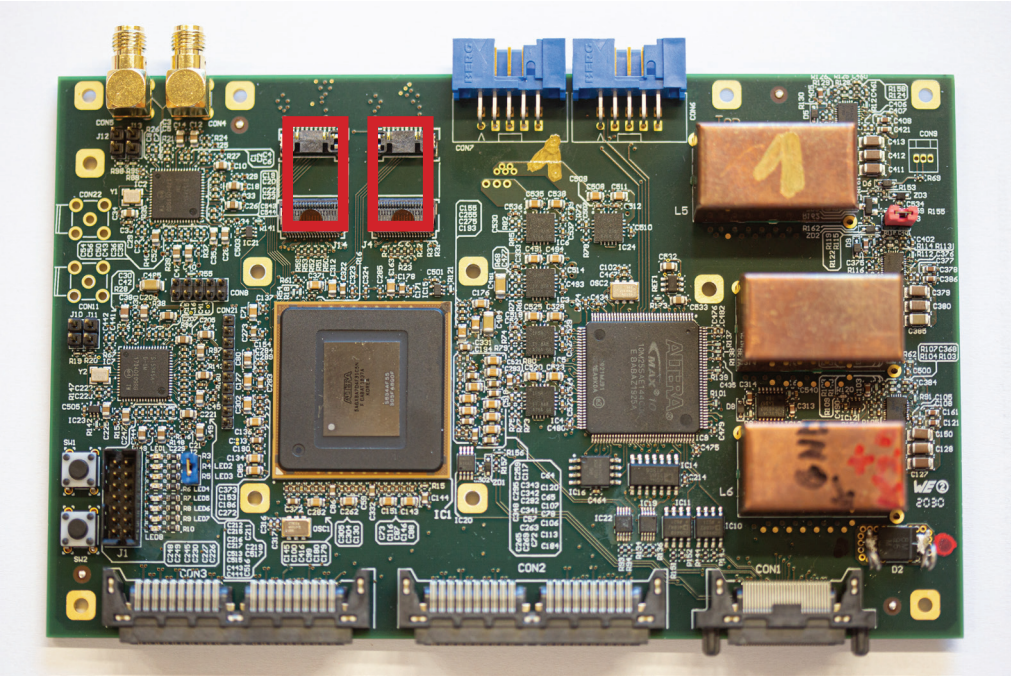
- On-board 50 MHz oscillators for startup and configuration of advanced clocking

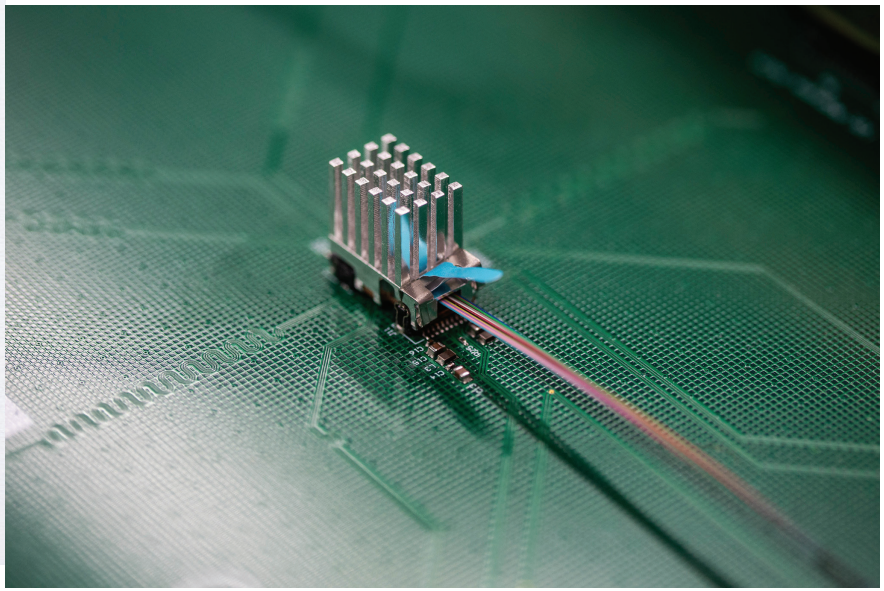
Clocking II:



- Two Si5345 jitter cleaners produce up to 20 clocks from optical or SMA input
- Synchronized to each other
- Five clocks with up to 625 MHz for the detector ASICs

Optical transceivers:

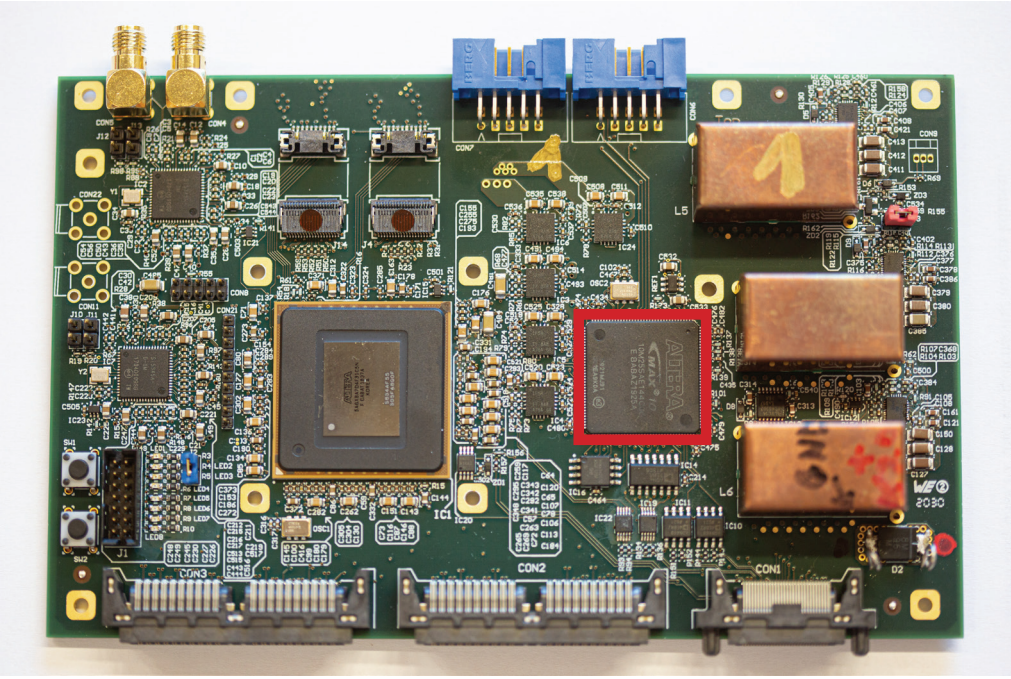




- Two Firefly 4RX/4TX transceivers
- One needed for operation:
  1 clock input (125 MHz, to Si)
  1 reset input (1.25 Gbit/s)
  1 control input (6.25 Gbit/s)

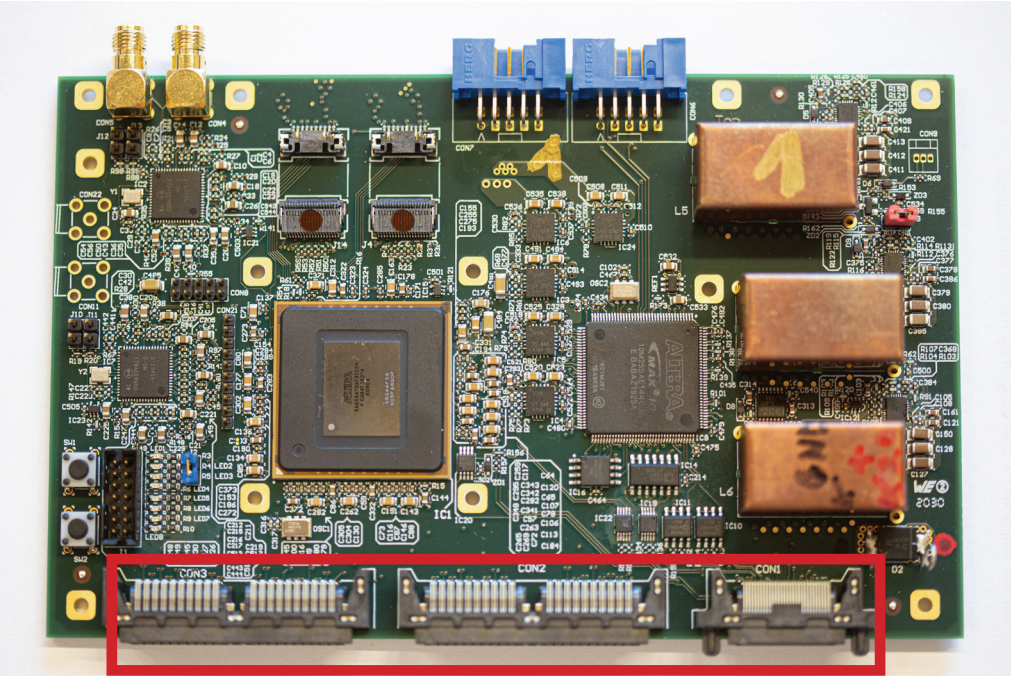
  1 data output (6.25 Gbit/s)
  3 spare outputs

Monitoring:



- MAX10 contains ADCs for temperature and voltage monitoring
- I2C and SPI interfaces to Fireflies and Si clock chips

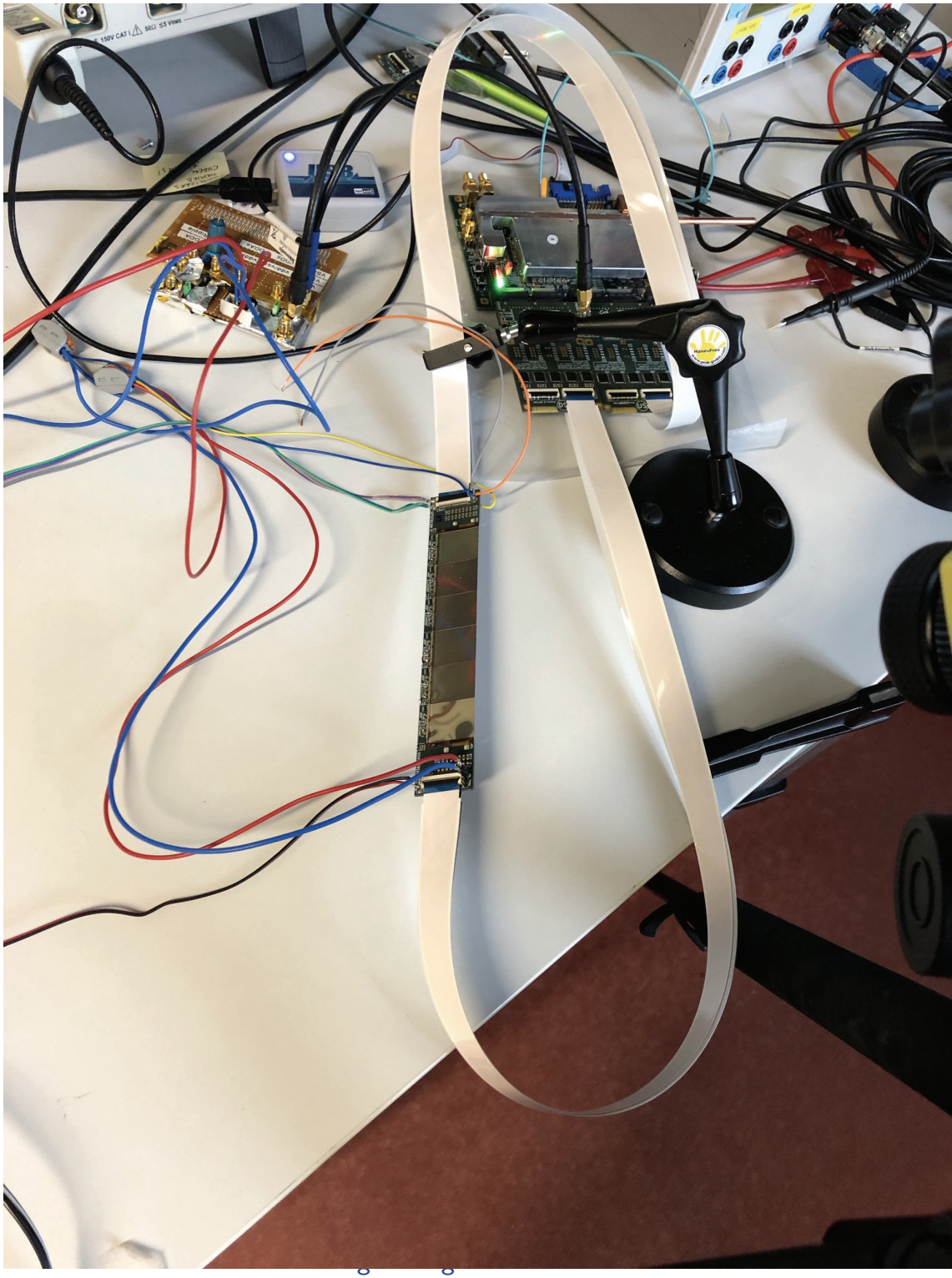
Backplane:



- Two connectors to the detector (MuPix/MuTrig)
- One for power and control signals
- Generic frond-end board, subdetector specific adapters on the other side of the backplane

Pixel readout

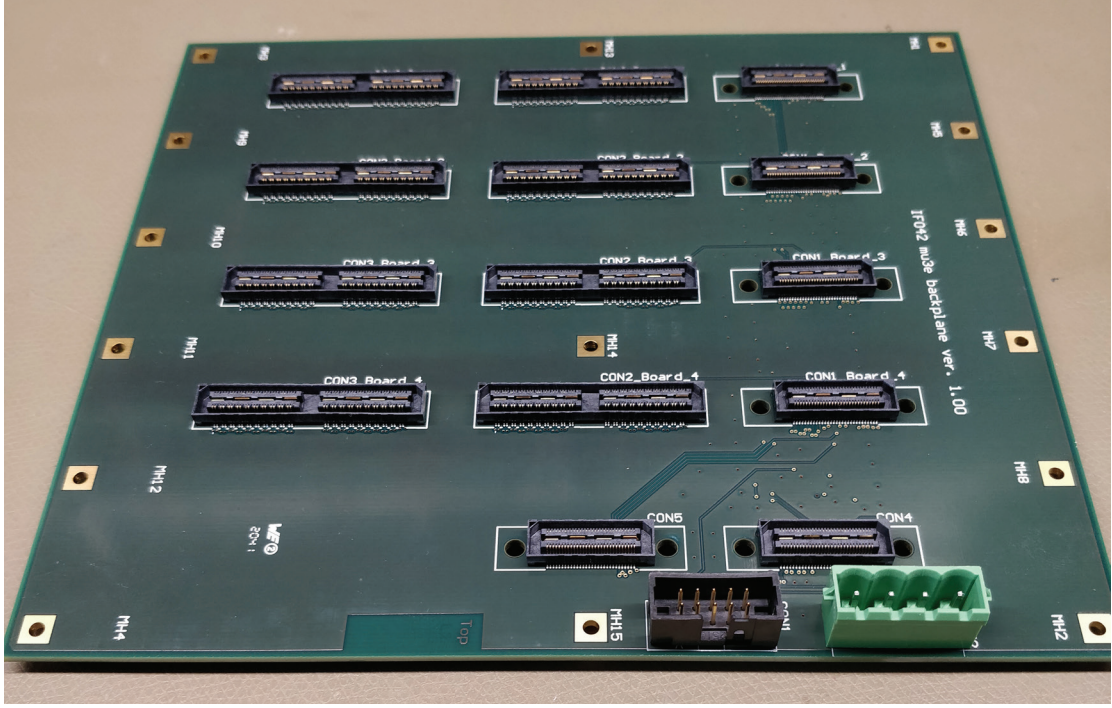
- Can configure and read MuPix ladders!

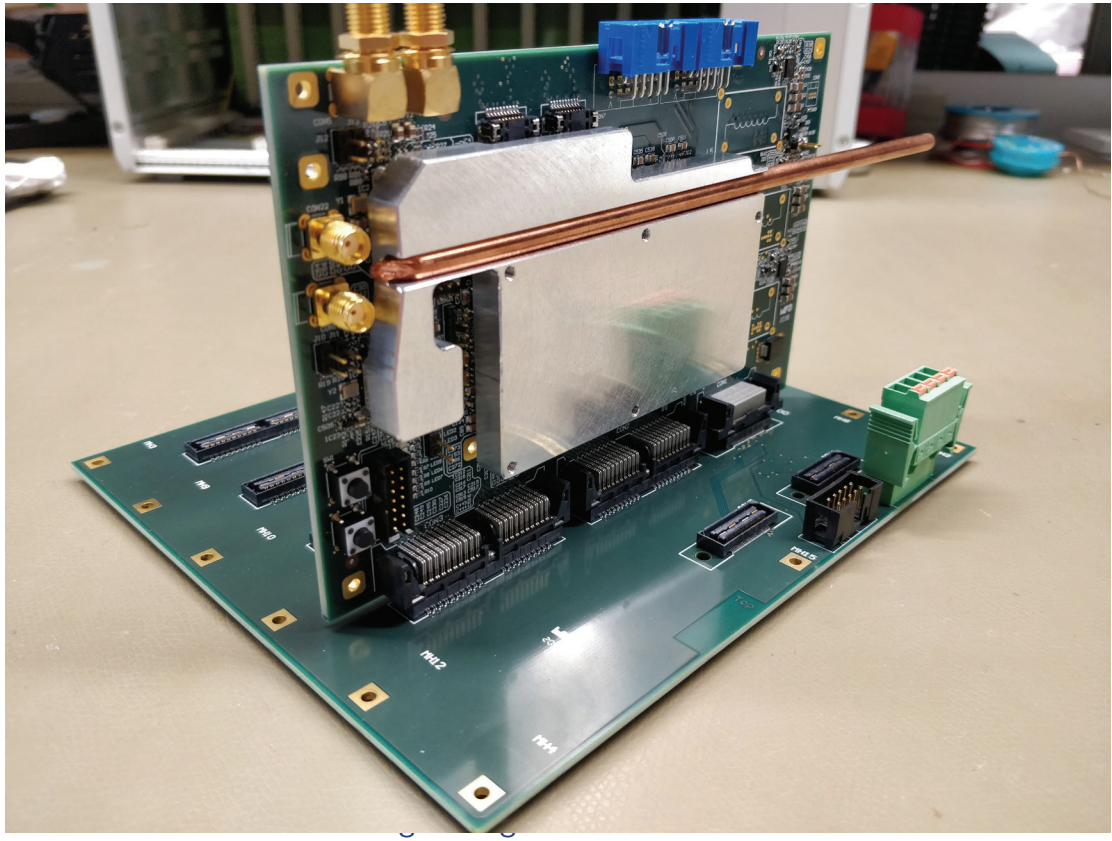


Front-end backplane

- Will combine up to 16 boards in a quarter-circular crate

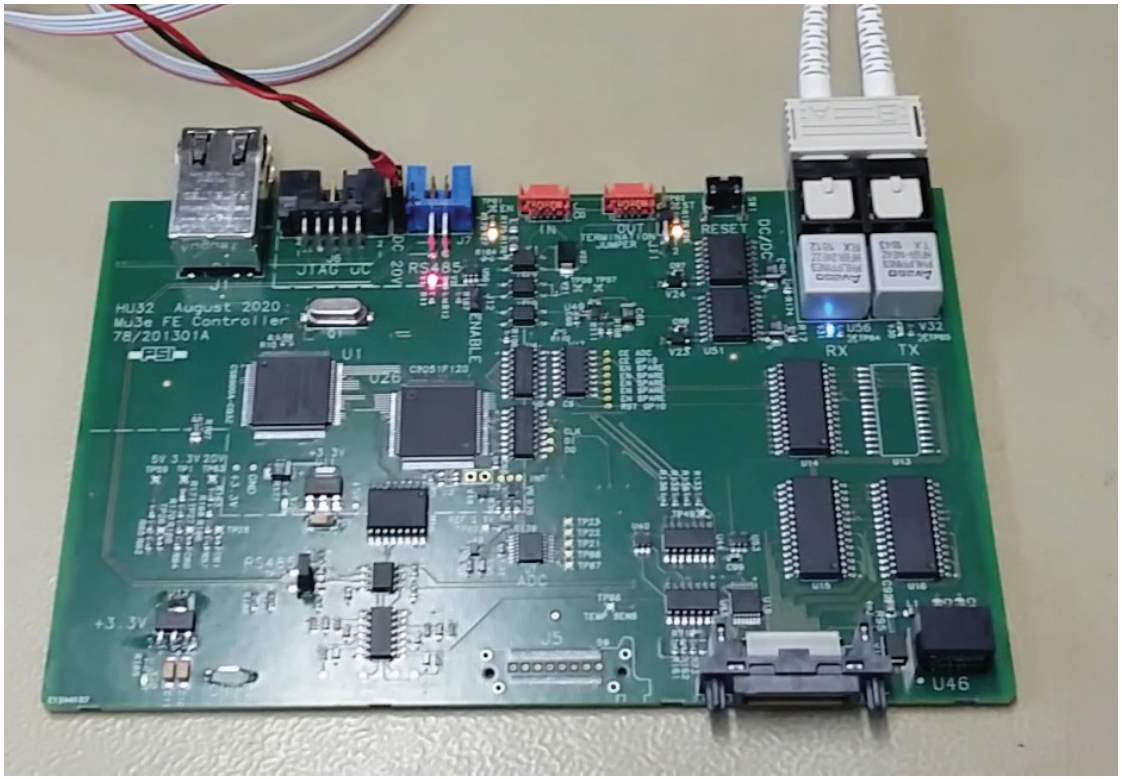
- Mini-backplane for lab tests and pilot run
- Holds four FEBs and a crate controller
- Designed in Heidelberg





Crate Controller

- Designed and produced at PSI (Ueli Hartmann)
- Microcontroller for monitoring, powering and programming front-end boards
- Communication via the MIDAS slow control bus with the outside world

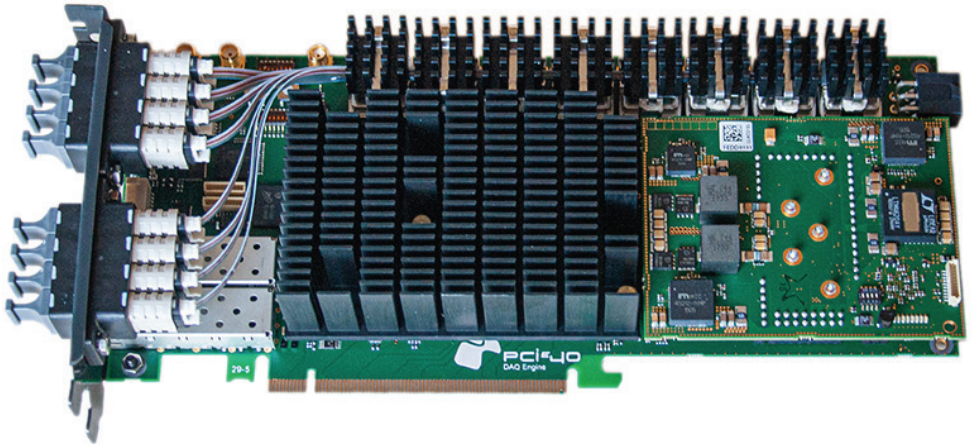


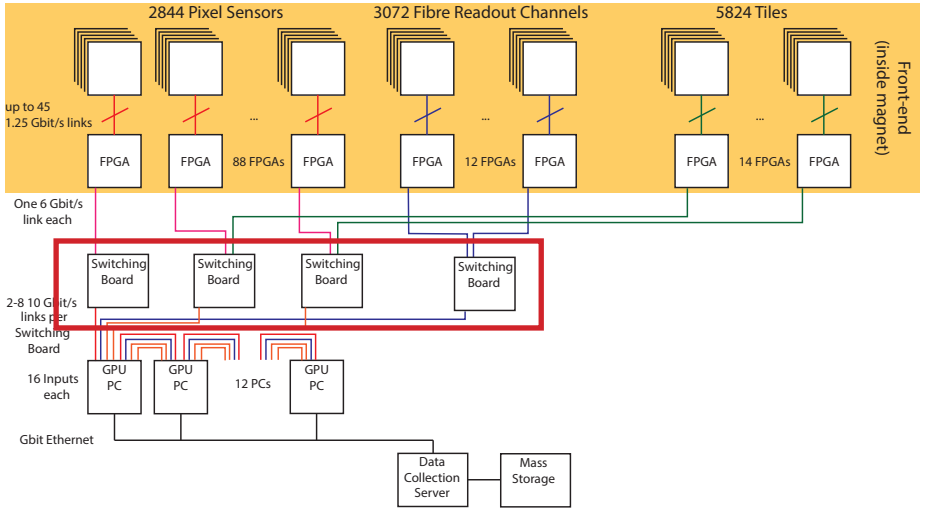
All together now...

- Crate with front-end board and crate controller
- Working well
- Also includes cooling infrastructure

Switching board

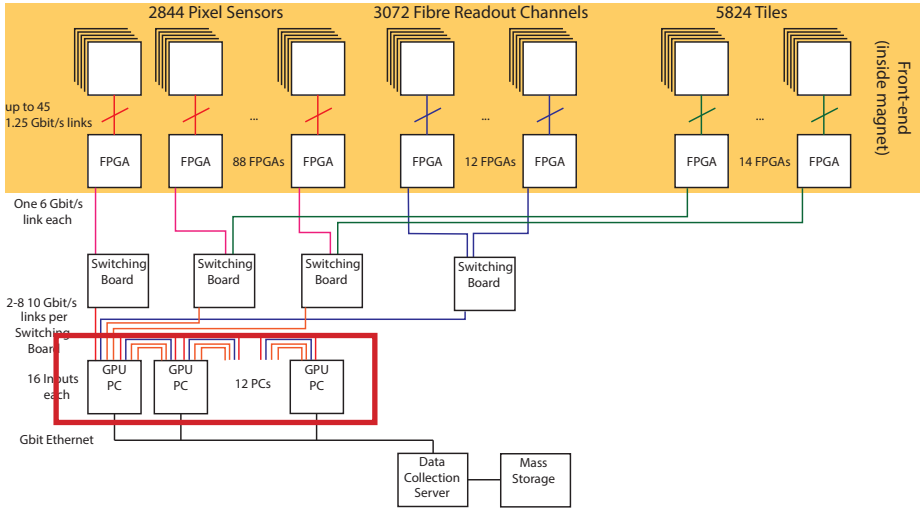
- Operates in a PC case
- Up to 37 front-end board inputs (and control lines)
- Up to eight 10 Gbit/s outputs to filter farm
- Use PCIe40 board developed in Marseilles for LHCb and ALICE upgrades
- Intel Arria 10 - 115 FPGA
- Avago MiniPod Transmitters and Receivers
- Two 8-lane PCIe 3.0 interfaces (used for control and monitoring data)



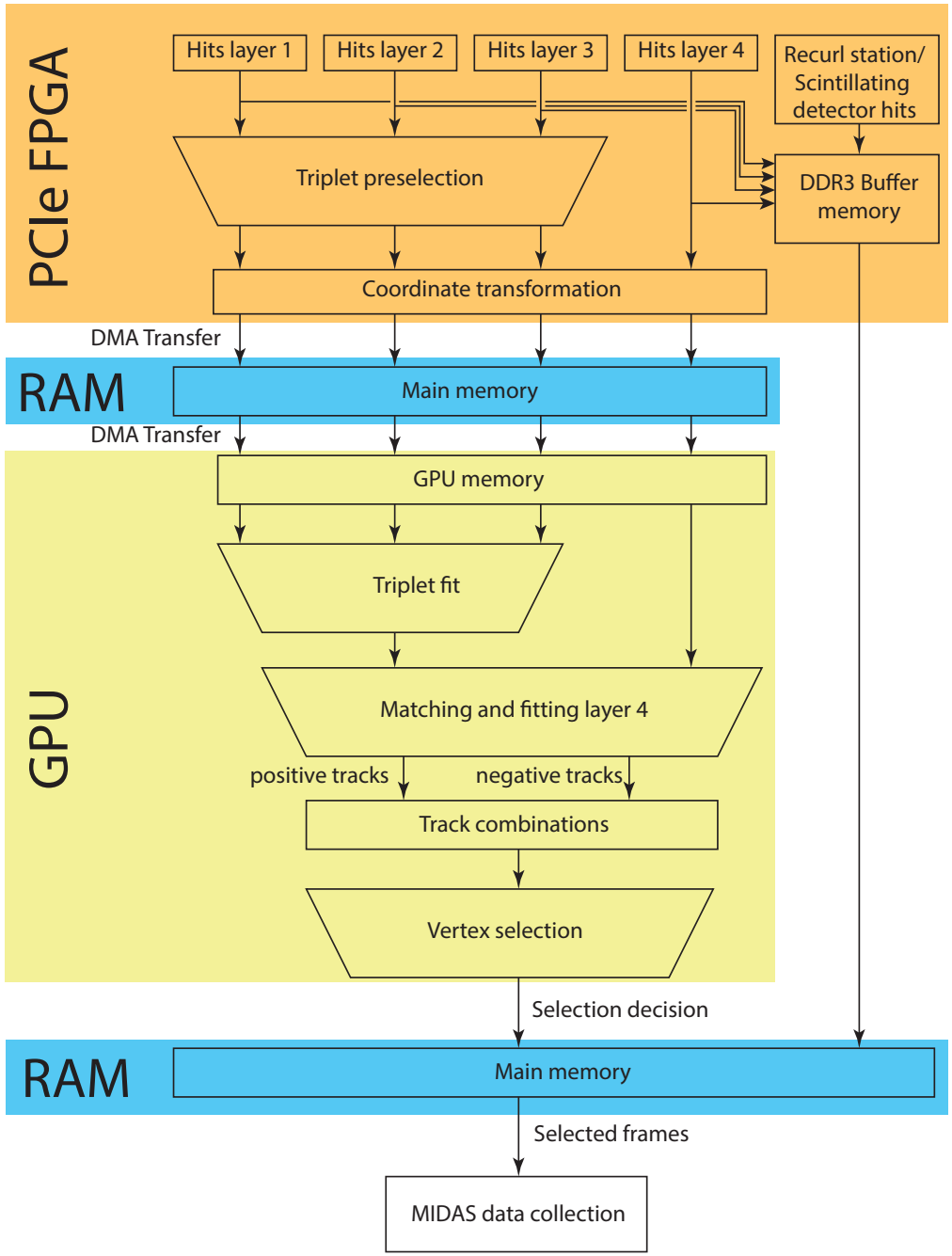


Receiving board

- Operates in a PC case, together with a GPU
- 16 10 Gbit/s inputs and outputs (daisy chain)
- Use commercial DE5A NET board from Terasic Inc.
- Intel Arria 10 - 115 FPGA
- DDR 3/4 memory for buffering
- QSFP Transmitters and Receivers
- 8-lane PCIe 3.0 interface



Farm data flow



- Buffer all incoming data in DDR memory
- Use subset from central detector for track and vertex finding on a GPU
- If interesting: Get full data from buffer, send to PC
- Up to 38 Gbit/s PCIe DMA transfers using custom firmware and driver
- After full reconstruction: Send off to mass storage

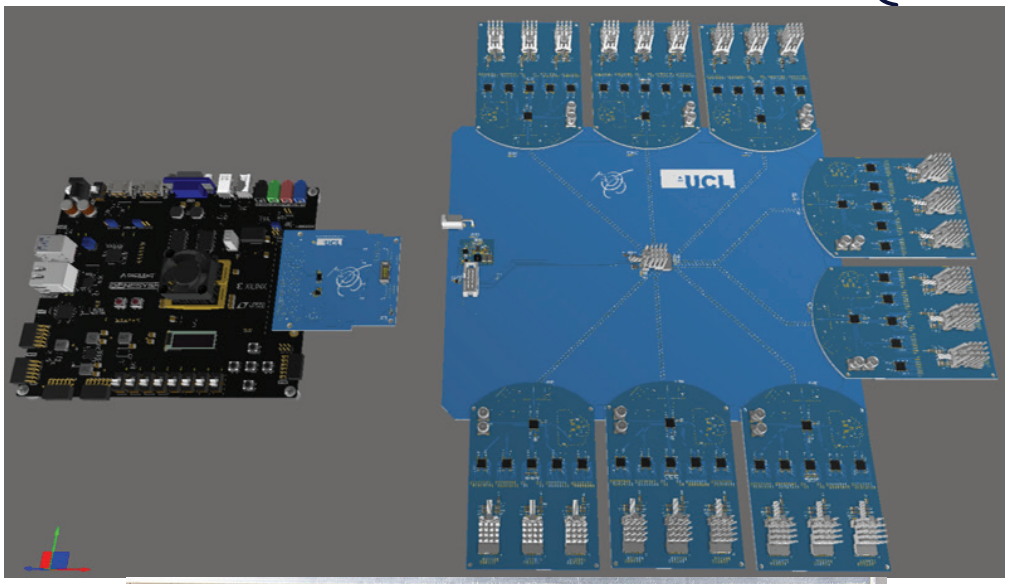
GPU reconstruction

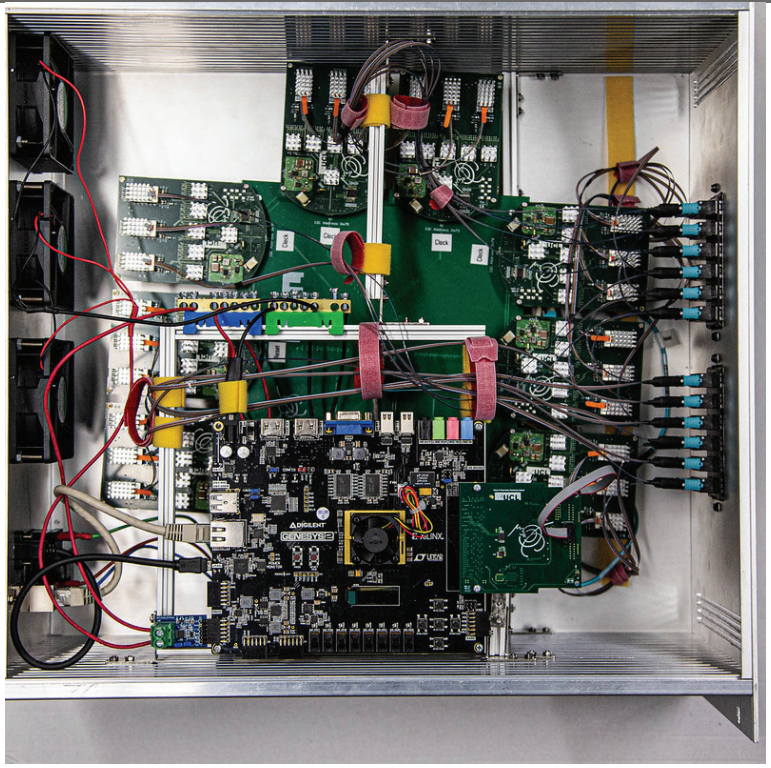
- GPU reconstruction on gaming cards
- Have achieved > 10^9 track fits/s per GPUs (Nvidia GTX 980)
- Twelve GTX 1080Ti are sufficient for dealing with 10^8 muon decays/s

- Excited about the possibilities with the latest cards...
- (and somewhat bummed that it is so hard to buy cards right now)

System synchronization

- Produce 144 copies of the 125 MHz system clock
- Produce 144 copies of the 1.25 Gbit/s, 8bit/10bit encoded reset and state transition signal
- Digilent Genesys FPGA board
- Samtec Firefly optical transmitters





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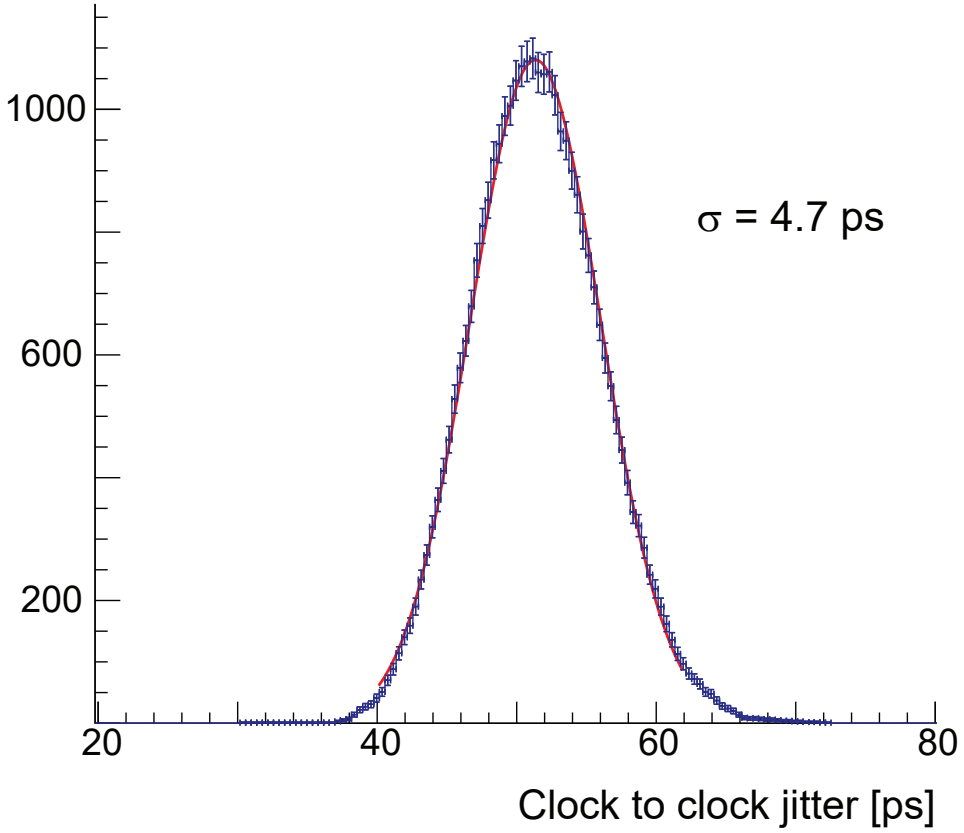
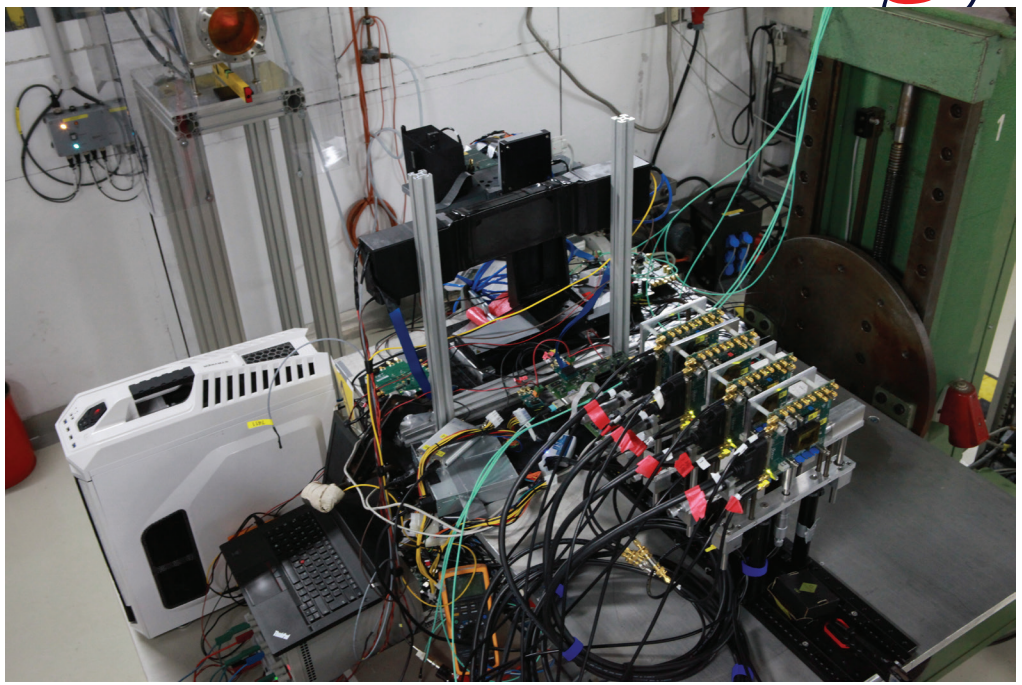
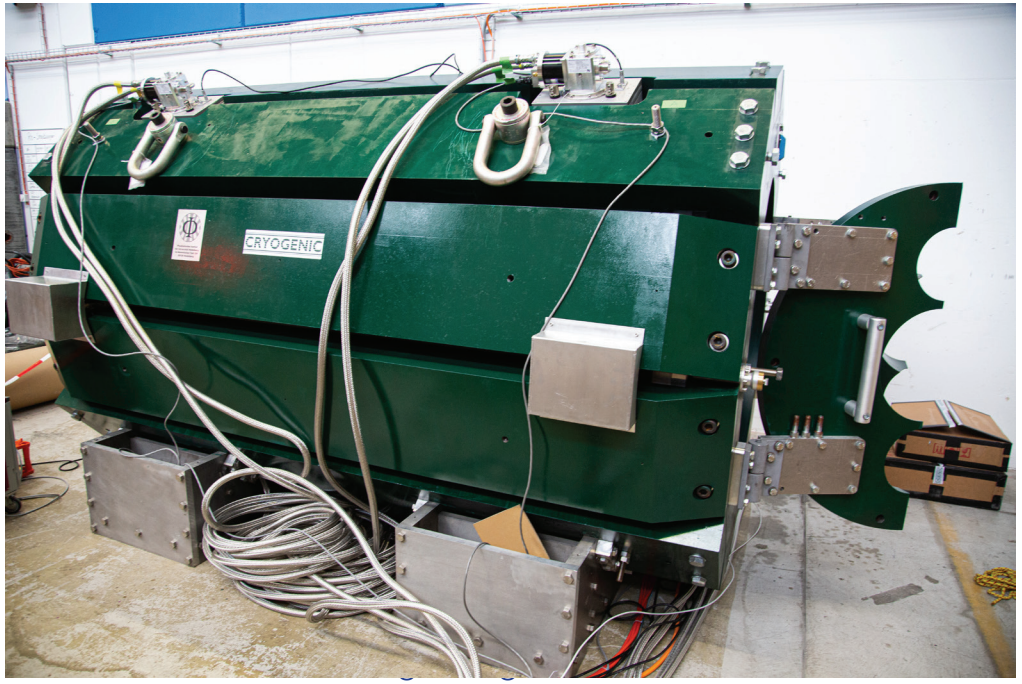
- Samtec Firefly optical transmitters
- Less than 10 ps clock-to-clock jitter



Current status

- All commercial components available and tested
- All detectors have been read out via a prototype front-end board
- Detector integration run inside magnet next month
- Full production of front-end boards and commissioning this year:
  Mu3e DAQ ready end of 2021
- Farm to be ready by end of 2022





Example for a firmware algorithm: Hit Sorting

Motivation

The MuPix chips read the "lowest" hit from each column per readout cycle:

- Hits are streamed out of time-order
- A streaming DAQ system needs data reasonably time-ordered
- Do sorting on the Front-End Board (also main motivation for choice of "large" FPGA)
- Need to do sorting in real time
  - essentially O(N) even tough the best sorting algorithms are O(N log N):
  There are potential losses

History

Sorter firmware was always a concern

- Two versions implemented by Ann-Kathrin Perrevoort Heidelberg Phd student), well documented in her thesis
- Used in most MuPix beam tests since, no problems even at very high rates (if the chip is fast enough)
- Concern here: Can I sort the hits from 15 MuPixes with 3 LVDS links each and also use the sorter to do the 45 -> 1 multiplexing?

Idea

- Memory with some slots for each timestamp
- Put hits there
- Know where there are hits
- Read them in order

Idea

- Memory with some slots for each timestamp
  (ok, the Arria V A7 has about 13 MB, we use a large part of this)

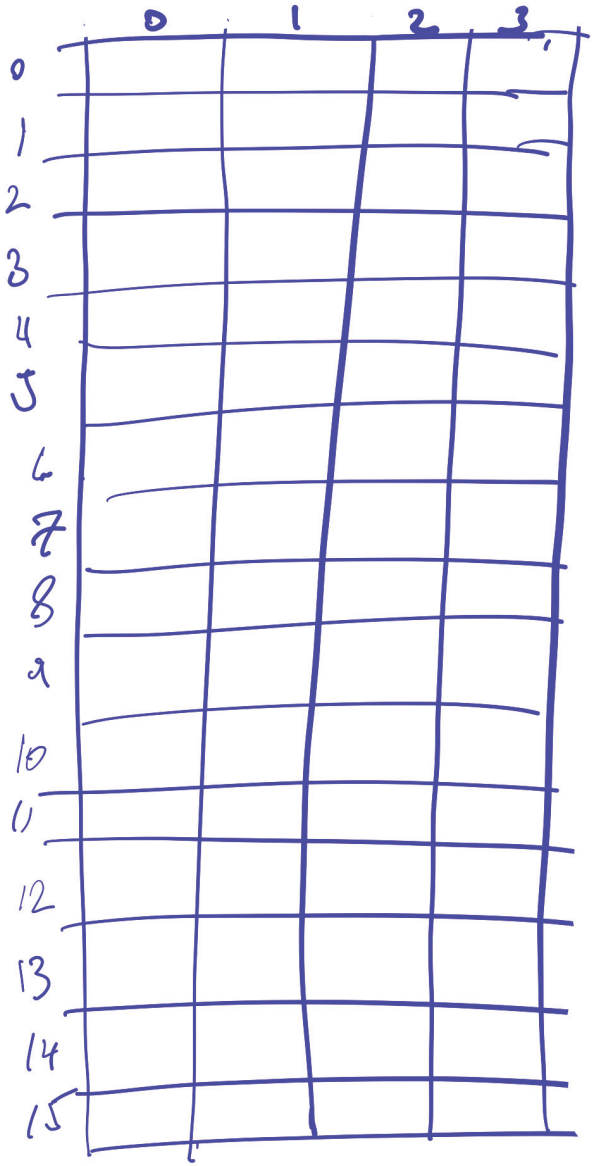
- Put hits there
  (very straightforward)

- Know where there are hits
  (naively implemented, explodes - use about 220'000 ALMs, 180'000 available)

- Read them in order
  (naively implemented, results in gigantic multiplexers, screwing up the timing)

Hit memories

- Also in old implementations:
  Use the MuPix protocol that takes four 125 MHz cycles to transmit 1 hit:
  Can do 4-1 (for the inner layers use 3-1) multiplexing: 15 instead of 45 inputs
- 15 memories with 16 slots each for 2048 timestamps (11 bit, MuPix10)



Hit memories

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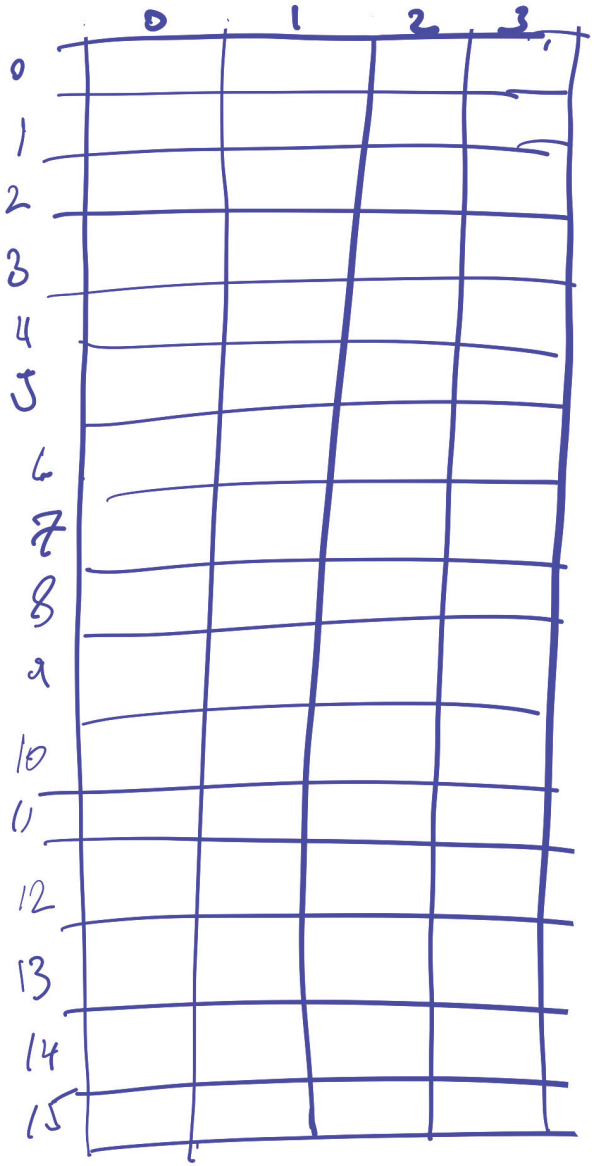
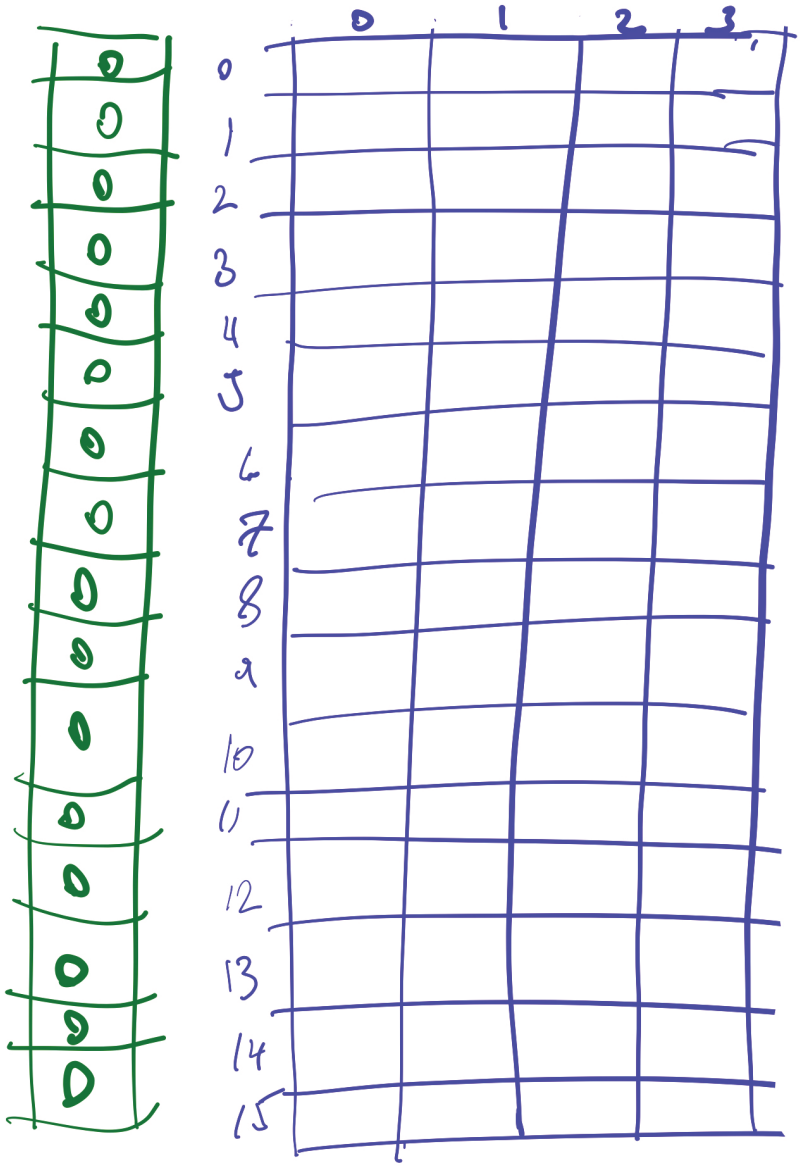
  Can do 4-1 (for the inner layers use 3-1) multiplexing: 15 instead of 45 inputs
- 15 memories with 16 slots each for 2048 timestamps (11 bit, MuPix10)
- Timestamp is encoded in address, save only 21 bits
- Now: Need to keep track how many hits were written per input and timestamp



Counting

- Need a lot of counters: 2048 x 15 x 4 bit plus overflow bit
- Need to multiplex them all for reading
- Does not fit in chip and is too slow



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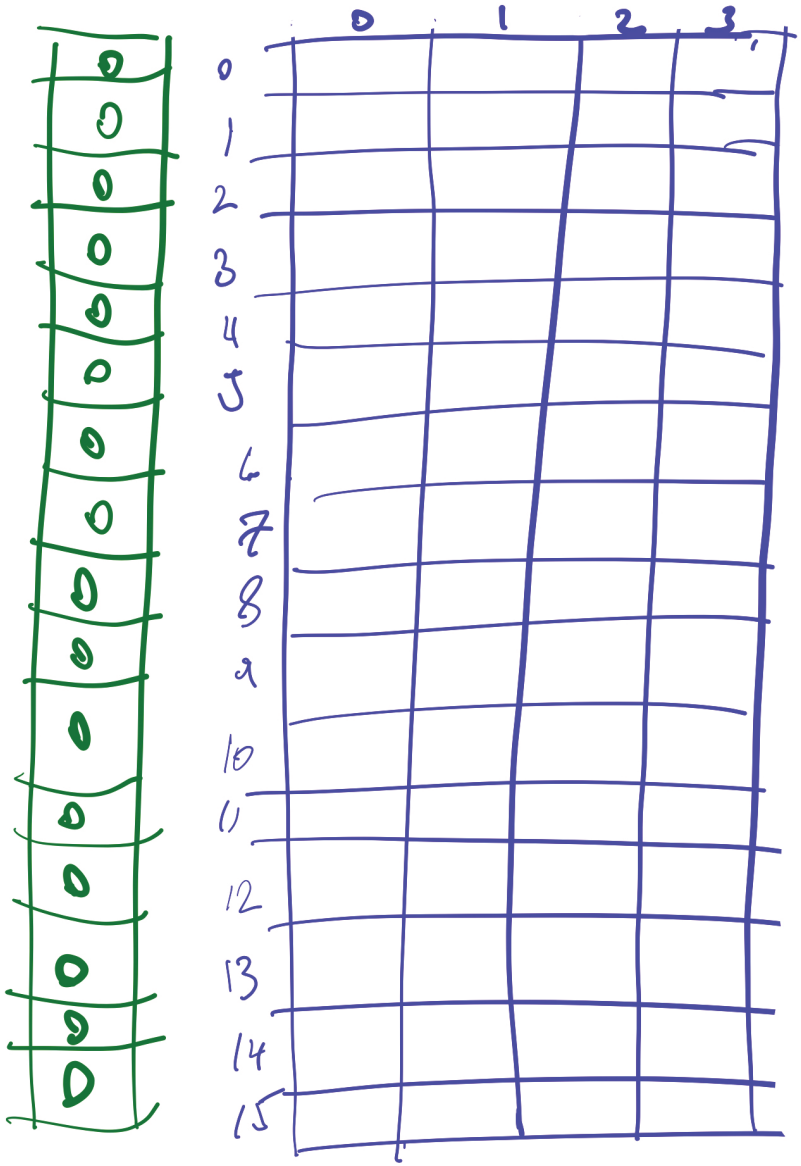

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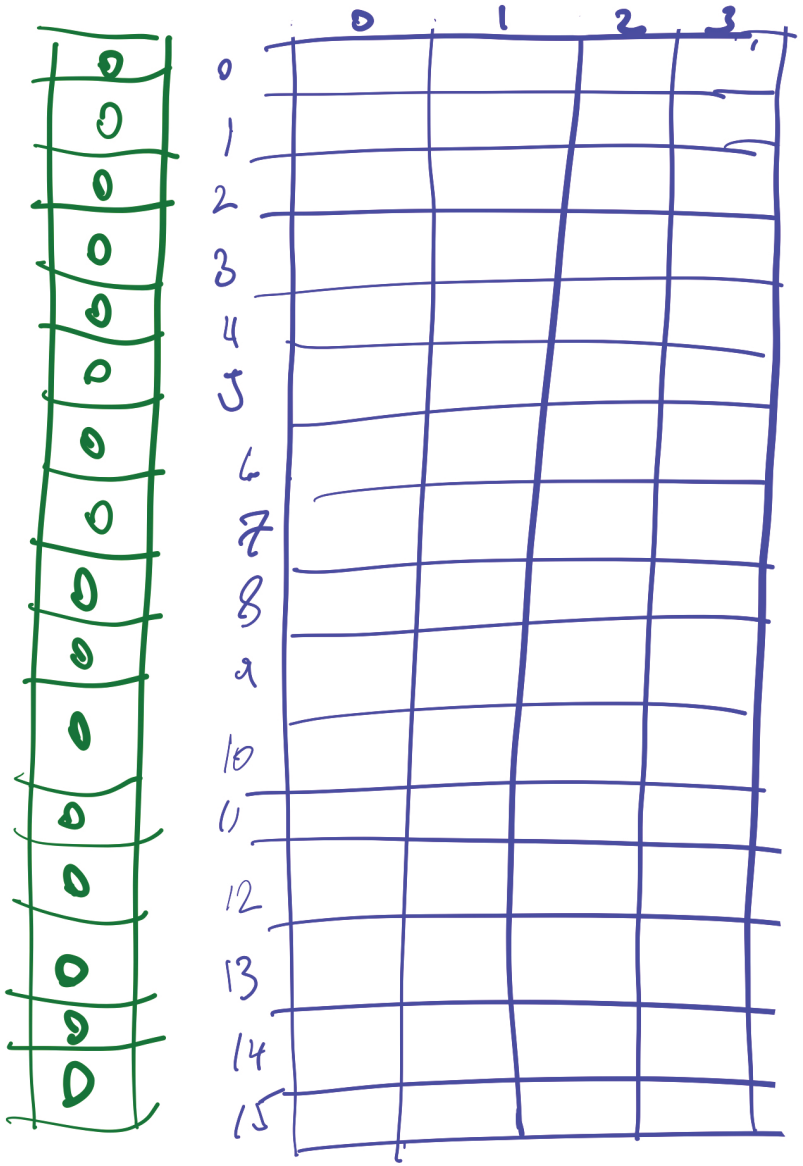
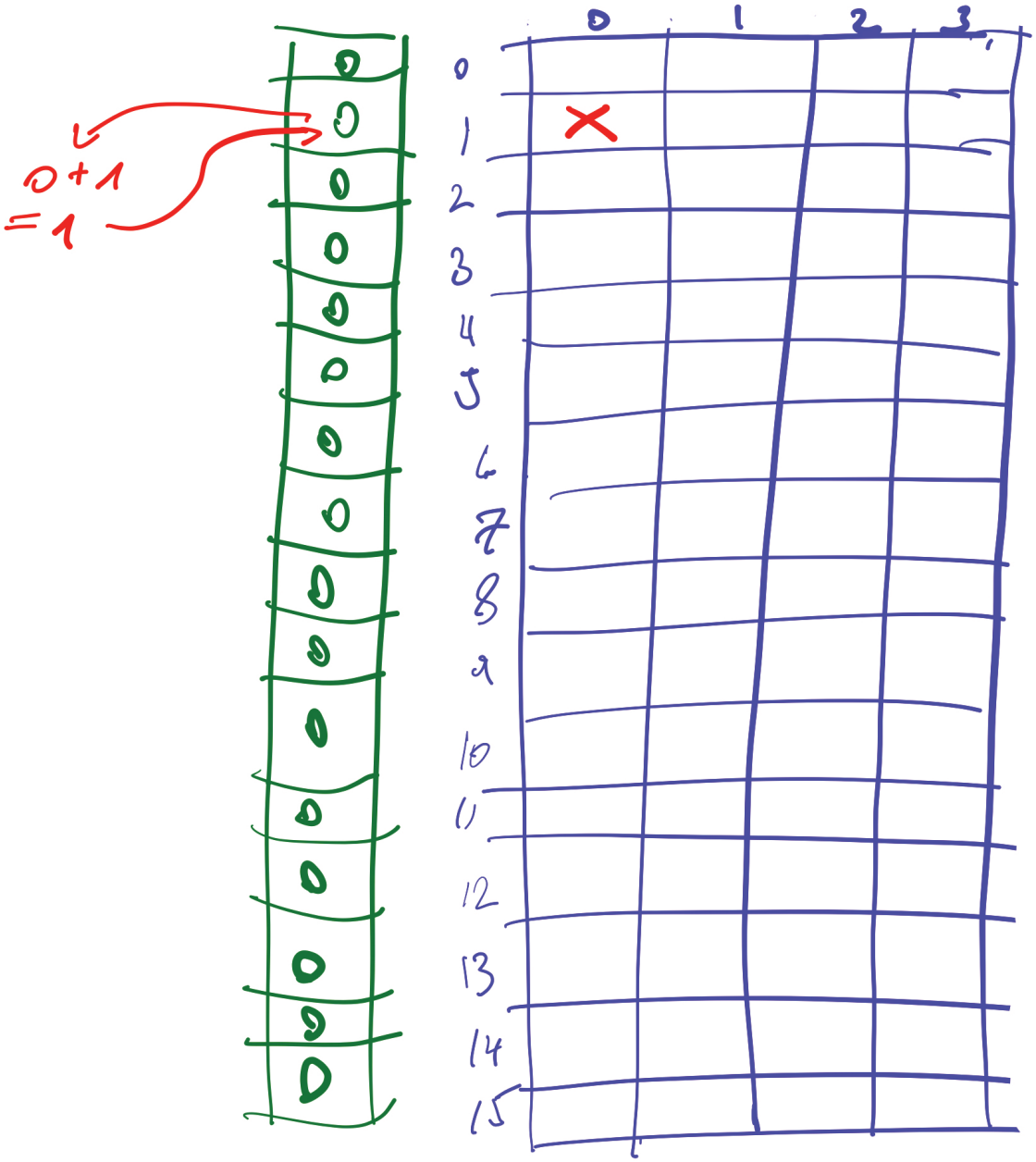
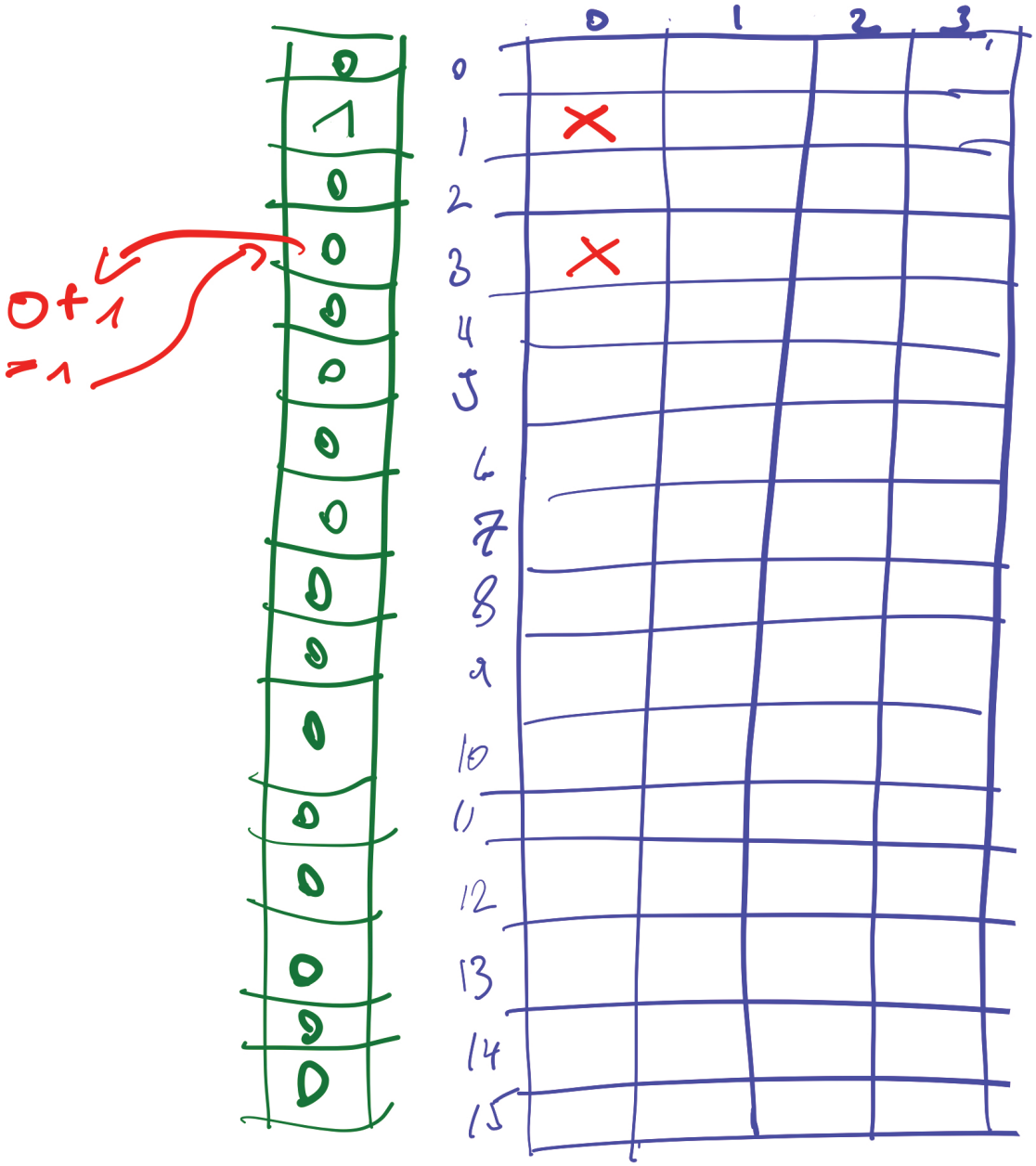
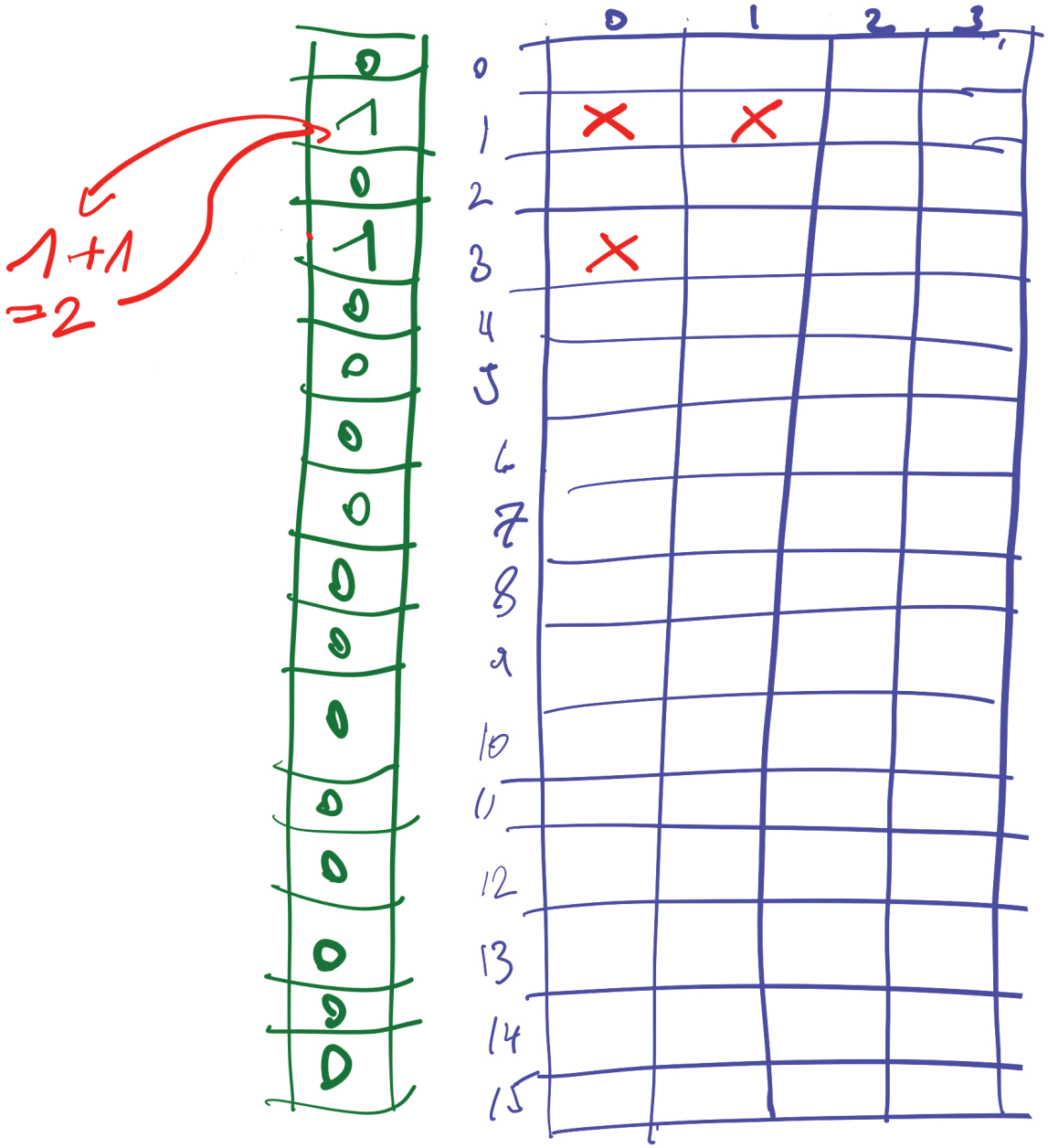
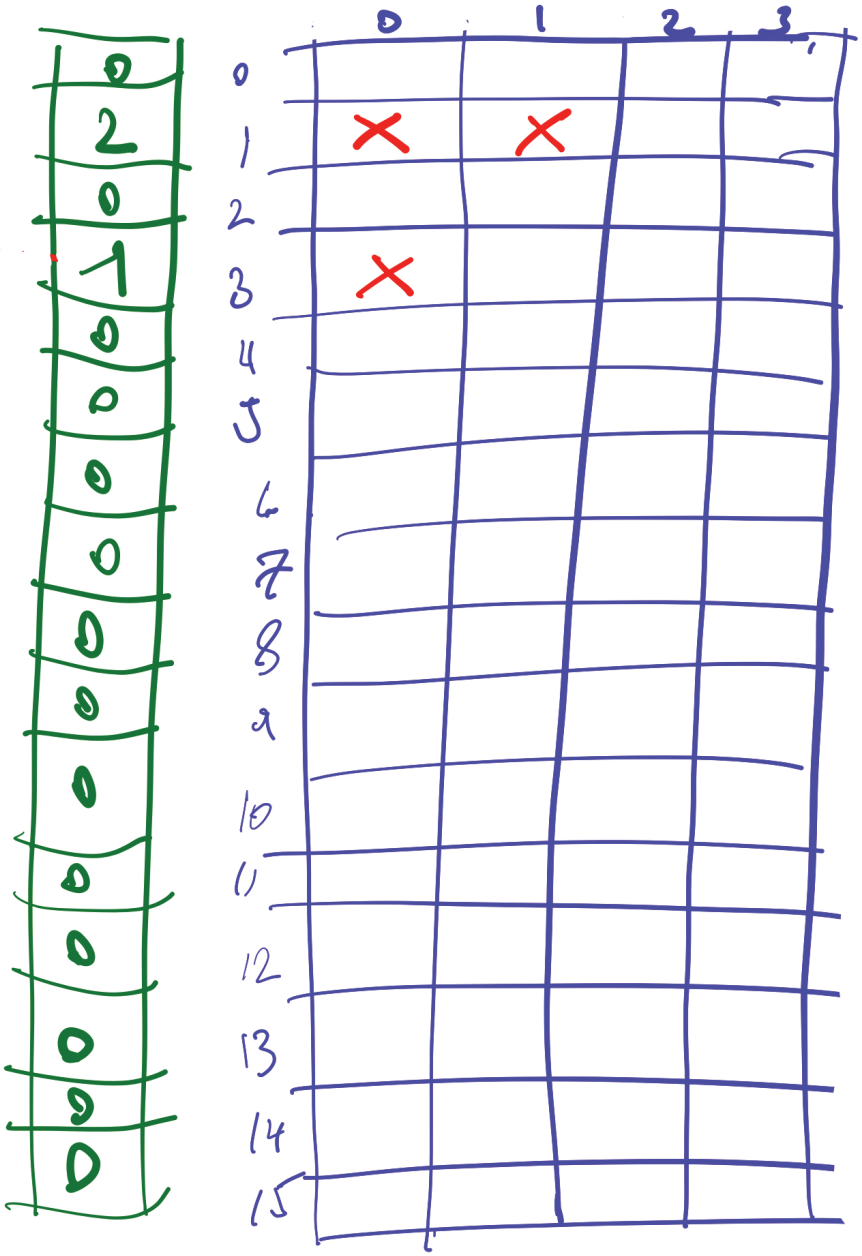



0+1
=1
0
1
2
3
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15


0 1 2 3
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
0+1
=1


1+1
=2
0
1
2
3


0
2
0
1
0
0
0
0
0
0
0
0
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0
0
0
0
0
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1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Counting

- Need a lot of counters: 2048 x 15 x 4 bit plus overflow bit
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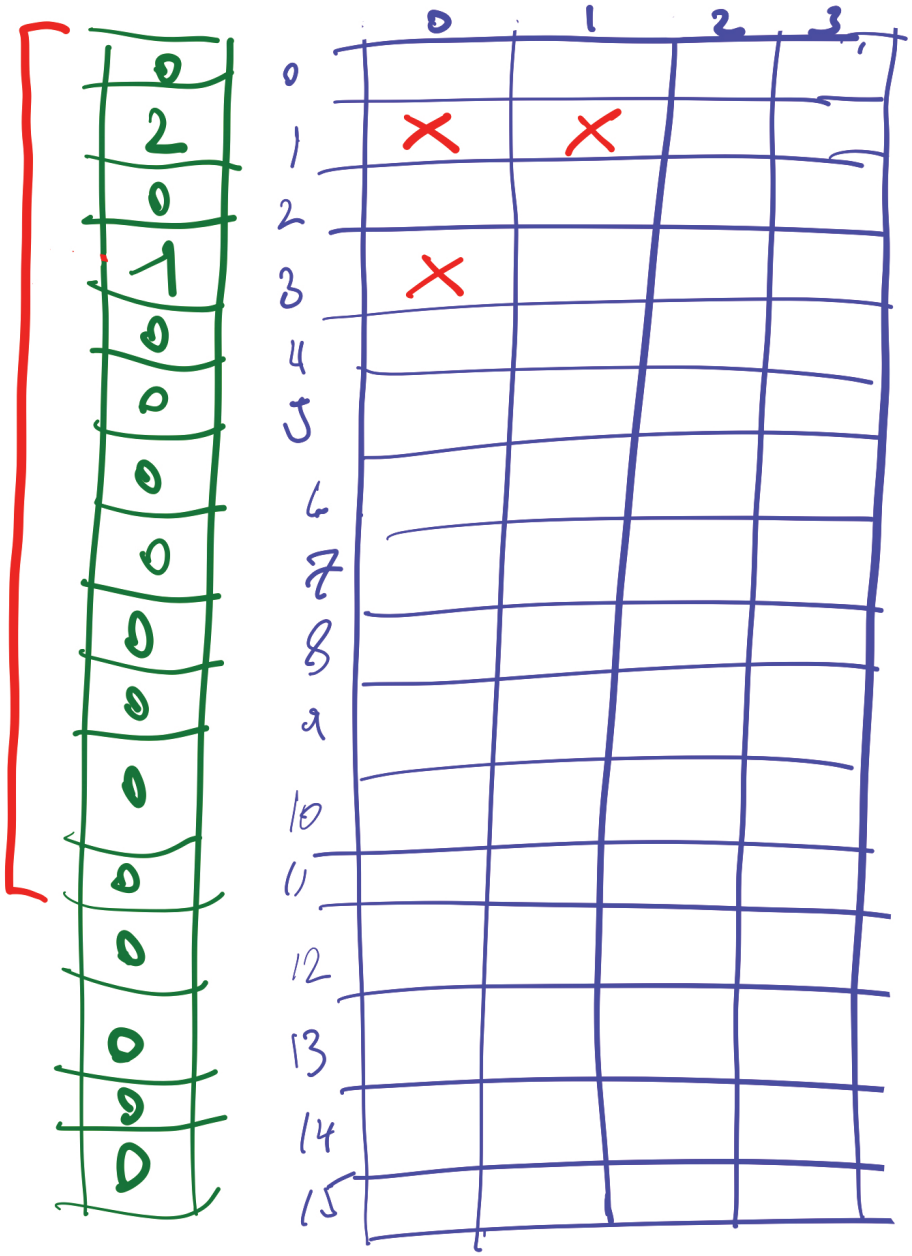
- Already suggested by Ann-Kathrin: Use a memory for the counters

- Works beautifully, somewhat trick due to read-modify-write over three cycles (need some "caching") and clearing after reading (not enough memory ports)

- Caching is a few lines of VHDL and a few dozen registers
- Clearing can be solved by splitting counter memory into blocks of timestamps - some are active for incrementing hit counts, some for reading hit counts and overwriting with zero
- Allows for 3/4 or 7/8 of all timestamps to be writeable at a given time
- Read hit counts for each timestamp; if timestamp runs at 250 MHz and FPGA at 125 MHz, read an even and an odd timestamp at the same time


0
2
0
1
0
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0
0
0
0
0
0
0
0
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0
0 1 2 3
0
1
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4
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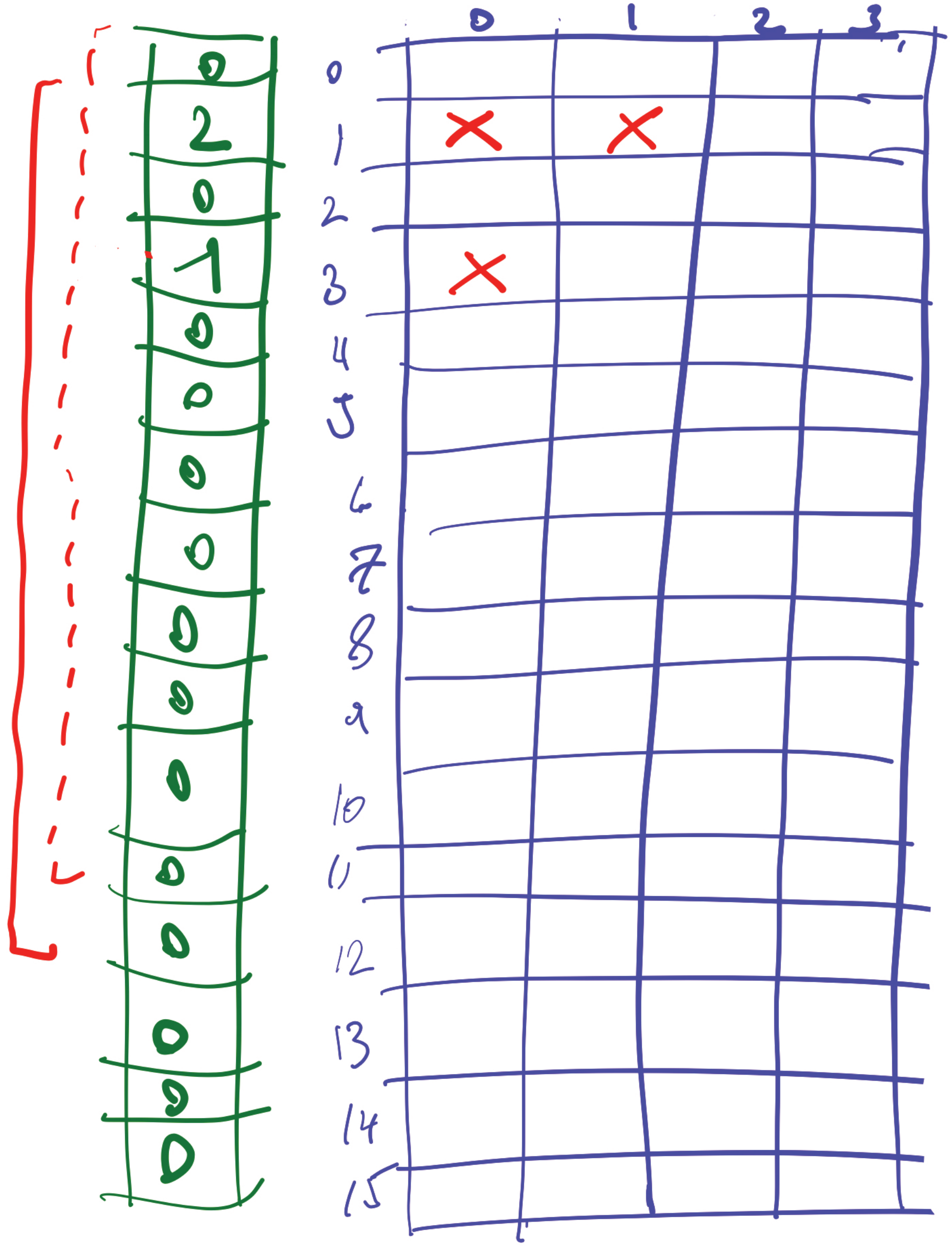
14
15


0
2
0
1
0
0
0
0
0
0
0
0
0
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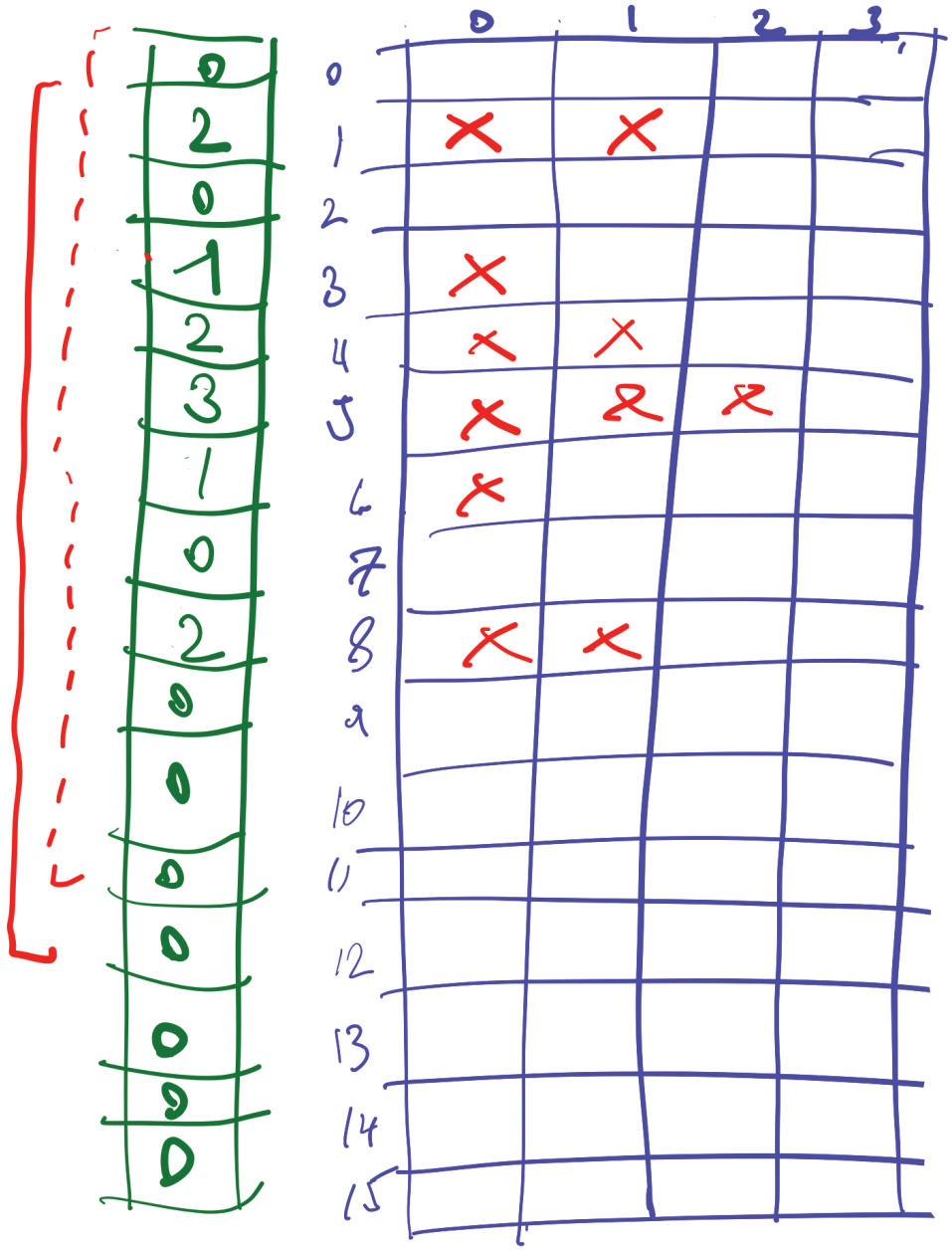
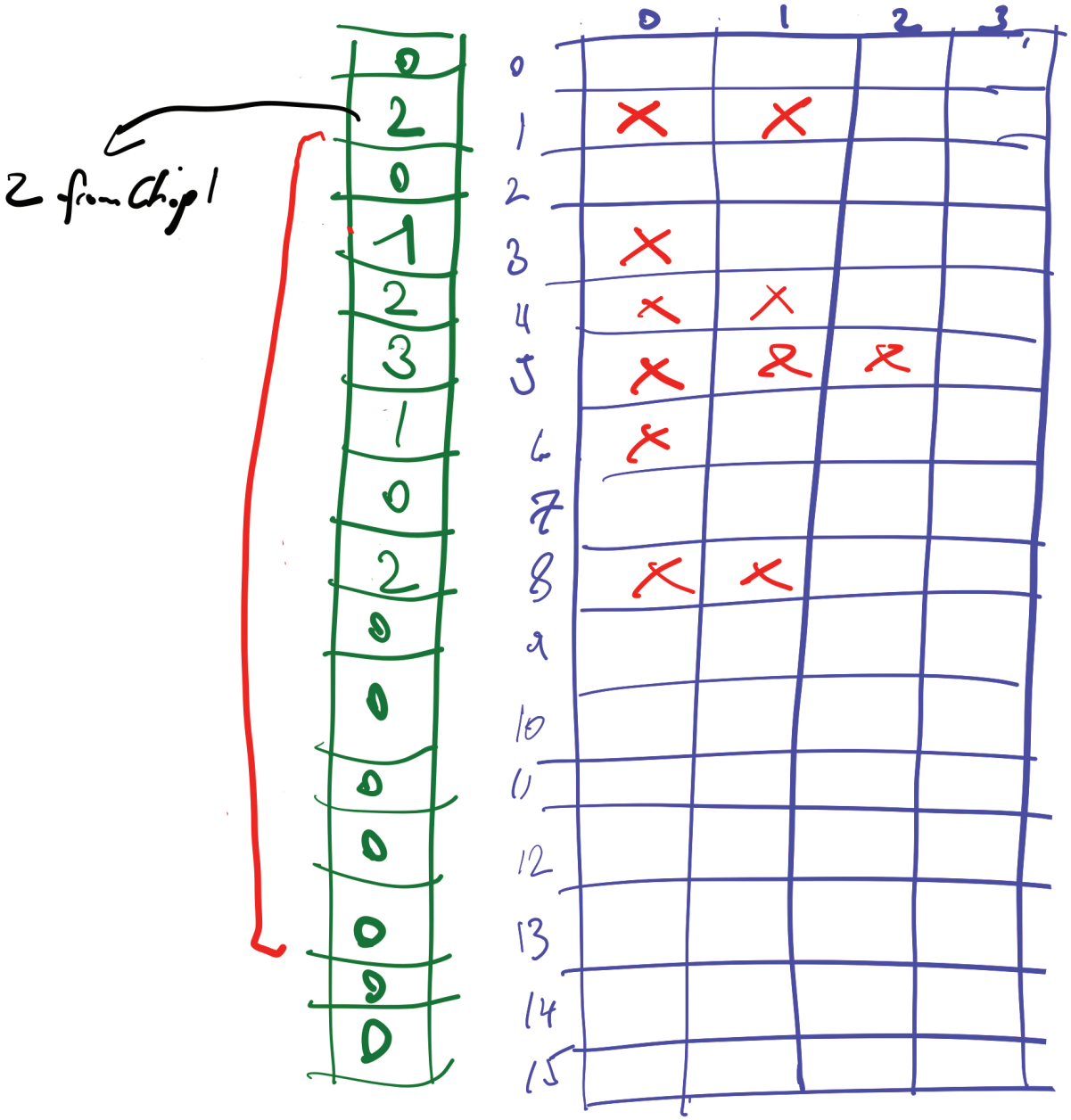
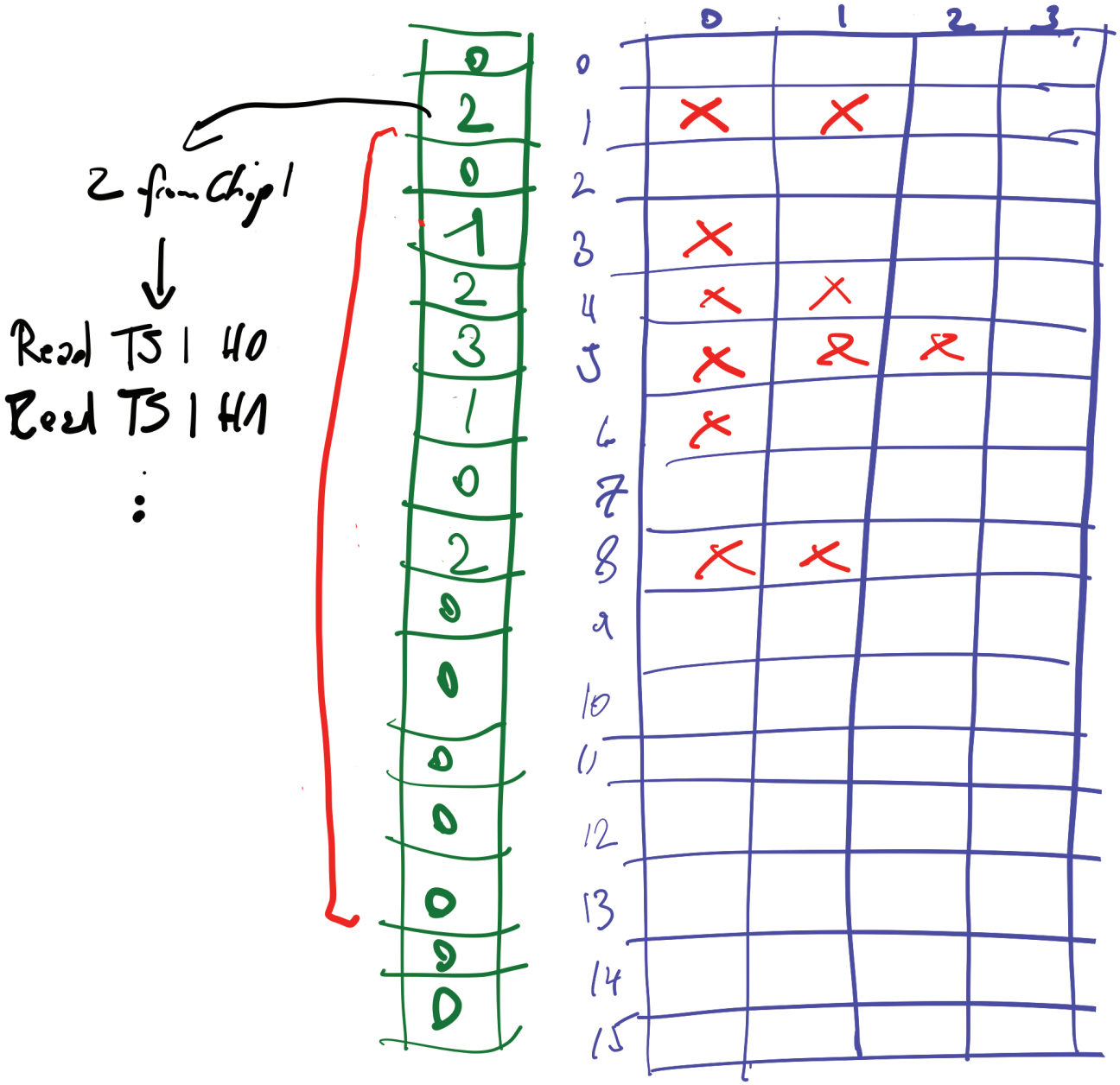
0
0
0 1 2 3
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15


0 1 2 3
0 2 0 1 2 3 1 0 2 0 0 0 0 0
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Generating read sequence

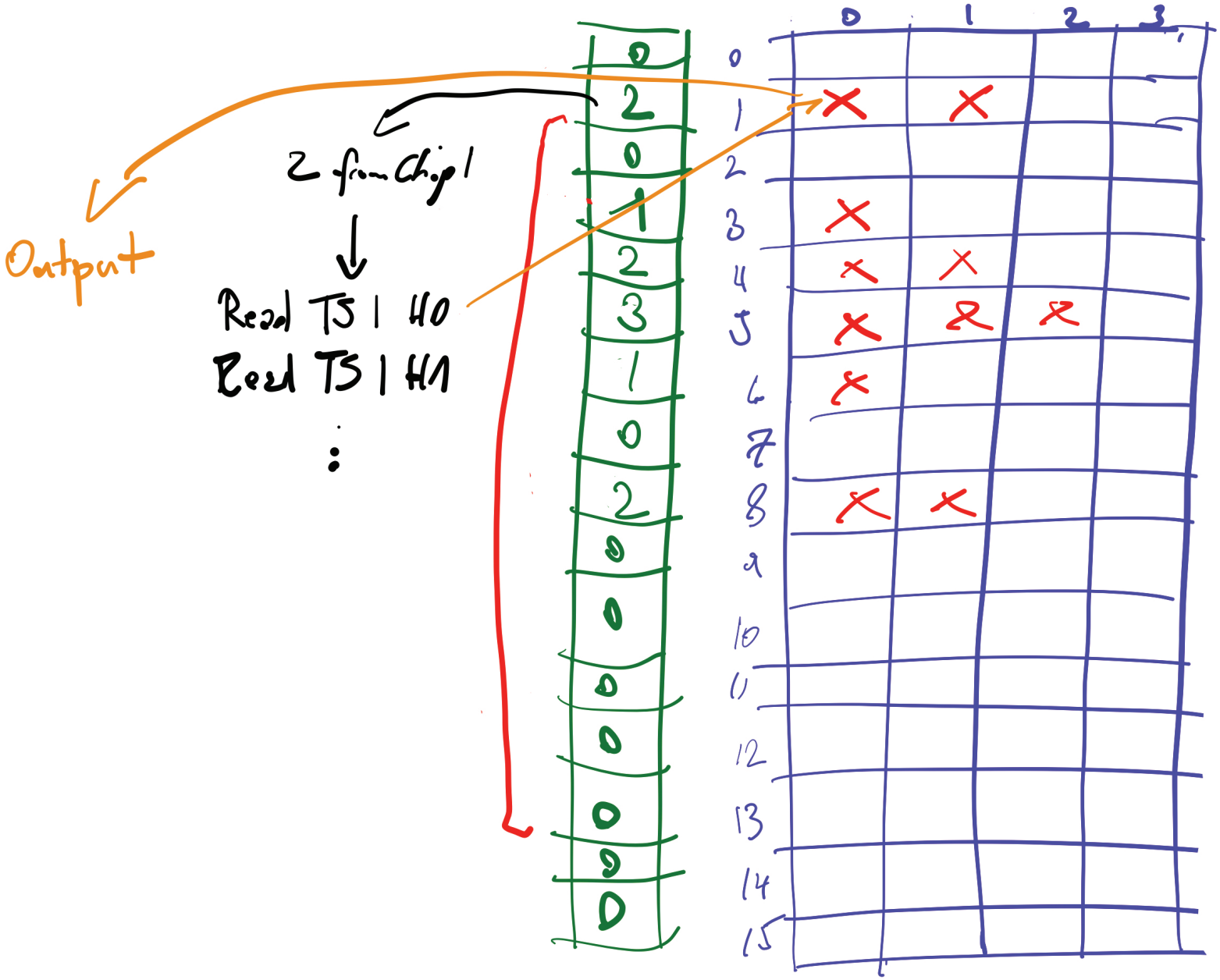
- From the counters, generate a sequence of how many hits are to be read from which timestamp from which input
- In this step, we can also identify timestamps with too many hits or if we are falling behind the writing with the reading:
  Skip timestamps, mark them as overflown, catch up
- Several mechanisms available (hard limits, credits, ...)

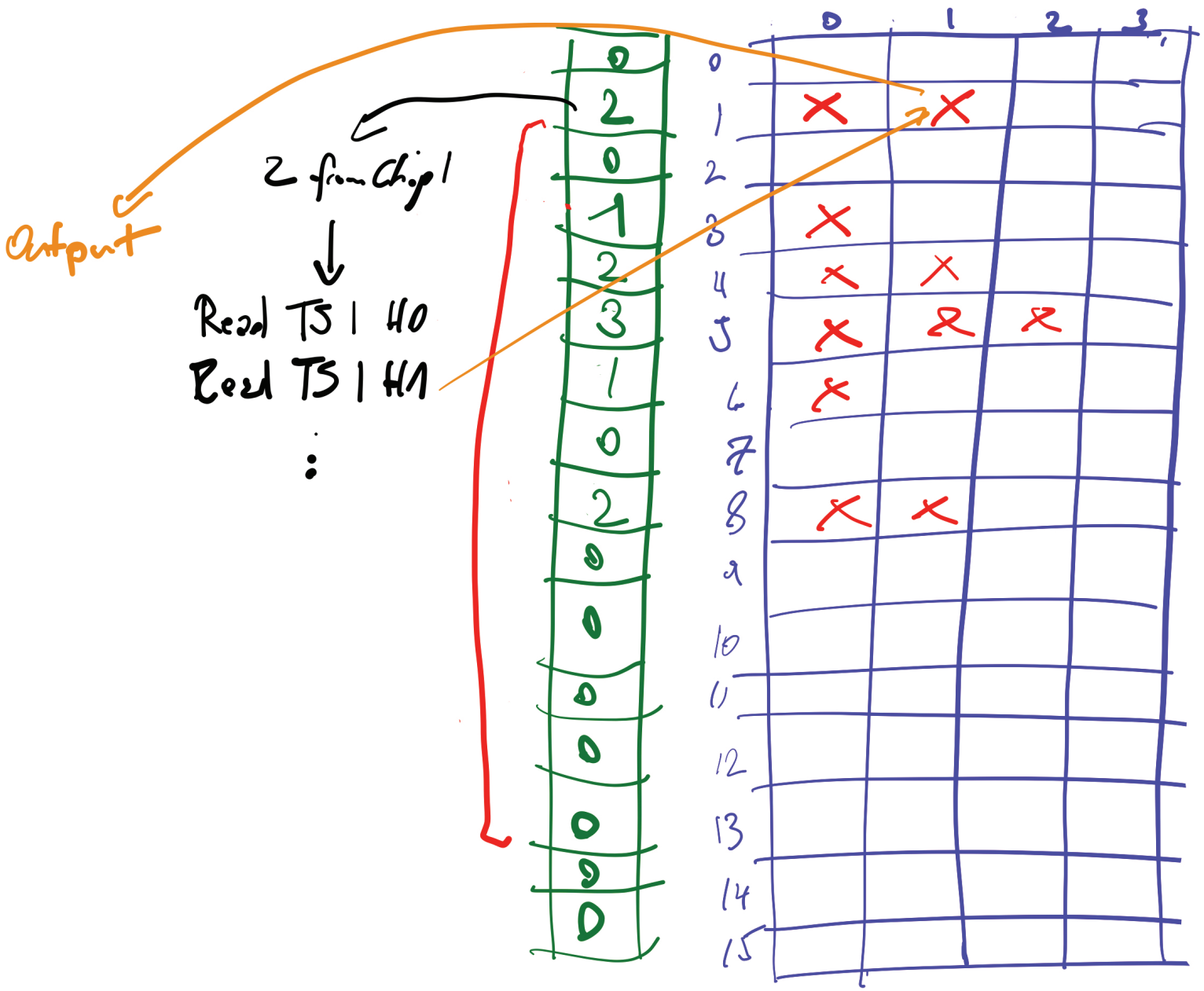

2 from Chip 1
0 1 2 3


2 from Chip 1
Read TS | H0
Read TS | H1
0 1 2 3

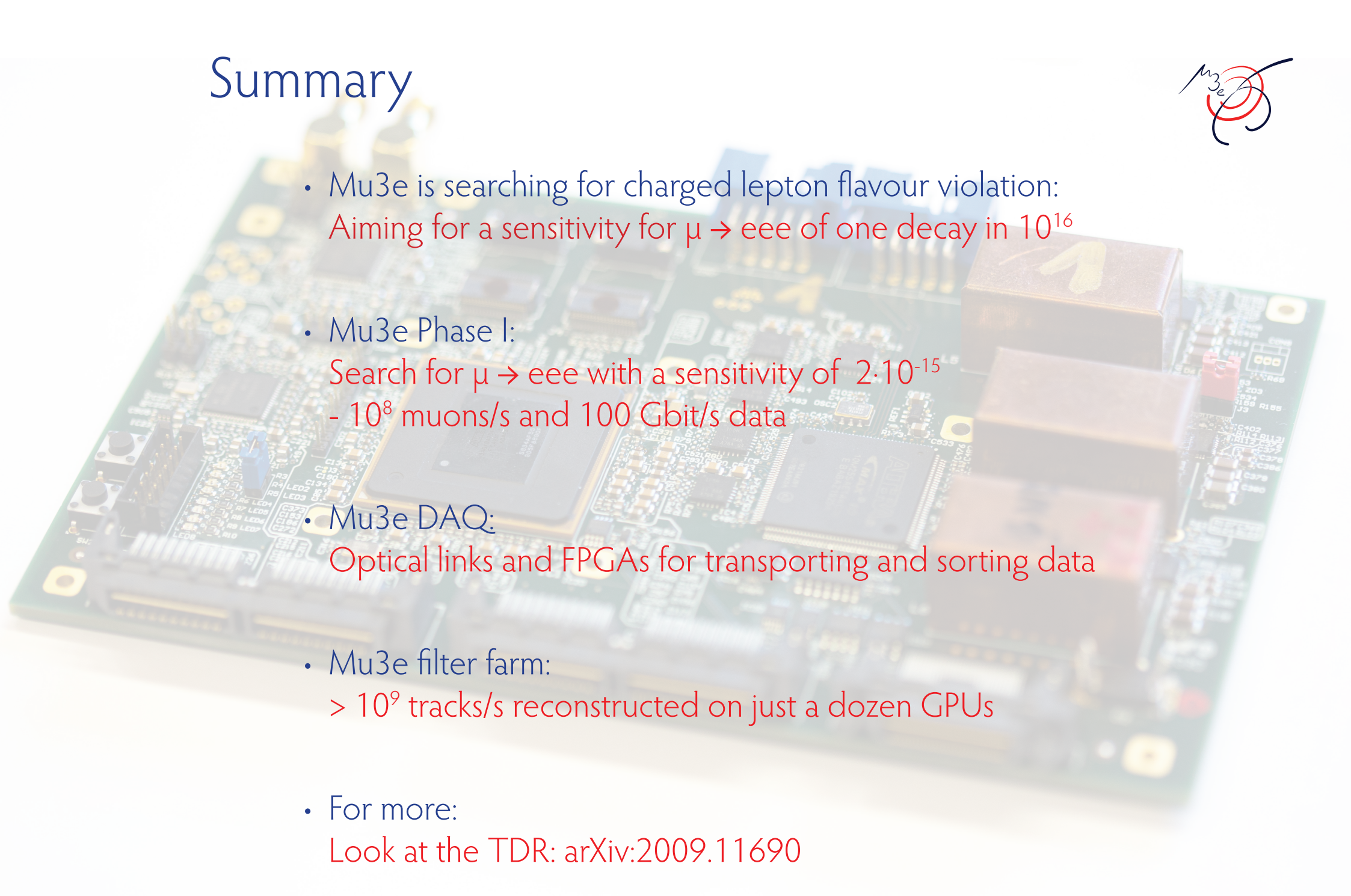
Output

- Output is a sequence of hits with a header for every timestamp overflow and a sub-header ever 16 timestamps
- Logic usage is very moderate (< 10 K logic elements including a lot of diagnostics)
- Runs at 125 MHz with some slack (the credit system is most tricky in terms of timing closure)


Output
2 from Chip 1
Read TS 1 H0
Read TS 1 H1
0 1 2 3


output
2 from Chip 1
Read TS 1 H0
Read TS 1 H1
0 1 2 3

Summary



- Mu3e is searching for charged lepton flavour violation:
  Aiming for a sensitivity for μ → eee of one decay in 10^{16}

- Mu3e Phase I:
  Search for μ → eee with a sensitivity of $2 \cdot 10^{-15}$
  - 10^{8} muons/s and 100 Gbit/s data

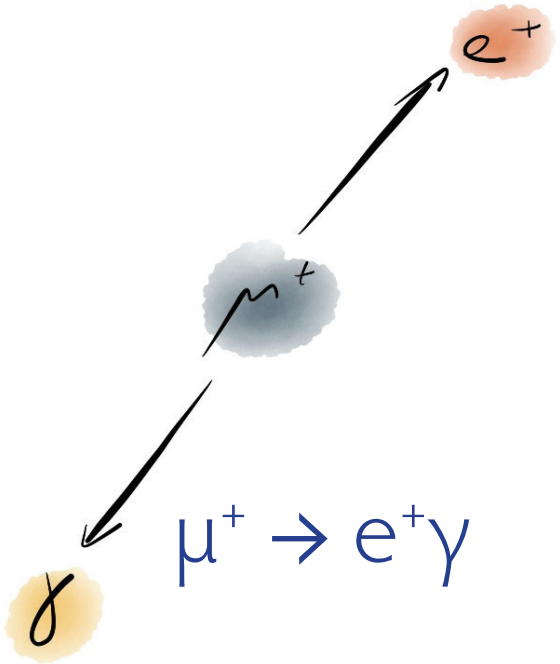
- Mu3e DAQ:
  Optical links and FPGAs for transporting and sorting data

- Mu3e filter farm:
  > 10^{9} tracks/s reconstructed on just a dozen GPUs

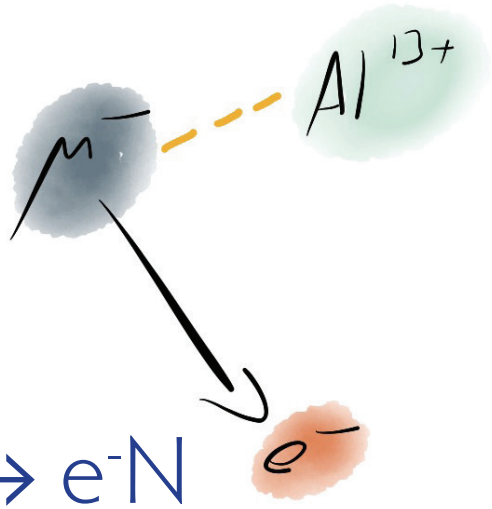
- For more:
  Look at the TDR: arXiv:2009.11690

Backup

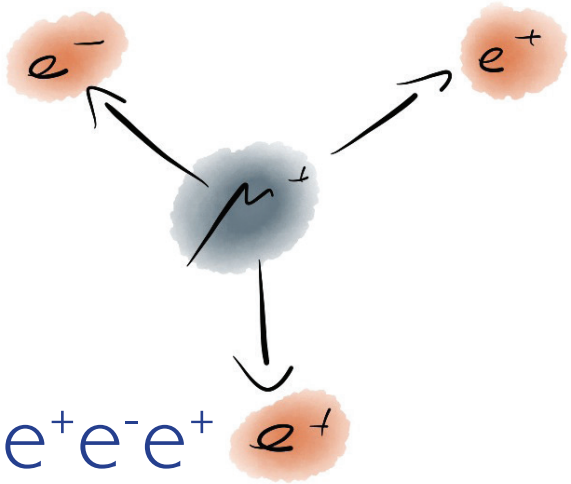
LFV Muon Decays



$\mu^+ \rightarrow e^+\gamma$

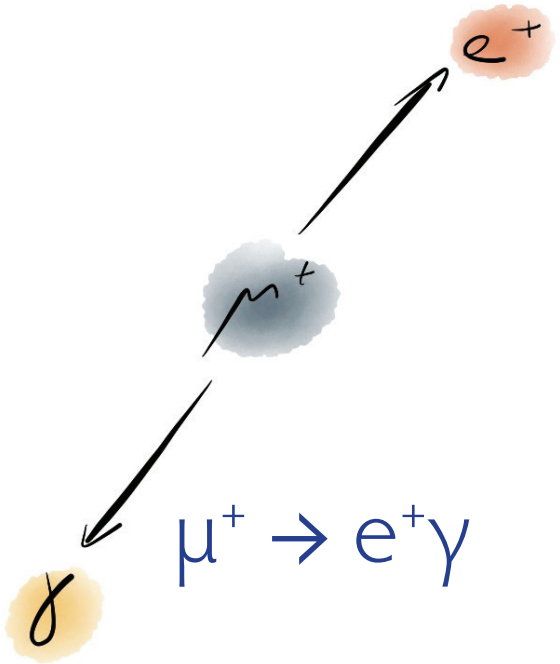


$\mu^-N \rightarrow e^-N$



$\mu^+ \rightarrow e^+e^-e^+$

LFV Muon Decays: Experimental Situation



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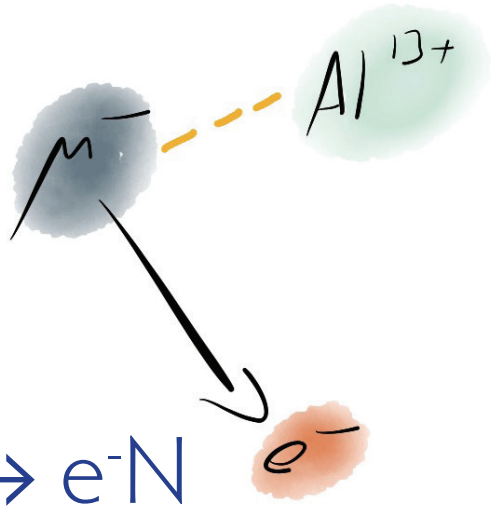

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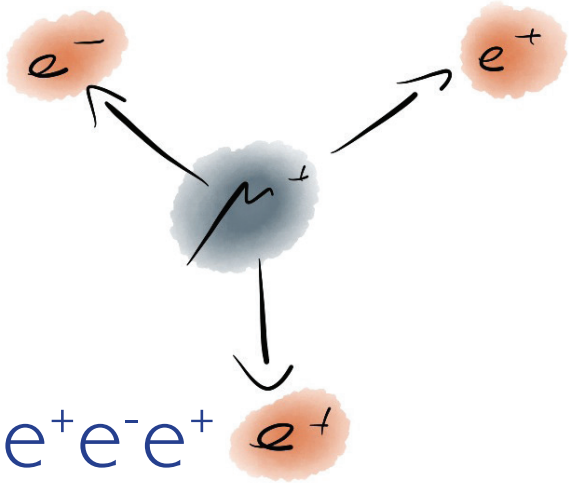


$\mu^+ \rightarrow e^+e^-e^+$

MEG (PSI)

$B(\mu^+ \rightarrow e^+\gamma) < 4.2 \cdot 10^{-13}$

(2016)

SINDRUM II (PSI)

$B(\mu^- Au \rightarrow e^- Au) < 7 \cdot 10^{-13}$

(2006)

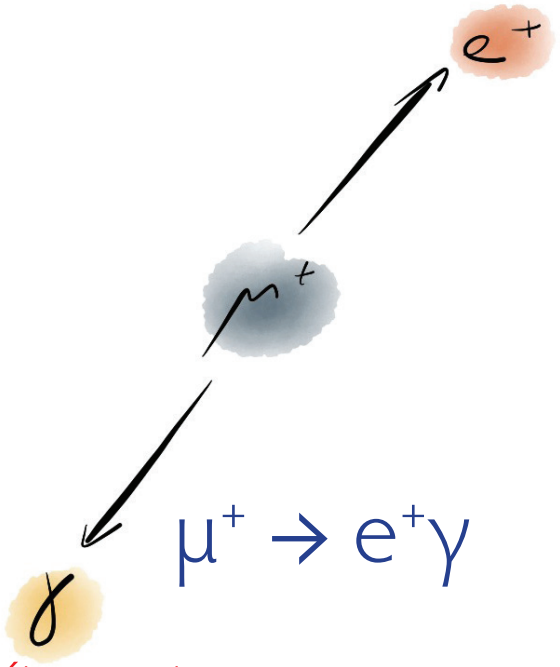
relative to nuclear capture

SINDRUM (PSI)

$B(\mu^+ \rightarrow e^+e^-e^+) < 1.0 \cdot 10^{-12}$

(1988)

LFV Muon Decays: Experimental signatures



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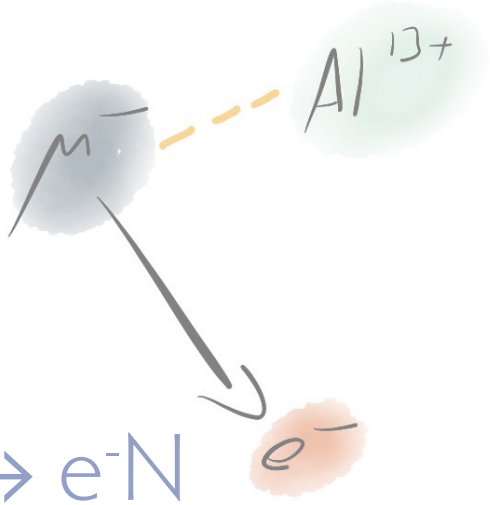
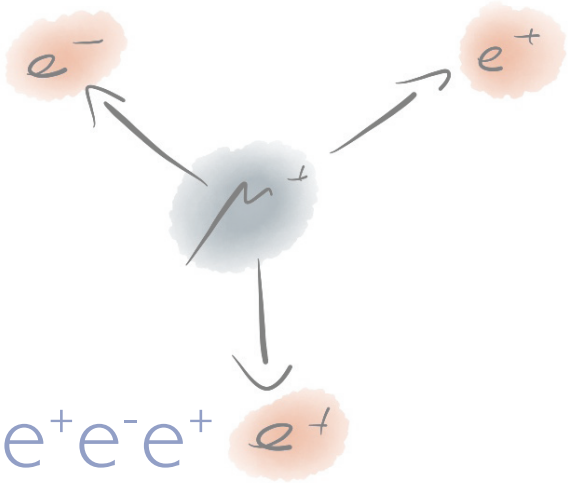


$\mu^-N \rightarrow e^-N$

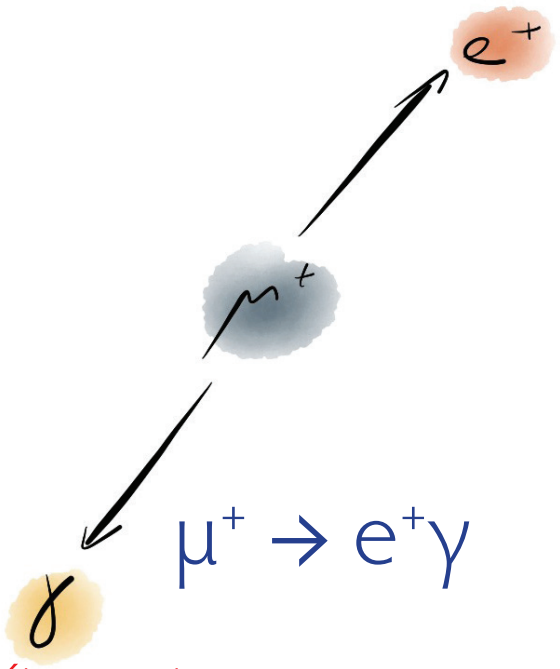


$\mu^+ \rightarrow e^+e^-e^+$

Kinematics

- 2-body decay
- Monoenergetic e^+, γ
- Back-to-back

LFV Muon Decays: Experimental signatures



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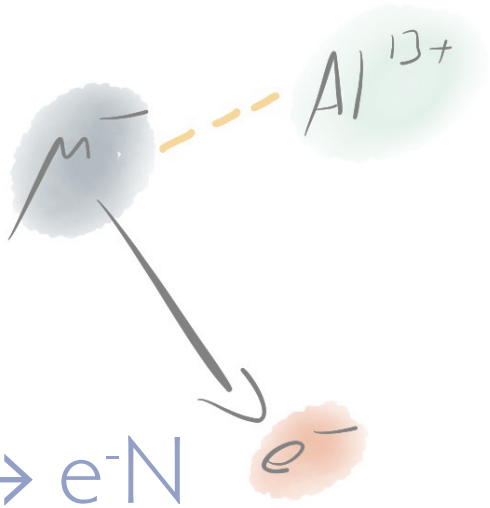

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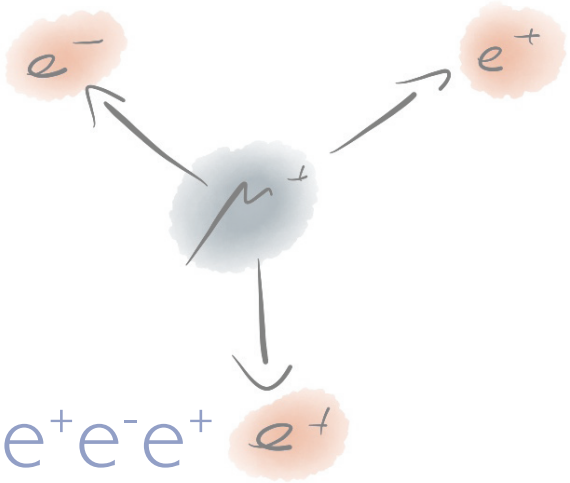


$\mu^+ \rightarrow e^+e^-e^+$

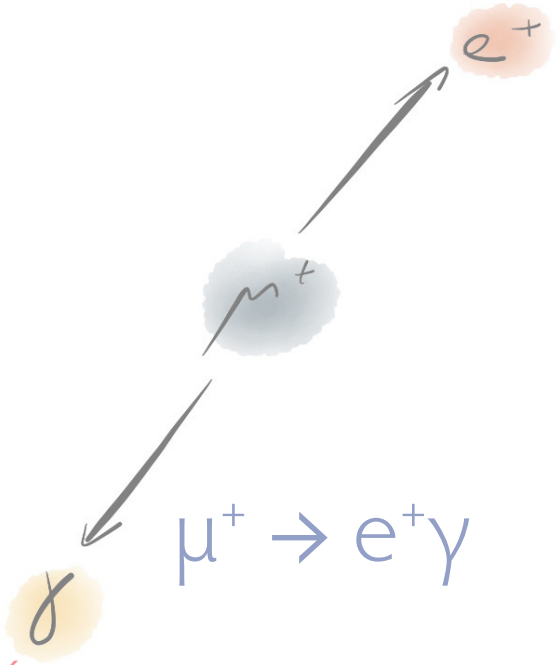
Kinematics

- 2-body decay
- Monoenergetic e^+, γ
- Back-to-back

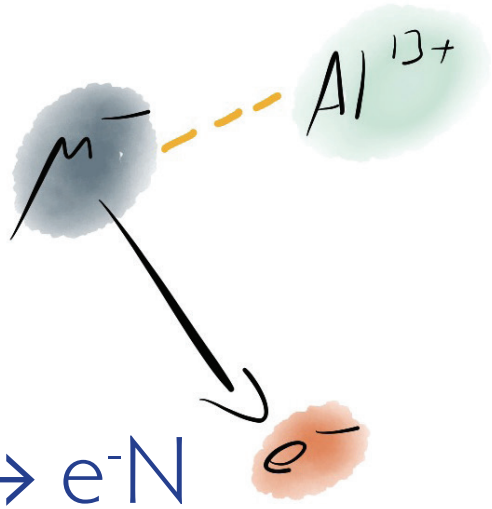
Background

- Accidental background
- Radiative decay

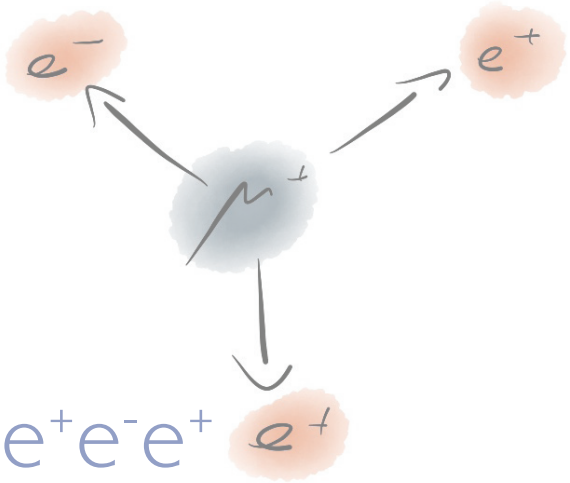
LFV Muon Decays: Experimental signatures



$\mu^+ \rightarrow e^+\gamma$



$\mu^-N \rightarrow e^-N$



$\mu^+ \rightarrow e^+e^-e^+$

Kinematics

- 2-body decay
- Monoenergetic e^+, γ
- Back-to-back

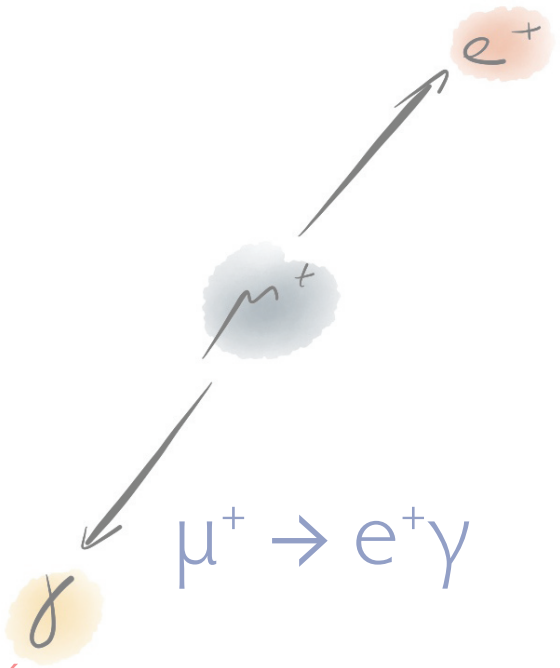
Background

- Accidental background
- Radiative decay

Kinematics

- Quasi 2-body decay
- Monoenergetic e^-
- Single particle detected

LFV Muon Decays: Experimental signatures



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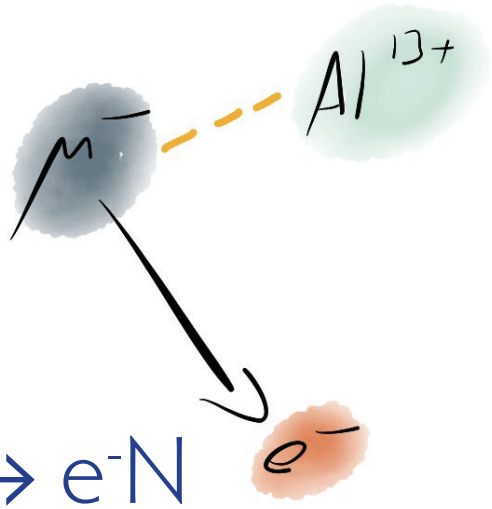

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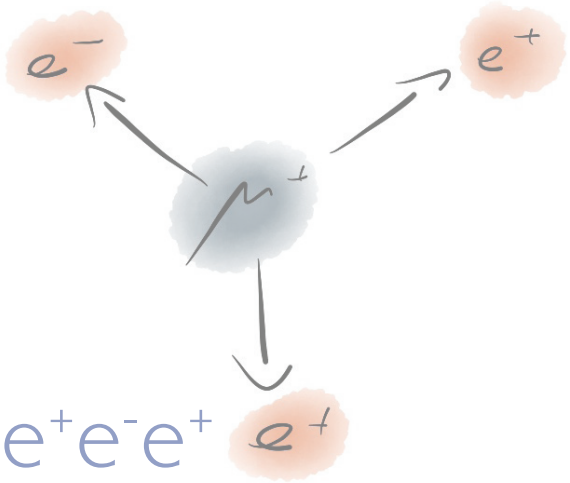


$\mu^+ \rightarrow e^+e^-e^+$

Kinematics

- 2-body decay
- Monoenergetic e^+, γ
- Back-to-back

Background

- Accidental background
- Radiative decay

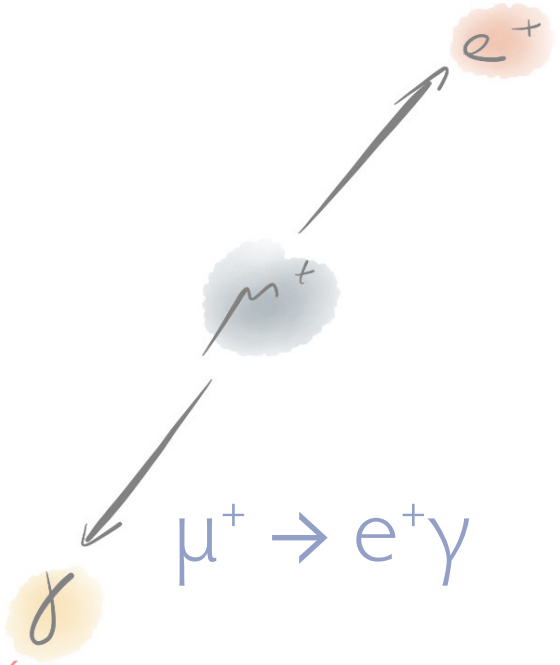
Kinematics

- Quasi 2-body decay
- Monoenergetic e^-
- Single particle detected

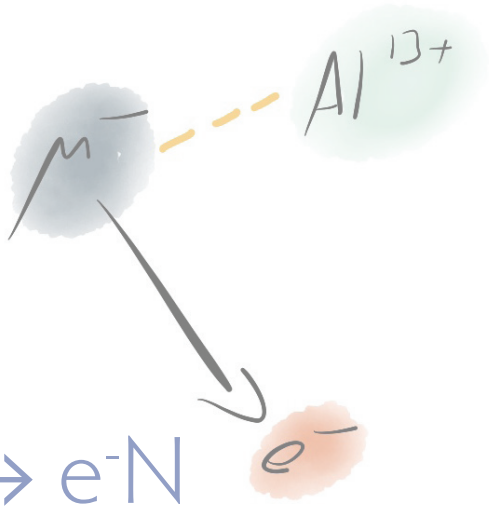
Background

- Decay in orbit
- Antiprotons, pions, cosmics

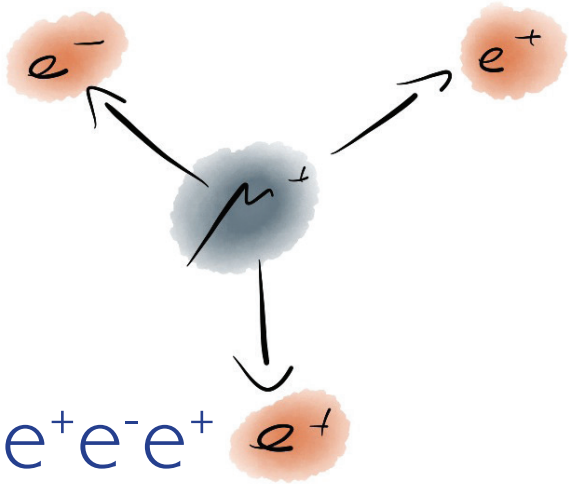
LFV Muon Decays: Experimental signatures



$\mu^+ \rightarrow e^+\gamma$



$\mu^-N \rightarrow e^-N$



$\mu^+ \rightarrow e^+e^-e^+$

Kinematics

- 2-body decay
- Monoenergetic e^+, γ
- Back-to-back

Background

- Accidental background
- Radiative decay

Kinematics

- Quasi 2-body decay
- Monoenergetic e^-
- Single particle detected

Background

- Decay in orbit
- Antiprotons, pions, cosmics

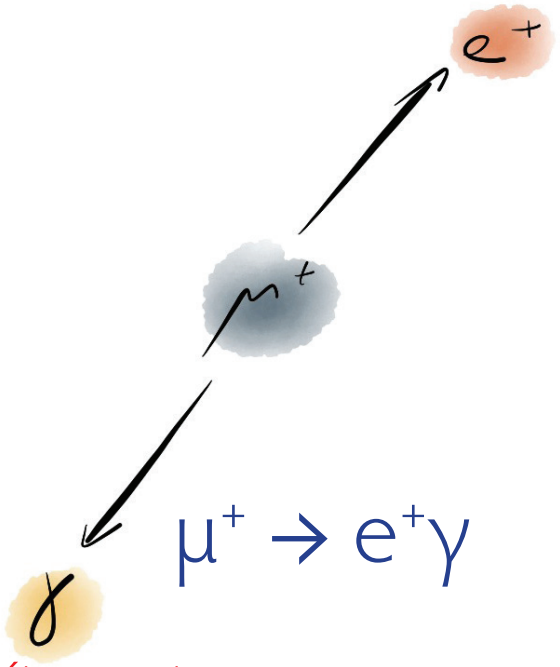
Kinematics

- 3-body decay
- Invariant mass constraint
- $\Sigma\, p_i = 0$

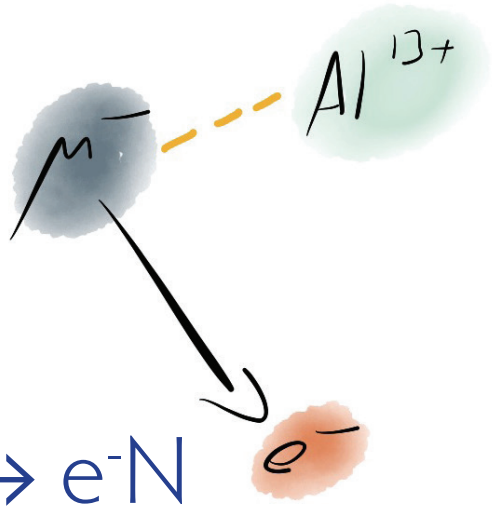
Background

- Internal conversion decay
- Accidental background

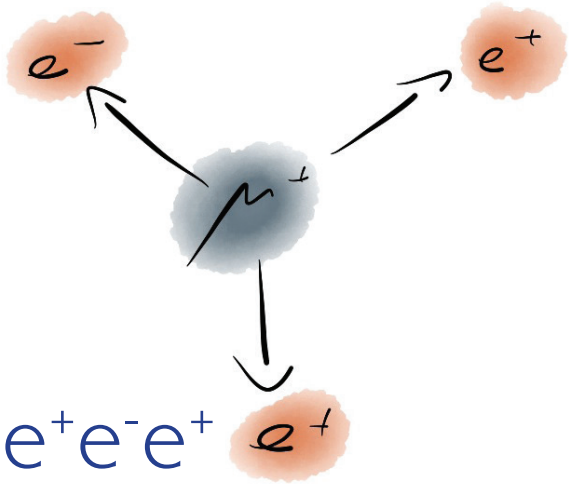
LFV Muon Decays: Experimental signatures



$\mu^+ \rightarrow e^+\gamma$



$\mu^-N \rightarrow e^-N$



$\mu^+ \rightarrow e^+e^-e^+$

Kinematics

- 2-body decay
- Monoenergetic e^+, γ
- Back-to-back

Background

- Accidental background
- Radiative decay

Kinematics

- Quasi 2-body decay
- Monoenergetic e^-
- Single particle detected

Background

- Decay in orbit
- Antiprotons, pions, cosmics

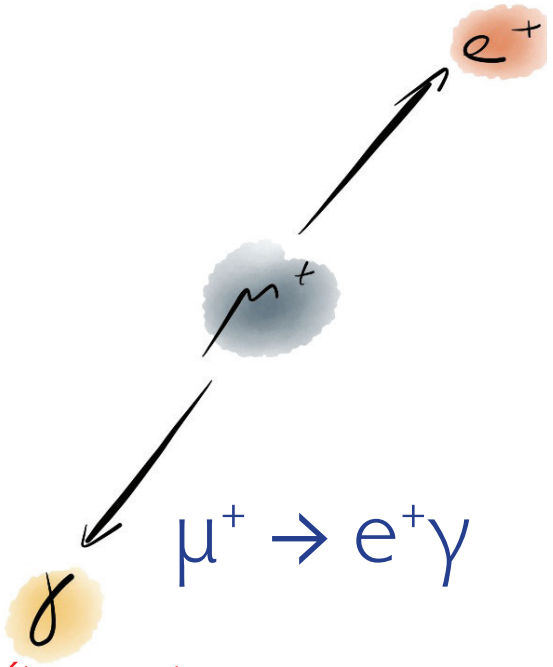
Kinematics

- 3-body decay
- Invariant mass constraint
- $\Sigma p_i = 0$

Background

- Internal conversion decay
- Accidental background

LFV Muon Decays: Experimental signatures



$\mu^+ \rightarrow e^+\gamma$

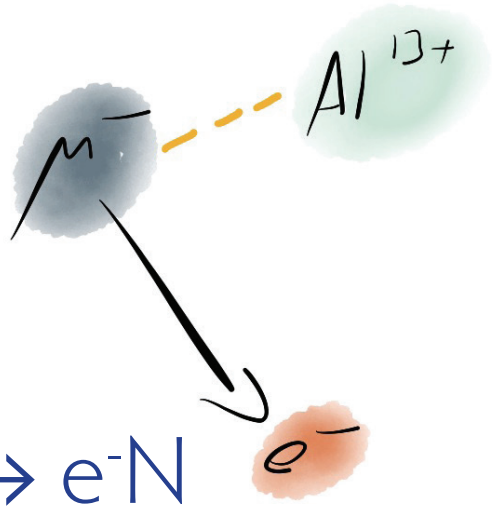
Kinematics

- 2-body decay
- Monoenerge
- Back-to-b

Backgro

- A al background

Continuous Beam



$\mu^-N \rightarrow e^-N$

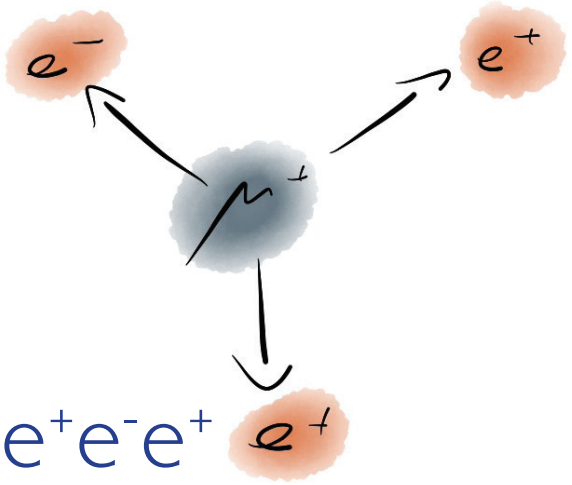
Kinematics

- Quasi 2-body d
- Monoenerge
- Single p etected

Backgro

- D orbit
- A protons, pions

Pulsed Beam



$\mu^+ \rightarrow e^+e^-e^+$

Kinematics

- 3-body decay
- Invariant mas aint
- $\Sigma p_i = 0$

Backgro

- R decay
- Ac dental background

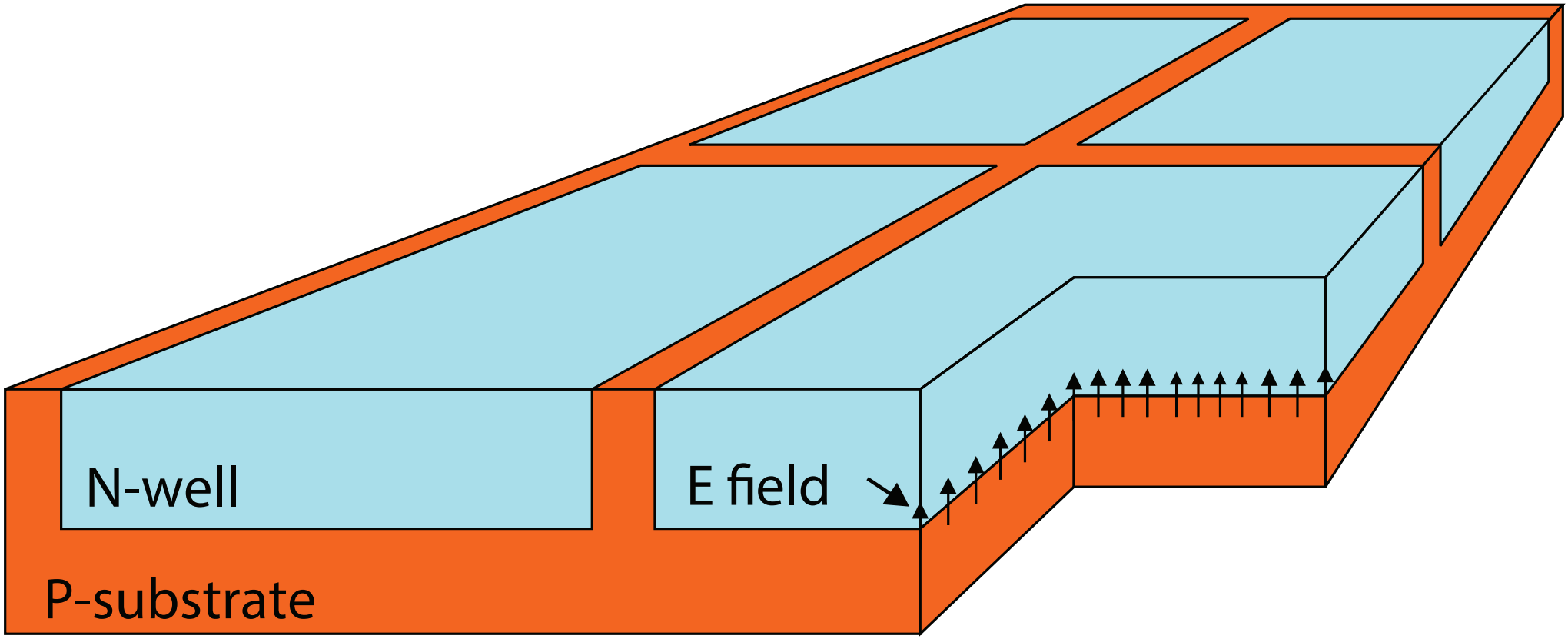
Continuous Beam

Very thin and fast silicon pixel sensors: HV-MAPS

Fast and thin sensors: HV-MAPS

High voltage monolithic active pixel sensors - Ivan Perić

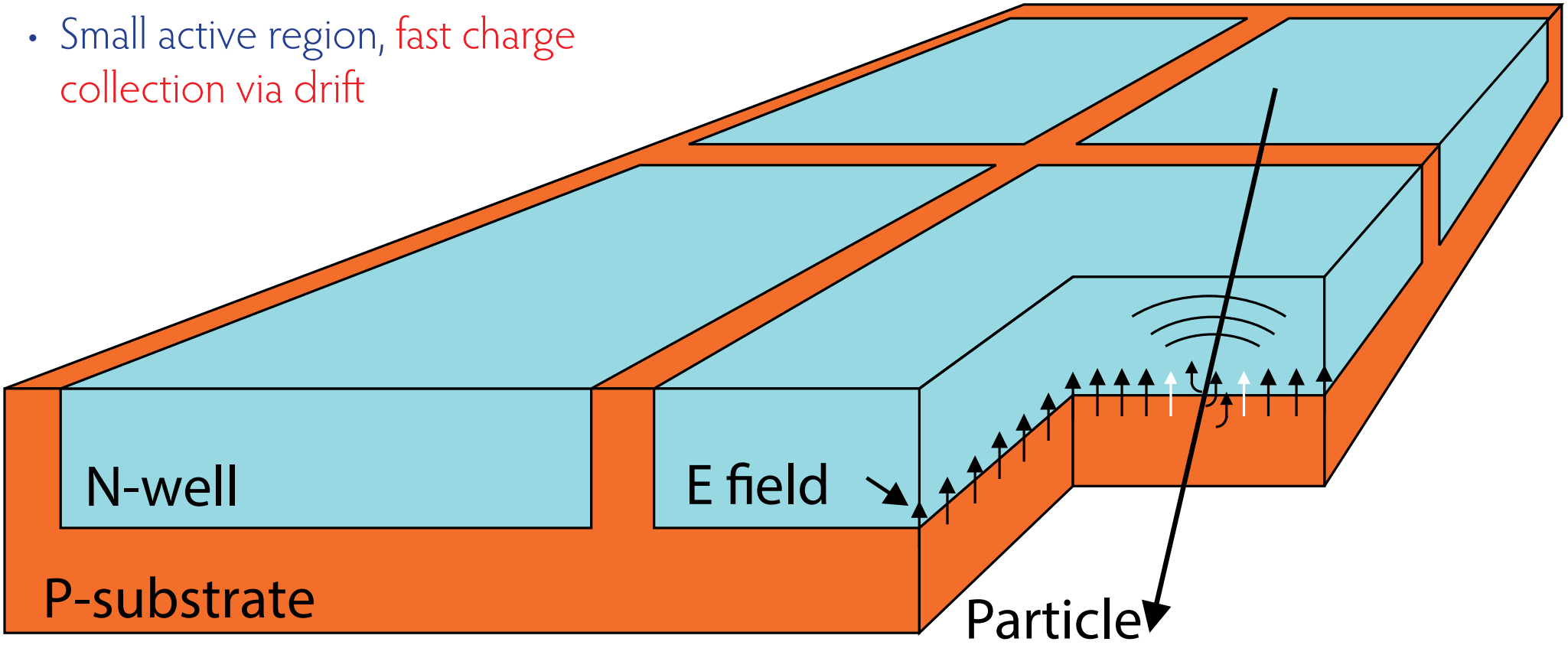
- Use a high voltage commercial process (automotive industry)



Fast and thin sensors: HV-MAPS

High voltage monolithic active pixel sensors - Ivan Perić

- Use a high voltage commercial process (automotive industry)
- Small active region, fast charge collection via drift



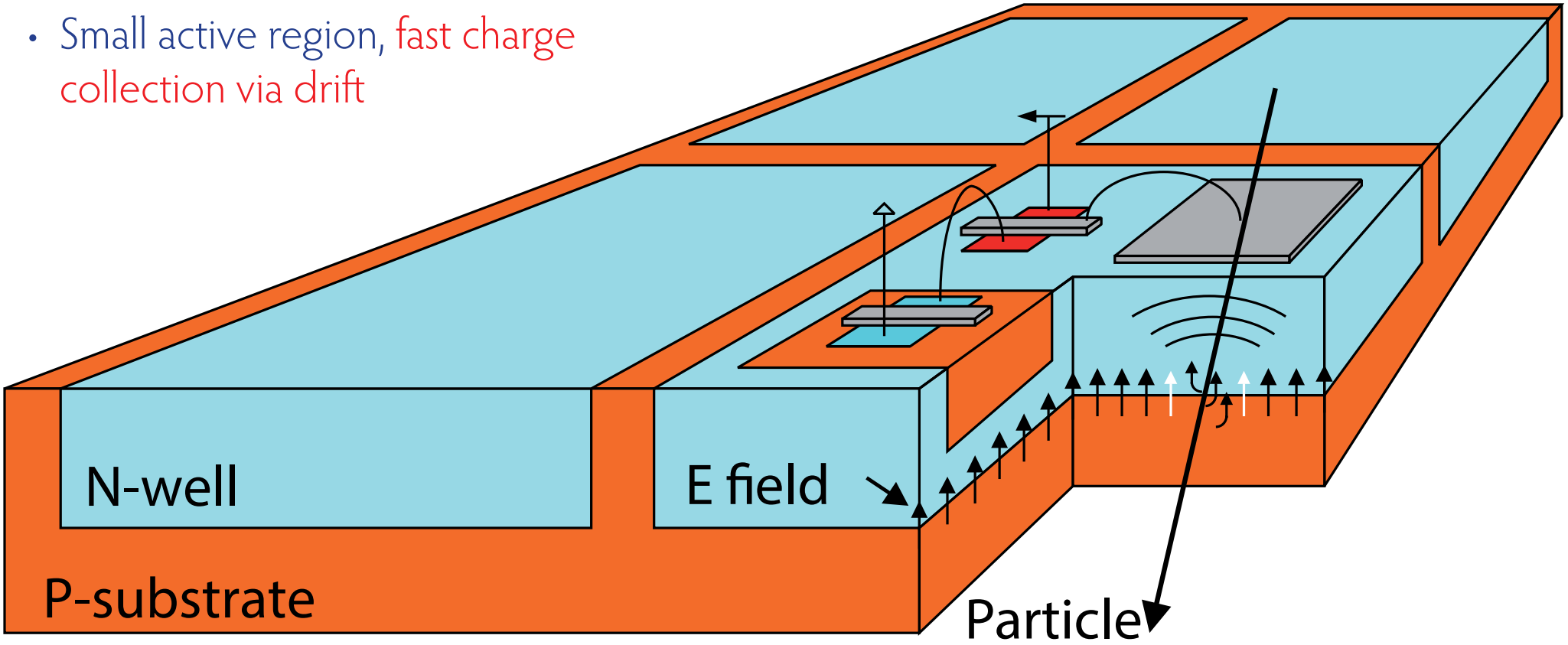
Fast and thin sensors: HV-MAPS

High voltage monolithic active pixel sensors - Ivan Perić

- Use a high voltage commercial process (automotive industry)
- Small active region, fast charge collection via drift

- Implement logic directly in N-well in the pixel - smart diode array
- Can be thinned down to < 50 µm

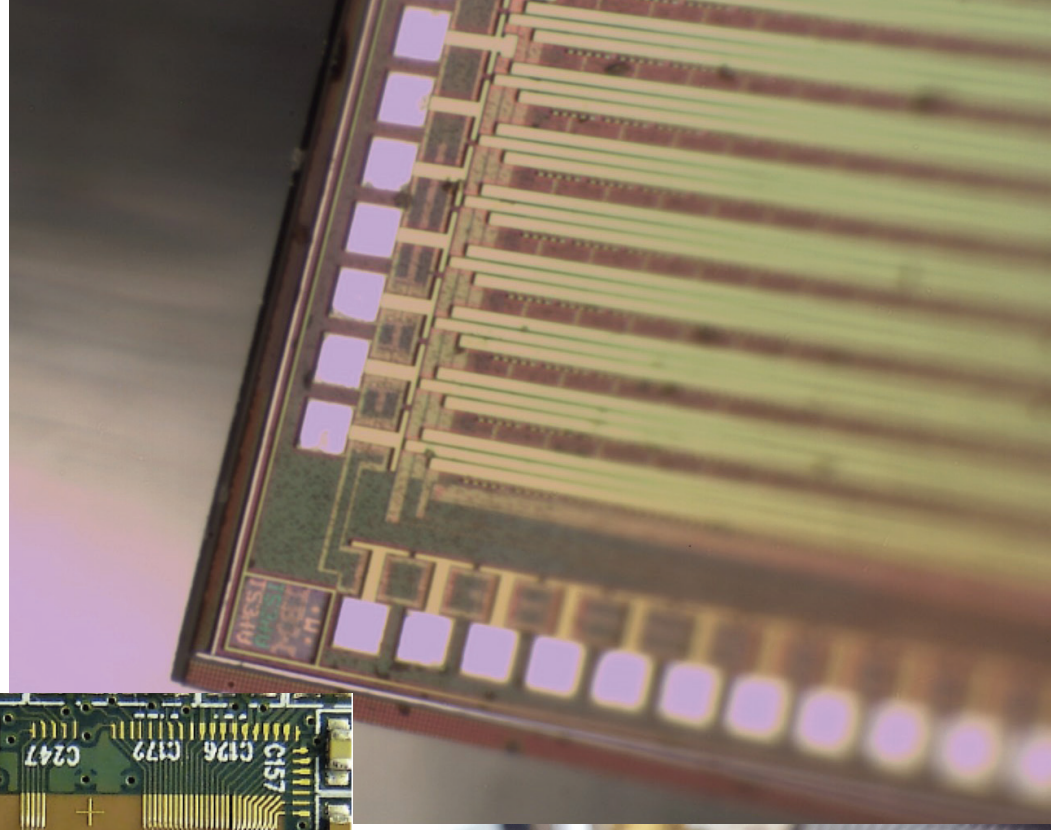
(I.Perić, NIM A 582 (2007) 876)

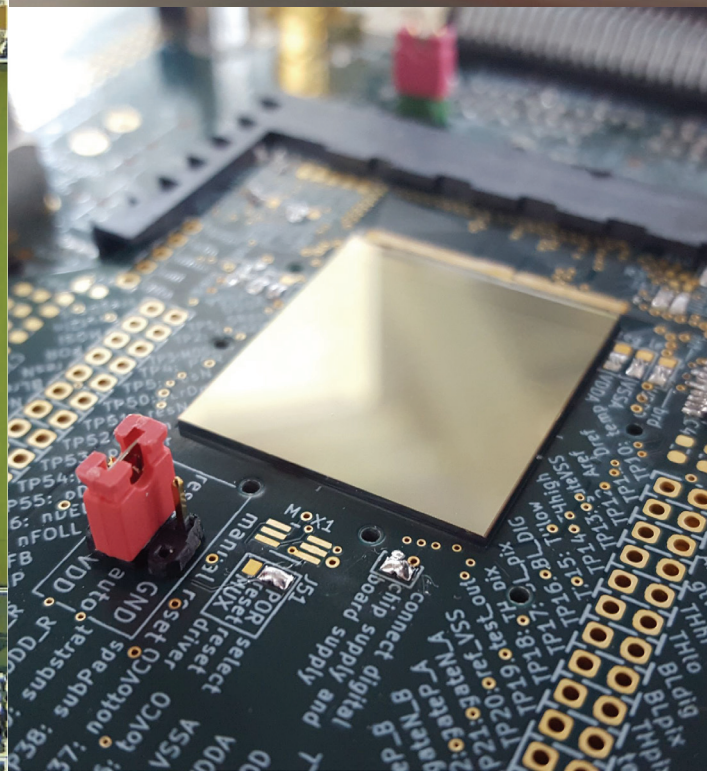


The MuPix Prototypes

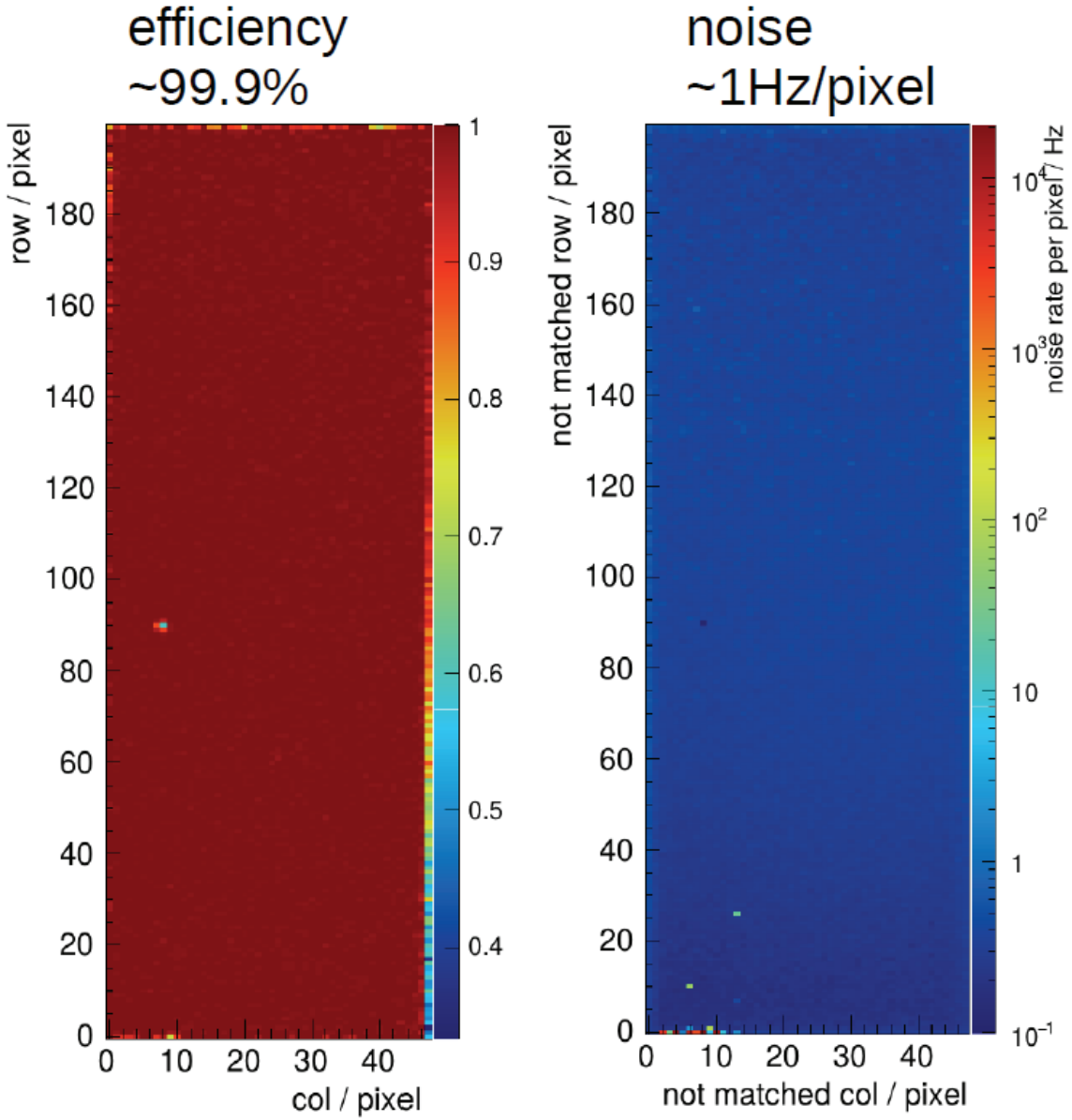
Developed a series of HV-MAPS prototypes

- Goal: Detection and signal processing with just 50 µm silicon
- 6th chip, MuPix7, was the first full system-on-a-chip
- Going "big" 2 x 1 cm^2 MuPix8 with 80 by 80 µm pixels also working nicely - some growing pains fixed
- Now: MuPix10, 2 x 2 cm^2, integration ready - under test

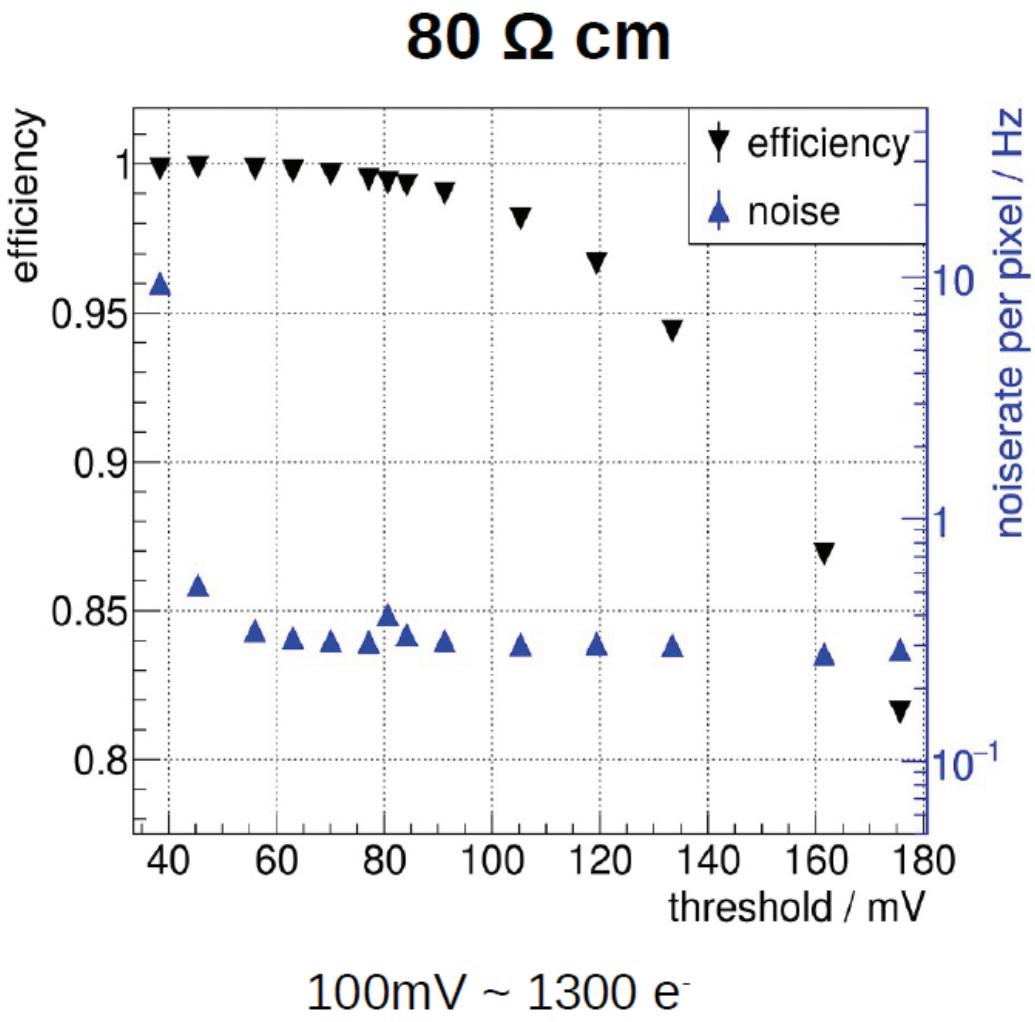




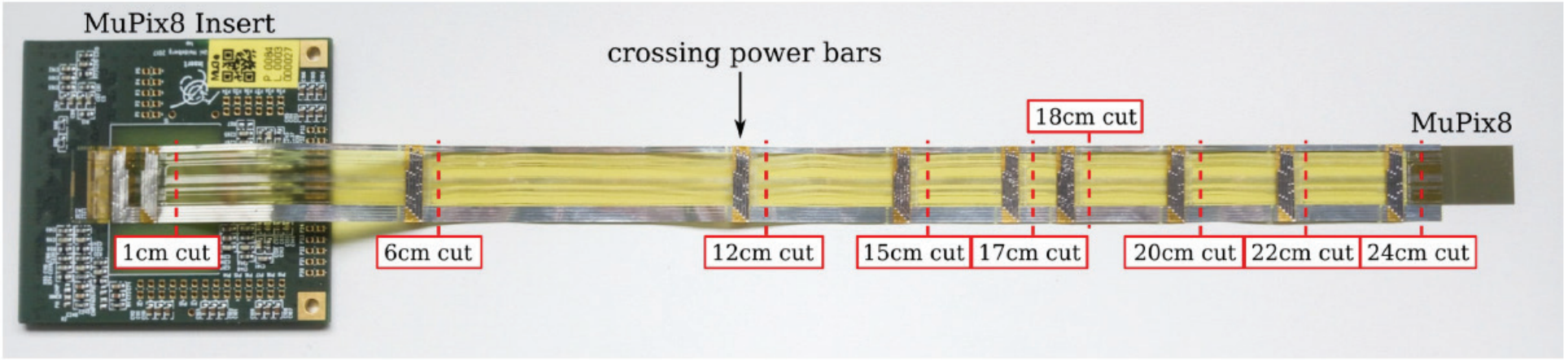
MuPix8: Results

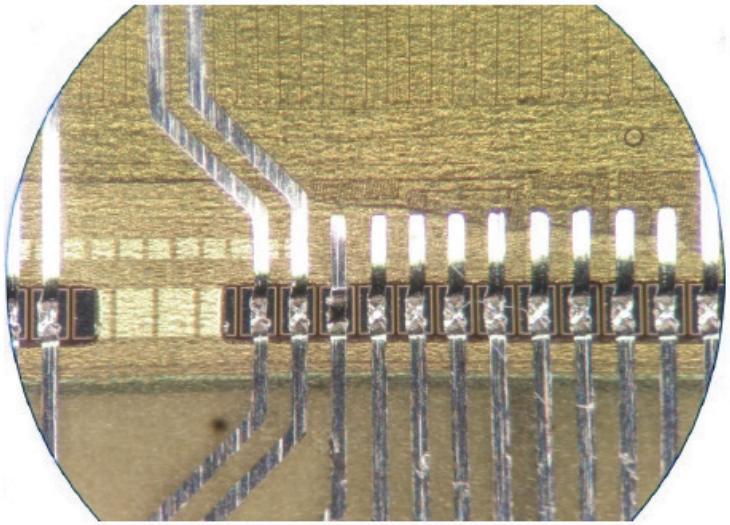


Time resolution of < 6 ns σ reached



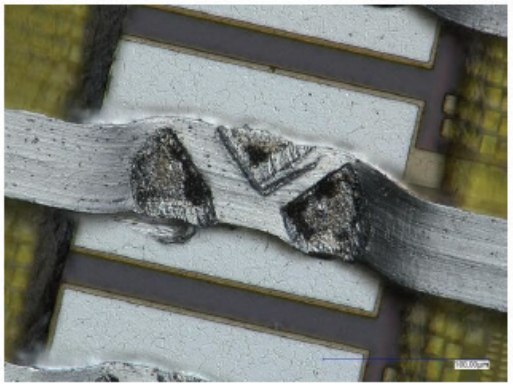
Integration with Flexprint





Operate MuPix on an aluminium-kapton flexprint without decoupling capacitors

- Low noise
- No transmission errors
- Longer than needed for Mu3e

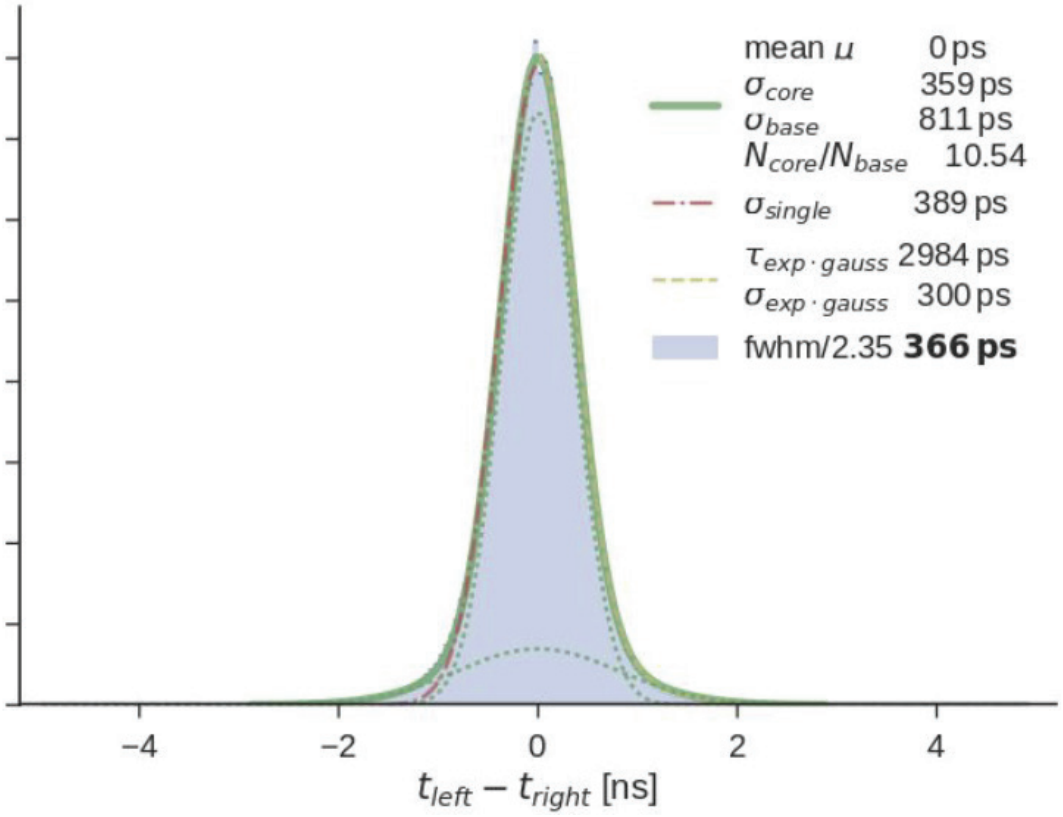


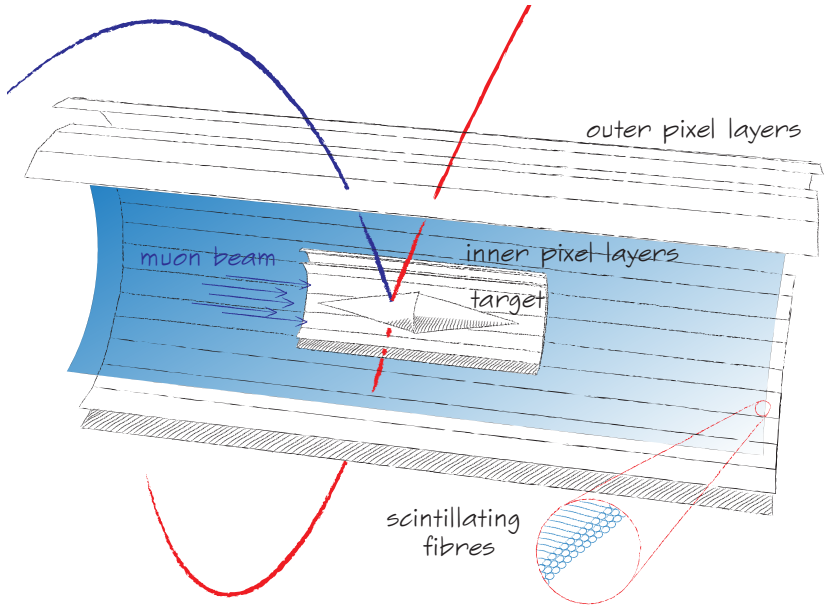
Better timing:
Scintillating fibres and tiles

Timing Detector: Scintillating Fibres

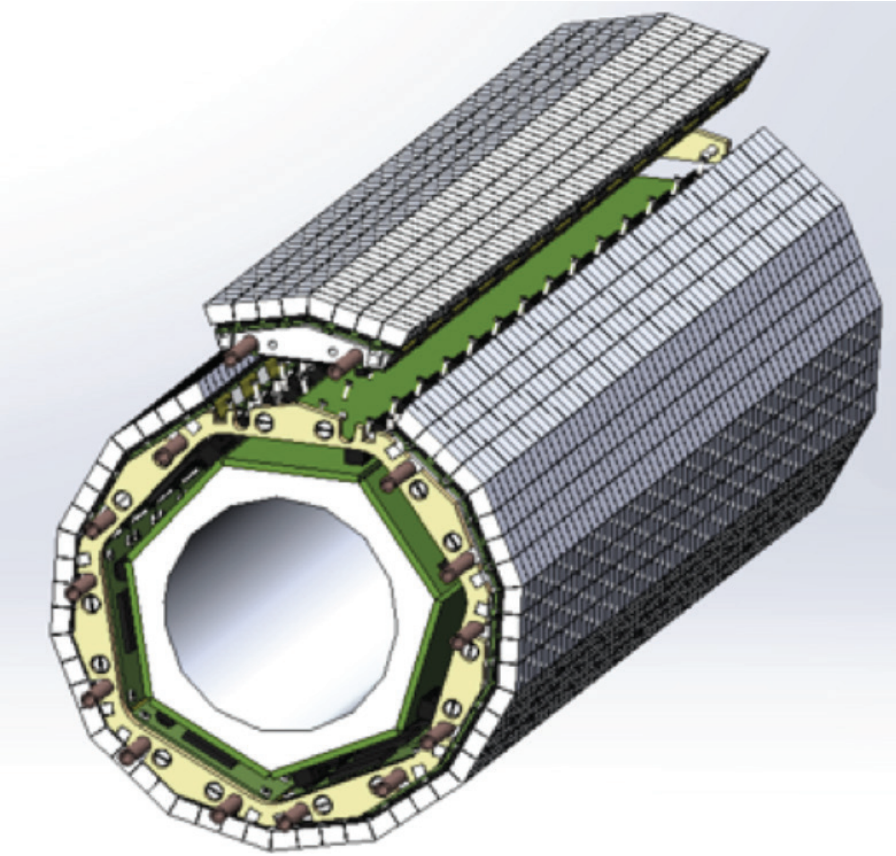
- 3 layers of 250 µm scintillating fibres
- Read-out by silicon photomultipliers (SiPMs) and custom ASIC (MuTRiG)

Timing resolution < 400 ps including ASIC

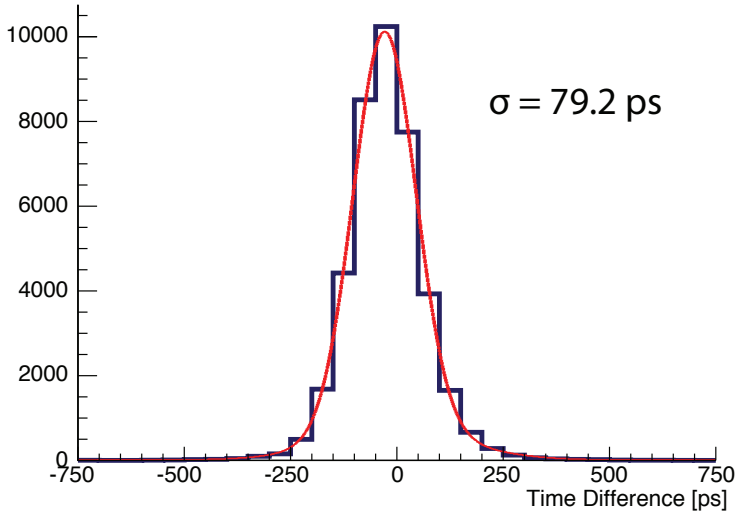


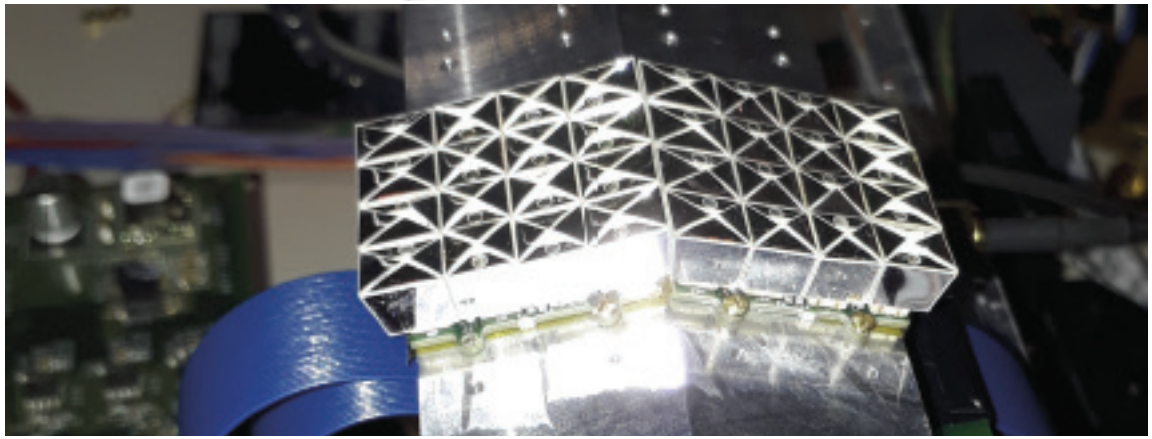


Timing Detector: Scintillating tiles



- ~ 0.5 cm^3 scintillating tiles
- Read-out by silicon photomultipliers (SiPMs) and custom ASIC (MuTRiG)





- Test beam with tiles, SiPMs and readout ASIC
- Timing resolution better 80 ps