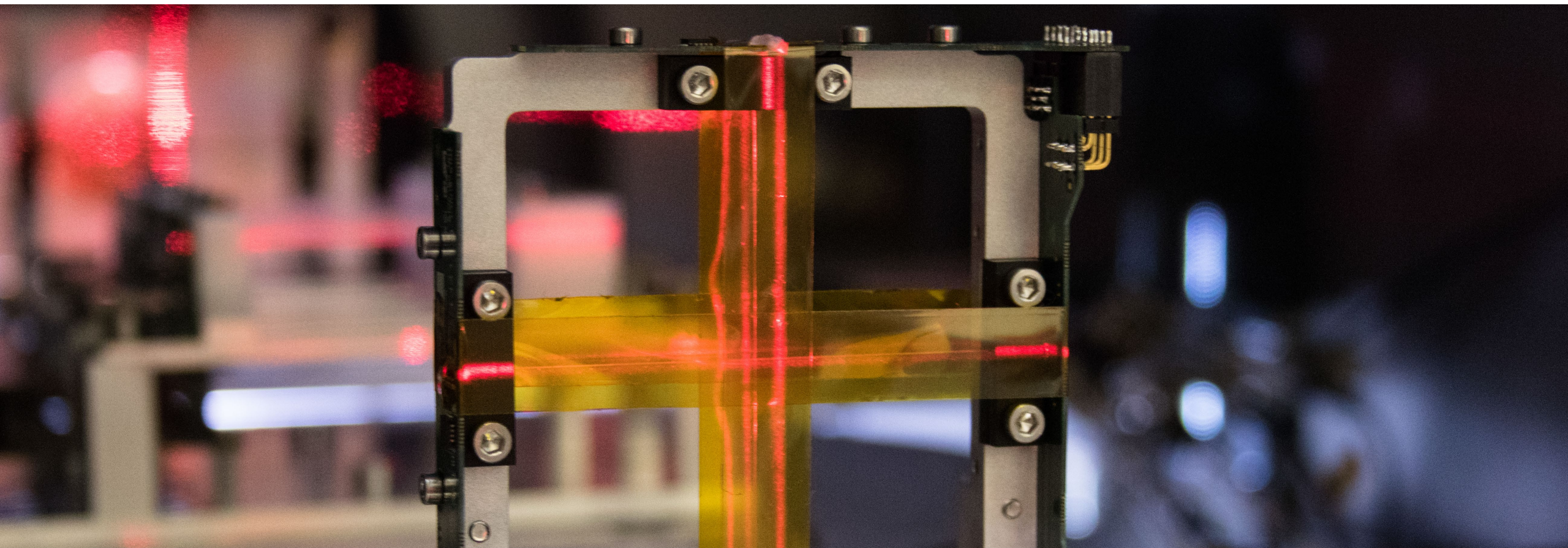


PCRM Scintillating Fiber Hodoscopes (SFHs): Update

Martin J. Losekamm | Technical University of Munich

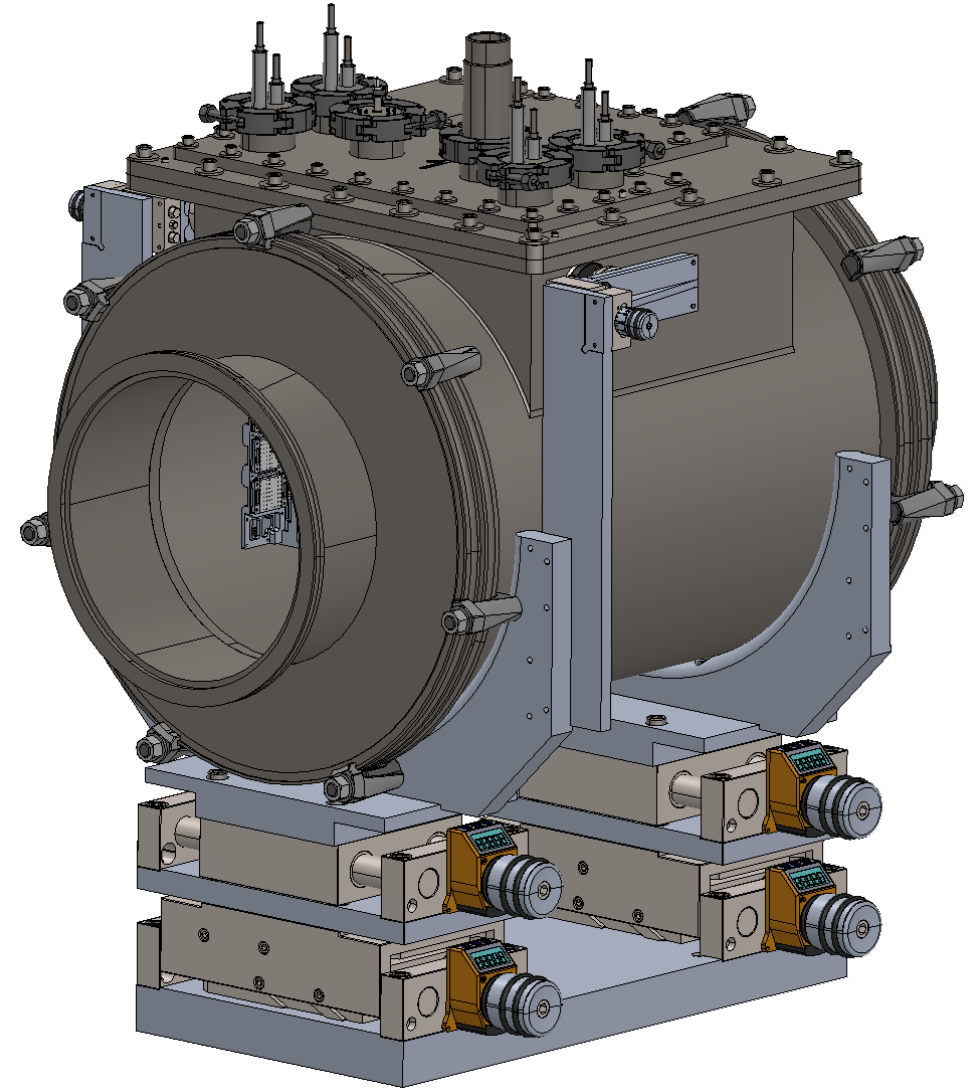
May 4, 2021



Funding

Tracking-Station Mechanics and SFHs

- We received full funding at TUM for the SFHs and the tracking-station mechanics
 - 60 k€ for vacuum vessel and feedthroughs for power, data, and cooling (for SFHs)
 - 30 k€ for alignment system
 - 18 k€ for SFH cooling system (can possibly be shared with SPDs/ALPIDEs)
- **We plan to have one tracking station ready for testing in 2021, including alignment system**
- Offers for mechanics (TUM workshop) and alignment system (MM Engineering GmbH) received
 - Budget and delivery times work out
- Coordination with Maxime, Stefano, Johannes, ... in the coming weeks to finalize design



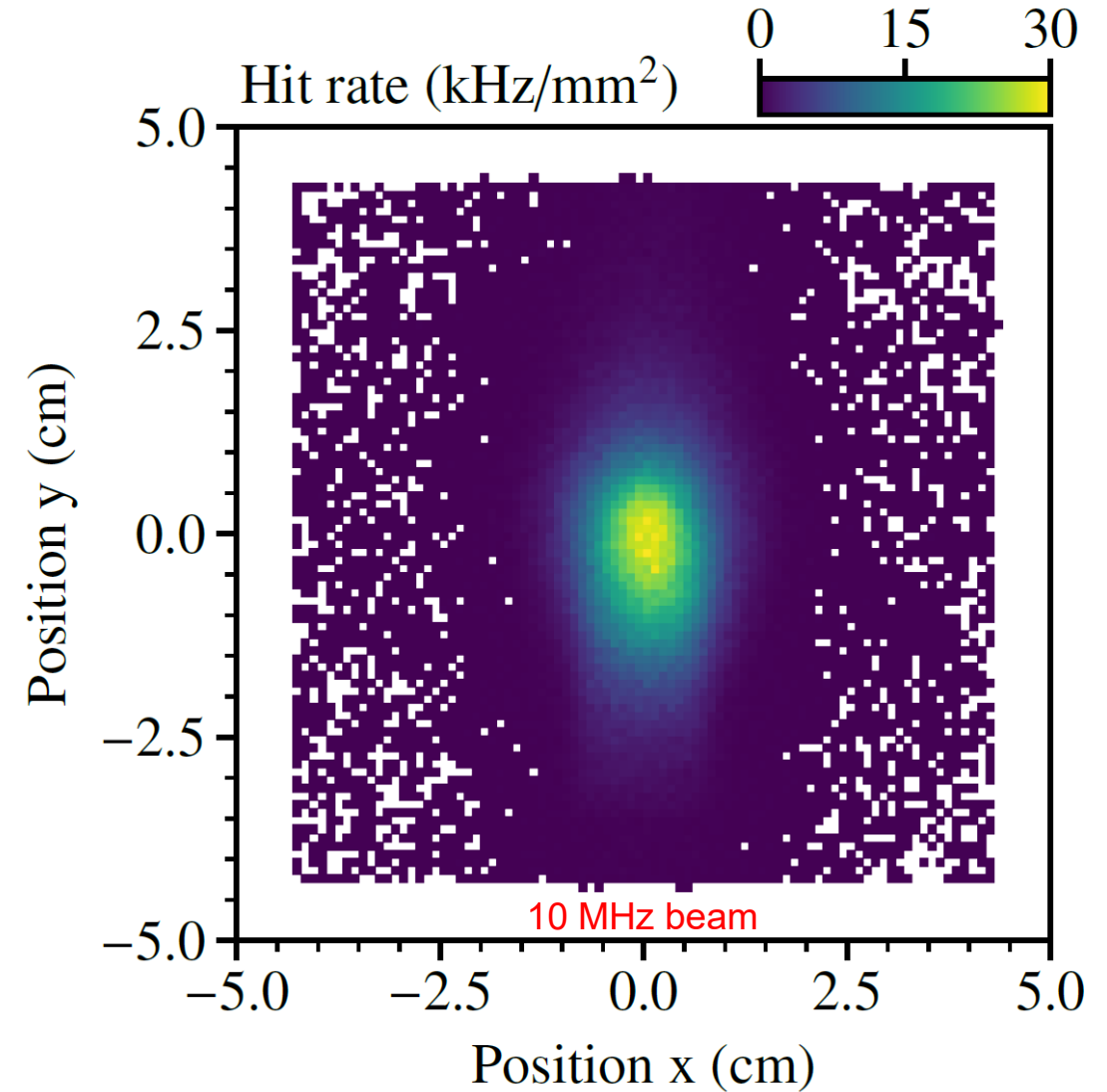
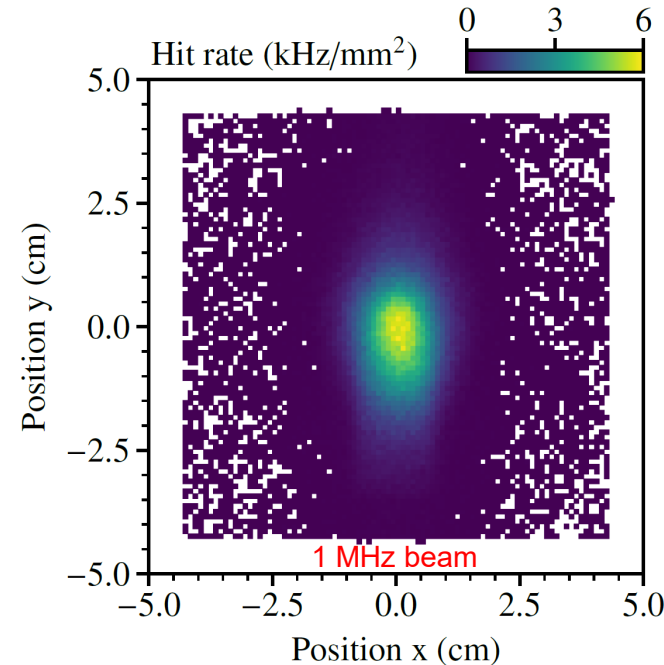
Expected Hit Rates

From Beam Profile

- Expected rates from rescaling beam profile at SFH/SPD position in target area
- 10 MHz integrated beam rate (design target)

➤ Hit rates of >100 kHz for central fibers

➤ Rates of >40 kHz even for 1-MHz beam rate



	CMAD #1	CMAD #2	Triroc	Petiroc	Citiroc
Sensitivity	< 1 pe ⁻	< 1 pe ⁻	< 1 pe ⁻	< 1 pe ⁻	1/3 pe ⁻
Dynamic range	< 3 pe ⁻ Attenuator required	< 3 pe ⁻ Attenuator required	~3000 pe ⁻	~3000 pe ⁻	~2500 pe ⁻
Max. hit rate	>5 MEvents/s per ch.	>5 MEvents/s per ch.	50 kEvents/s	40 kEvents/s (digital) >1 MEvents/s per ch. (analog)	20 MEvents/s per ch.
Power consumption	26 mW/ch	26 mW/ch	10 mW/ch	6 mW/ch	7 mW/ch
Gain / bias adjust.	no	no	yes	yes	yes
Channels per chip	8	8	64	32	32
PCB space for 192 channels (chips only)	>60 cm ²	>60 cm ²	<5 cm ²	<10 cm ²	<10 cm ²
Development effort	Array backplane CMAD carrier iFTDC firmware adaption Multiplexer / coincidence	Array backplane (incl. μ C) Firmware CMAD carrier Multiplexer / coincidence	Array backplane (incl. FPGA and μ C) Firmware Multiplexer / coincidence	Array backplane (incl. FPGA and μ C) Firmware Multiplexer / coincidence	Array backplane (incl. FPGA and μ C) Firmware Multiplexer / coincidence
Comments				Choice of digital (time, energy) or analog readout (e.g., for tests) Max. analog rate TBC	Energy readout required external ADC
Cost (ASIC)	0 €	0 €	484 € (net)	330 € (net)	330 € (net)

SFH Delivery and Lead Times

As of May 2021

- Kuraray committed to a delivery of fibers in July
- Delivery of SiPM arrays for prototype by the end of June
 - Remainder of order by end of October
- Test boards for front-end/DAQ tests with Citiroc and iFTDC should arrive within 2 weeks
- Production time for prototype tracking-stations mechanics: ~2 months
- Lead time for alignment system: ~2 weeks

