

## VMM3a related firmware activities in 2020 and 2021

ESS work on RD51 SRS components

DOROTHEA PFEIFFER (ESS) STEVEN ALCOCK (ESS) SERGEI ODINTSOV (UNIVERSITY OF TALIN)

15/02/2021





- 1. Tallinn University Inkind project: Cleanup, refactoring and documentation of VMM3a hybrid firmware
- 2. Integration of RD51 VMM3a hybrid into ESS readout
- 3. SRS FEC firmware and slow control changes



### Tallinn University: Refactoring firmware for RD51 VMM3a hybrid

15/02/2021

### Inkind project for NMX

Tallinn University: Refactoring firmware for RD51 VMM3a hybrid



- Project between the electronics department of Tallinn University and ESS NMX, signed just before Xmas in 2019
- Aim of the project was to clean up the hybrid firmware, refactor and document it
- Person chosen: Sergei Odintsov, Electronics Engineer, FPGA expert, at the moment finishing his PhD
- Original plan was, Sergei comes to CERN for a few weeks to get familiar with the SRS, and works together with Marek
- But then came Corona...
- We did not have a spare SRS system to send to Tallinn, therefore we set up a PC so that Sergei could have remote access to an SRS system via Teamviewer



- Xilinx Vivado (tool for series 7), the successor of the much hated ISE, was build using Planahead technology
- Planahead can be used instead of ISE for Virtex 6 and Spartan 6
- Repo does not store numerous ISE project files anymore, or even Planahead project, just tcl script (fun fact: Marek, Sergei and Steven came up in parallel with the same solution)
- TCL script is executed in Planahead and creates the project

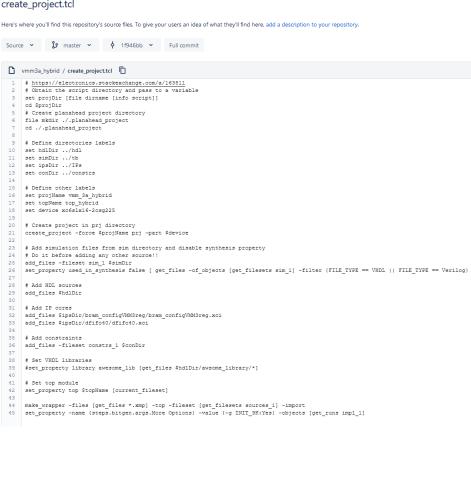
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### RD51 VMM3a hybrid firmware brightness

#### Change of repository logic

- create\_project.tcl script is very simple, describes which directories and files are added to the project
- Strategies for synthesis and implementation can be added, e.g. set\_property strategy TimingWithIOBPacking [get\_runs synth\_1]
- Since project is generated and not stored in repo, no more problems and errors due to temporary ISE project files (my computer was driving me insane, claiming insufficient rights all the time)
- Repo contains only vhdl, verilog files and xci files for IP cores
- Repo structure follows "quasi" standard: vhdl/Verilog files are in hdl, xci files for IP cores in IPs, ucf constraints files in constrs, and test benches in tb
- Sub folders used in hdl to create logical structure of the source code

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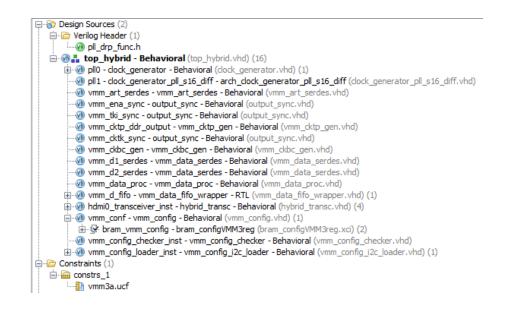
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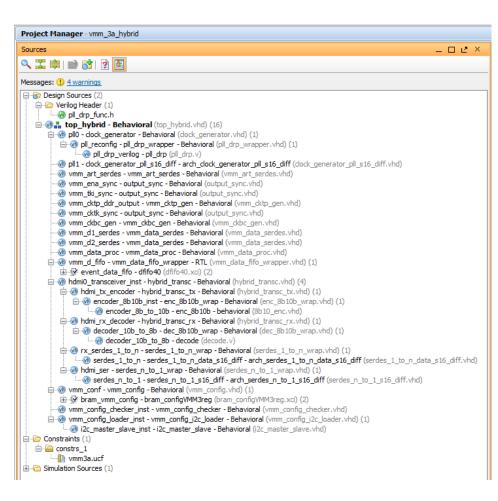


### RD51 VMM3a hybrid firmware brightness

#### Change of unit names and cleaning of code

- Unused modules removed
- Unused code in modules removed
- Units were renamed so that names are consistent
- Code structured in three major parts, PLLs, HDMI transceivers and VMM





### RD51 VMM3a hybrid firmware brightness Coding standard

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- Naming of signals according to following coding standard
  - Constants: capital letters starting with C ٠
  - Wires connected to output, i\_ or o\_ depending on direction ٠
  - Types: t\_ •
  - Internal wires: w ٠
  - Registers: f ٠
  - Outputs of combinatorial logic: k\_ ٠
- Components are changed to entities
- Use of generics and constants instead of numbers
- Reformatting of code
- Correction of sensitivity lists of processes, replacing clk'event by rising edge
- Explanatory comments added
- Structural changes to simplify code

#### 67 architecture Behavioral of hybrid transc is 68 -- C .\* = constant 69 constant C\_RST\_SYNC\_SHIFT\_REG\_LEN : natural := 2: 70 : natural := 3; constant C VMM DATA FIFO CLEAR TTC POS 71 constant C\_VMM\_BCR\_TTC\_POS : natural := 4; 72 constant C\_VMM\_CKTP\_GENERATOR\_EN\_TTC\_POS : natural := 0; 73 -- o .\* i = wire connected to output 74 signal o hdmi tx i : std logic vector (G\_VMM\_NUM - 1 downto 0); 75 signal o\_hdmi\_rx\_config\_data\_i : std logic vector (work.hybrid transc rx pkg.C DATA WORD LEN - 1 downto 0); 76 signal o hdmi rx config addr i : std logic vector (work.hybrid transc rx pkg.C DATA WORD LEN - 1 downto 0); 77 signal o hdmi rx config data valid i : std logic; 78 signal o\_vmm\_data\_fifo\_rd\_en\_i : std logic vector (G VMM NUM - 1 downto 0); 79 : std logic; signal o\_vmm\_data\_fifo\_clear\_i 80 signal o\_hdmi\_link\_state\_acq\_i : std logic; 81 : std logic vector (G VMM NUM - 1 downto 0); signal o\_vmm\_tki\_i 82 signal o\_vmm\_bcr\_i : std logic; 83 signal o\_vmm\_cktp\_generator\_en\_i : std logic; 84 : std logic; signal o hdmi 8b10b decoding error i -- t .\* = type type t\_8bl0b\_encoder\_output\_array is array (natural range <>) of std logic vector(C\_8Bl0B\_ENCODER\_OUTPUT\_LEN - 1 downto 0); -- w .\* = wire signal w\_rst\_sync : std logic; signal w\_tx\_data\_10b : t\_8b10b\_encoder\_output\_array(1 downto 0); signal w\_reset\_phy : std logic; signal w rx data bitslip : std logic; signal w ttc : std logic vector (work.hybrid transc rx pkg.C DATA WORD LEN - 1 downto 0); 93 signal w\_ttc\_valid : std logic; 94 signal w rx data 10b : std logic vector (C 8B10B DECODER INPUT LEN - 1 downto 0); 95 signal w\_8b10b\_code\_err : std logic; : std logic; signal w\_8b10b\_disp\_err signal w\_rx\_link\_state\_init : std logic; signal w\_rx\_link\_state\_link : std logic; 99 signal w rx link state idle : std logic; signal w rx link state acq : std logic; : std logic; signal w rx serdes init done -- f .\* = register 103 signal f\_link\_state\_acq : std logic; 104 signal f f link state acq : std logic; : std logic vector (G\_VMM\_NUM - 1 downto 0); 105 signal f\_vmm\_tki 106 signal f\_rx\_serdes\_toggle : std logic; 107 signal f\_rst\_sync : std logic vector (C\_RST\_SYNC\_SHIFT\_REG\_LEN - 1 downto 0); attribute ASYNC REG : string; attribute ASYNC REG of f rst sync : signal is "TRUE"; -- k .\* = combinational logic output 111 signal k reset serdes : std logic;



### RD51 VMM3a hybrid firmware brightness Status summary and future

- Refactoring finished, documentation and writing of test benches still ongoing
- Private bitbucket.com project <u>https://bitbucket.org/europeanspallationsource/vmm3a\_hybrid</u>
- Access can be granted to anybody, not limited to people with CERN or ESS email address
- Project based on latest commit 5c5eb939 from Marek to gitlab.com (02.09.2020 firmware flashed to new hybrids)
- Firmware will now be ported to Spartan7
- After porting, ESS firmware will evolve in different direction : No ART, different BC clock and data clock (ESS facility clock 88 MHz, hence BCCKL 44 MHz, SERDES for HDMI 440 MHz, CKDT 176 MHz DDR)



### Integration of RD51 VMM3a hybrid into ESS Readout

### RD51 VMM3a hybrid at ESS

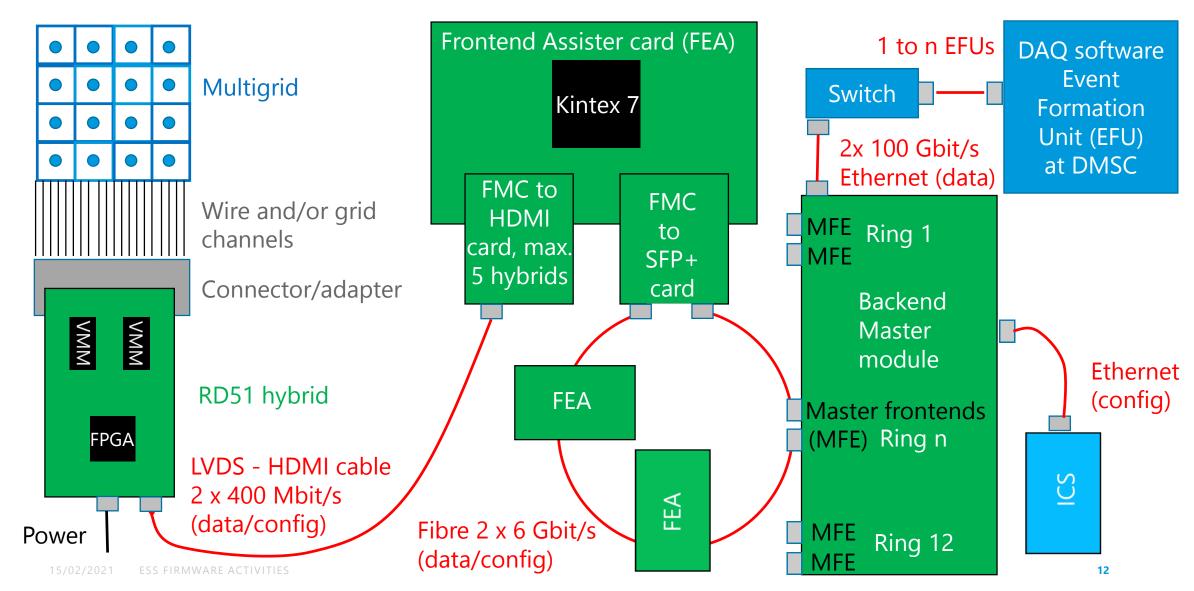


#### Integration into the ESS readout

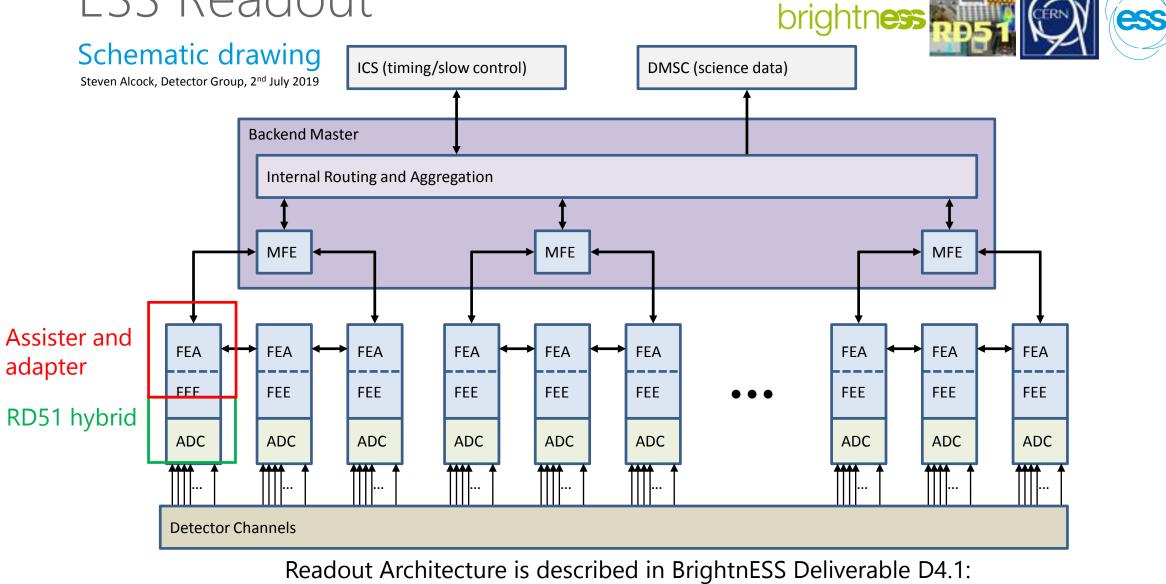
- Since 2018 ESS has shown that VMM3a can also be used for non-MPGD gaseous detectors like Multigrid and Multiblade (analog and digital data taken)
- Multigrid is basically grids of single wires, Multiblade is a cathode strip chamber
- VMM3a is the electronics choice to read out the NMX (GEM), CSPEC (Multigrid), ESTIA, TREX and FREIA (all Multiblade) detectors
- •Successful Multigrid detector review in August, reviewers agree with the choice of RD51 VMM3a hybrid as front end
- Only worry: Limitation of <= 4 Mhits/s per channel might be too low if ESS is operated at full power, in cases of very high instantaneous rates on grid, since a grid has a surface area of several cm<sup>2</sup>

### Readout chain Multigrid





### ESS Readout



https://dx.doi.org/10.17199/BRIGHTNESS.D4.1

### FEA for RD51 hybrid Integration of RD51 hybrid into ESS readout

#### Adapter card connects two RD51 hybrids to the FMC connector of the Kintex KC705 evaluation board

- Upgraded version will contain 5 HDMI ports
- RD51 SRS FEC Virtex6 firmware ported to FEA Kintex 7
- Substantial changes: E.g. new ethernet MAC since IP could not be ported
- No problems with FIFO IP
- Care needed with Xilinx components like SERDES and DELAY





### FEA for RD51 hybrid Integration of RD51 hybrid into ESS readout

- Data transmission via UDP and configuration of VMMs operational
- Xilinx KCU 705 has now all functionalities of the RD51 SRS FEC that are compatible with the hardware of the evaluation board, and can be used with the slow control and ESS DAQ
- Now changing the data format to the ESS data format, and transfer data to the well established assister firmware so that the RD51 hybrid can be used with the full ESS readout (rings, backend)

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# SRS FEC firmware and slow control changes



### Slow control Cleaning up and changes

- Lucian created very nice new repo <u>https://gitlab.cern.ch/rd51-slow-</u> <u>control/vmmsc</u>
- Major clean-up, restructuring and adding of new features
- Hard reset for all VMMs, copy of channel settings to all VMMs, new calibration features
- For fitting of data (linear and non-linear regression), integration of alglib (cross-platform numerical analysis and data processing library) https://www.alglib.net/
- In ESS branch work in progress, implementation of new features, in master branch more stable version

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### FEC firmware

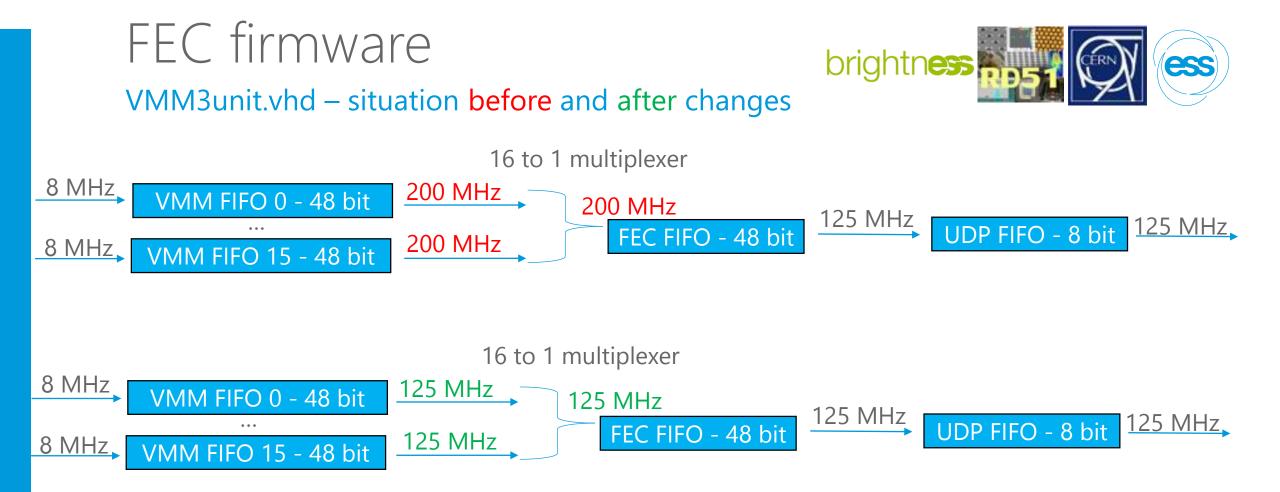
#### Repo, project and timing errors

- Change to Planahead project like hybrid firmware
- Removal of unused modules, cleaning up code, cleaning up constraints file
- Code not yet refactored like hybrid firmware
- Aim of changes: reliable and fast continuous mode without timing errors
- Main sources of timing errors (timing score of around 40000):
- Triggered mode (not correctly working anyway, compared non-gray encoded FEC trigger counter with gray encoded VMM BCID)
- FIFO logic in vmm3unit.vhd
- Due to use of DDR3 memory, logic that determines the next VMM FIFO to read is run at 200 MHz, combinatorial logic too slow to meet timing requirements

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-MAXPERIOD (6)		it/daqbik.wr[4].u vmm fifo/U0/xst fifid.cstr/ramloop[0].ram.r/v6 noinit.ram/SDP.WIDE PRIM36.ram	appUnit i/Inst vmm3unit/dagblk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	6.134			5 dk20
- MINHIGHPULSE (88)		it/dadbik.wr[4].u vmm fifoAJ0/xst fifid.cstr.hamloop[0].ram.r/v6 noinit.ram/SDP.WIDE PRIM36.ram	appUnit i/Inst vmm3unit/dappk.u fec fifoJU0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	6.086			5 dk20
- MINLOWPULSE (43)	Path 5 -1.167 anni Init Minst ymm Bun	it/daqbik.wr[4].u vmm fifo/U0/xst fifid.cstr/ramloop[0].ram.r/v6 noinit.ram/SDP.WIDE PRIM36.ram	appUnit i/Inst vmm3unit/dagblk.u fec fifo/U0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	6.035			5 dk20
-MINPERIOD (209)		it/daobik.wr[4].u ymm fifoAJ0/xst fifid.cstr/ram/pop[0].ram.r/v6 noinit.ram/SDP.WIDE PRIM36.ram	appUnit (/Inst_vmm3unit/dagblk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	6.021			5 dk20
		it/dagbik.wr[4].u vmm fifo/U0/xst fifid.cstr/ramloop[0].ram.r/v6 noinit.ram/SDP.WIDE PRIM36.ram	appUnit i/Inst vmm3unit/dappk.u fec fifo/U0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	6.001	3.192	46.8	5 dk20
		it/daqbik.wr[4].u. vmm_fifo/U0/xst_fifid.cstr/ramloop[0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit i/Inst vmm3unit/dagblk.u fec fifo/U0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	5.995			5 dk20
		it/daobik.wr[4].u vmm fifo/Li0/xst fifid.cstr/ramloop[0].ram.r/v6 noinit.ram/SDP.WIDE PRIM36.ram	appUnit_i/Inst_vmm3unit/dagblk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.990			5 dk20
		it/daqblk.wr[4].u vmm fifo/U0/xst fifid.cstr/ramloop[0].ram.r/v6 noinit.ram/SDP.WIDE PRIM36.ram	appUnit_j/bnst_vmm3unit/dagbk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SDMPLE_PRIM36.ram	5.986			5 dk20
		it/dagbik.wr[4].u_vmm_fifo/U0/xst_fifid.cstr/ramloop[0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit //Inst_vmm3unit/dagblk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.959			5 dk20
		it/dadbik.wr[4].u vmm fifo/U0/xst fifid.cstr/ramlooo[0].ram.r/v6 noinit.ram/SDP.WIDE PRIM36.ram	appUnit i/Inst vmm3unit/dappk.u fec fifo/U0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	5.906			5 dk20
		it/dagbik.wr[4].u. vmm_fifo/U0/xst_fifid.cstr/ramloop(0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit i/Inst vmm3unit/dagblk.u_fec_fifo/U0/x[0].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.890			5 dk20
		it/dadbik.wr[8].u ymm fifo/U0/xst fifid.cstr/ram/oco[0].ram.r/v6 noinit.ram/SDP.WIDE PRIM36.ram	appUnit i/Inst vmm3unit/dappk.u fec fifo/U0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	5.815			5 dk20
		it/dagbik.wr[3].u ymm fifo/U0/vst fifid.cstr/ram/oop[0].ram.r/v6 noinit.ram/SDP.WIDE PRIM36.ram	appUnit i/Inst vmm3unit/dapblk.u fec fifo/U0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	5.782			5 dk20
		it/daobik.wr[0].u_vmm_fifo,U0/xst_fifid.cstr/ramloop[0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit i/Inst_vmm3unit/dagblk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.781			5 dk20
		it/dagbik.wr[2].u ymm fifo/U0/xst_fifid.cstr/ram/oop[0].ram.r/v6_noinit.ram/SOP.WIDE_PRIM36.ram	appUnit i/Inst vmm3unit/dappk.u fec fifo/U0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	5.762			5 dk20
		it/dagblk.wr[13].u. vmm_fifo/U0/xst_fiid.cstr/ramloop(0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit i/Inst vmm3unit/dagbk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.744			5 dk20
		it/dacbik.wr[4].u_vmm_fifo/U0/xst_fifid.cstr/ramloop[0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit_i/Inst_vmm3unit/dagblc.u_fec_fifo/U0/x[1].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.750			5 dk20
		it/dagbik.wr/9).u vmm fifo/U0/vst fifid.cstr.hamloop/01.ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit i/Inst vmm3unit/dapbk.u fec fifo/U0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	5.757			5 dk20
		it/daobik.wr[9].u_vmm_fifo/U0/xst_fifid.cstr/ramloop(0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit //Inst_vmm3unit/dagbk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.755			5 dk20
		it/daobik.wr[12].u_vmm_fifo/U0/xst_fiid.cstr/ranloop(0).ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit_j/Inst_vmm3unit/dagblk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.700			5 dk20
		it/dadbik.wr[3].u. vmm_fifo/U0/xst_fifid.cstr.iramloop(0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit i/Inst vmm3unit/dapbk.u fec fifo/J0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	5.686			5 dk20
		it/daoblk.wr[1].u_vmm_fifo/U0/vst_fifid.cstr/ramloop[0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit j/Inst_vmm3unit/dagblk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.678			5 dk20
		it/dadblk.wr[5].u_vmm_fifo.U0/vst_fifid.cstr.iramloop[0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit i/Inst vmm3unit/dapblk.u fec fifo/U0/x[2].ram.r/v6 nonit.ram/SDP.SIMPLE PRIM36.ram	5.674			5 ck20
		it/daobik.wr[11].u. ymm fifo/U0/xst_fiid.cstr/ramloop[0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit i/Inst vmm3unit/dagblk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.661			5 dk20
		it/daobik.wr[3].u_vmm_fifo/U0/xst_fifid.cstr/ramloop[0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit //Inst_vmm3unit/dagblk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.640			5 dk20
		it/dadbik.wr[11].u. ymm fifo/U0/xst. fiid.cstr/ramloop[0].ram.r/y6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit i/Inst vmm3unit/dapbk.u fec. fifo/J0/x[2].ram.r/v6 nomit.ram/SDP.SIMPLE PRIM36.ram	5.659			5 dk20
		it/daoblk.wr[0].u.vmm_fifo/U0/vst_fifid.cstr/ramloop[0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit i/Inst vmm3unit/dagblk.u fec fifo/U0/x[2].ram.r/v6 noinit.ram/SDP.SIMPLE PRIM36.ram	5.653			5 dk20
		it/dacjok.wr[12].u_vmm_ffo/U0/xst_fiid.cstr/ramloop[0].ram.r/v6_noinit.ram/SDP.WIDE_PRIM36.ram	appUnit_//Inst_vmm3unit/dagblk.u_fec_fifo/U0/x[2].ram.r/v6_noinit.ram/SDP.SIMPLE_PRIM36.ram	5.632			5 ck20
		PERIOD TIMEGRP "sysUnit   Inst sysCliMgrCTF dock unit ckfx" TS ck200 / 0.2 HIGH 50%; (					
		it/daqbik.wr[8].u ymm fifo/U0/xst fifo/gcanyfifo.rf/grf.rf/gnty ar sync fifo.gcx.dkx/rd pntr ac 3	appUnit i/Inst vmm3unit/dagblk.wr[8].u vmm fifofo.gcx.ckx/gsvnc stage[1].wr stg inst/Q reg 3	1.449	0.435	70.0	2 dk20
		it/dadbik.wr[8].u vmm fifo/U0/xst fifo/gconvfifo.rf/grf.rf/gntv or sync fifo.gcx.clxx/rd pntr gc 1	applinit i/Inst vmm3unit/dapbk.wr/81.u vmm fifofo.gcx.ckx/gsvnc stage[1].wr stg inst/O reg 1				2 dk20
		it/daqbik.wr[12].u ymm fifo/U0/xst fifo/gconvfifo.rf/grf.rf/gnty or sync fifo.gcx.ckx/rd pntr gc 5	appUnit i/Inst vmm3unit/dagblk.wr[12].u vmm fiffo.gcx.ckx/gsvnc stage[1].wr stg inst/O reg 5				2 dk200
		it/dagbik.wr[8].u ymm fifo/U0/xst fifo/gconvfifo.rf/grf.rf/gntv or sync fifo.gcx.dkx/rd pntr.gc 0	appUnit i/Inst vmm3unit/dagblk.wr[8].u vmm_fifofo.gcx.ckx/gsync_stage[1].wr_stg_inst/Q_reg_0				2 dk200
		it/dagbik.wr[3].u ymm fifo/U0/xst fifo/gconyfifo.rf/grf.rf/gnty or sync fifo.gcx.dkx/rd pntr gc 8	appUnit i/Inst vmm3unit/dagbik.wr[3].u vmm fifofo.gcx.ckx/gsvnc stage[1].wr stg inst/O reg 8				2 dk200
		it/dadbk.wr[8].u vmm fifo/U0/xst fifo/gconvfifo.rf/grf.rf/gntv or sync fifo.gcx.dkx/rd pntr gc 6	appUnit //Inst vmm3unit/dagbk.wr[8].u vmm fifofo.gcx.ckx/gsvnc stage[1].wr stg inst/Q reg 6				2 dk20
		it/dadpk.wr[3].u_vmm_fifo/U0/xst_fifo/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.ckx/rd_pntr_gc_6	appUnit //Inst_vmm3unit/dagbk.wr[3].u_vmm_fifofo.gcx.ckx/gsync_stage[1].wr_stg_inst/Q_reg_6				2 dk20
	1						



831	check if the pointed vmm_fifo has data and the connected fifo is full or no
832	vmm3_rden_gen : FOR i IN 0 TO 15 GENERATE
833	PROCESS (nextvmmpointer, fec_fifo_pgfull, vmm_fifo_emptyn)
834	BEGIN
835	IF nextvmmpointer = i THEN
836	IF vmm_fifo_emptyn(i) = '1' THEN
837	IF fec_fifo_pgfull = '0' THEN
838	<pre>vmm_fifo_rden(i) &lt;= 'l';</pre>
839	ELSE
840	<pre>vmm_fifo_rden(i) &lt;= '0';</pre>
841	END IF;
842	ELSE
843	<pre>vmm_fifo_rden(i) &lt;= '0';</pre>
844	END IF;
845	ELSE
846	<pre>vmm_fifo_rden(i) &lt;= '0';</pre>
847	END IF;
848	END PROCESS;
849	END GENERATE;
850	
851	look for a nonempty vmm_fifo
852	<pre>vmm_fifo_emptyn &lt;= cfg_chmask(15 DOWNTO 0) AND (NOT vmm_fifo_empty);</pre>
853	
854	PROCESS (clk200)
855	VARIABLE var1 : INTEGER RANGE 0 TO 15 := 0;
856	VARIABLE var2 : INTEGER RANGE 0 TO 15 := 0;
857	BEGIN
858	var1 := 0;
859	var2 := 0;
860	IF rising_edge(clk200) THEN
861	FOR i IN 0 TO 15 LOOP
862	IF vmm_fifo_emptyn(15-i) = '1' THEN
863	varl := 15 - i;
864	IF 15 - i > nextvmmpointer THEN
865	var2 := 15 - i;
866	END IF;
867	END IF;
868	END LOOP;
869	IF var2 > var1 THEN
870	<pre>nextvmmpointer &lt;= var2;</pre>
871	ELSE
872	<pre>nextvmmpointer &lt;= varl;</pre>
873	END IF;
874	END IF;
875	END PROCESS;



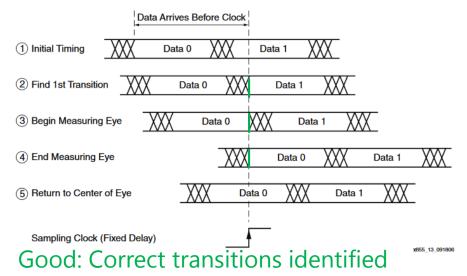
- Bottleneck is UDP, 8bit send with125 MHz (1 Gbits/s ethernet)
- Reading of the 48 bit VMM FIFOs with 200 MHz does not make sense, choosing VMM FIFO to read and write to FEC FIFO does not work at 200 MHz (logic too slow)
- Performance stays the same, if VMM FIFOs are read with 125 MHz, and FEC FIFO is written with 125 MHz, timing is met

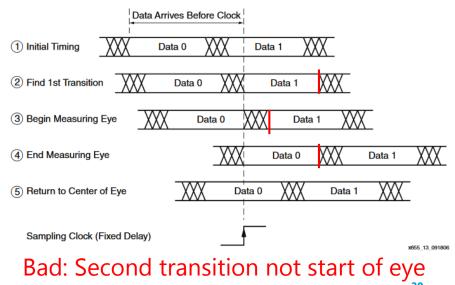
### FEC firmware

#### Link status

- HDMI SERDES use master and slave ISERDES\_NODELAY together with IODELAY
- IODELAY has 64 taps of 78 ps that can shift the data (tap 64 is identical to tap 0 again)
- ISERDES can do bitslip to rearrange the 10 bits (after 10 bitslips one arrives again at the original word)
- Aim of alignment: To be in the center of the eye and receive correct 8b/10b control word from Spartan 6 on hybrid (link control word)
- Originally FEC was using bit align machine of Xilinx <u>https://www.xilinx.com/support/documentation/application\_notes/xapp855.pdf</u>
- Problem: If after finding the first transition, the second transition that is found is not on the other side of the window, but just the end of the same transition as the first, the center of the eye is not found
- Therefore Xilinx released update
   <u>https://www.xilinx.com/support/answers/38672.html</u>
- Now user has to set a parameter that specifies the minimum width of the eye, to avoid the identification of a transition as eye
- With new DVM card, XAPP855 was unstable, thus successfully implemented update in spring 2020







### FEC firmware

#### Link status



- When using the CTF card, we still had problems to obtain a stable link status 4 (probably the minimum eye width parameter would have to be adapted per channel and would be different for use with CTF and without)
- I implemented thus my own bit align code, based on firmware I wrote for the Kintex 7
- On Kintex 7, the Xilinx bit align machine does not work anymore at all (no surprise, it was for Virtex 5)
- IODELAY has only 32 taps of 78 ps, so that one cannot scan through the whole eye when running the SERDES with 400 MHz (delays between 0 and 2.418 ns possible), 400 MHz is slow for Series 7
- New code measures all combinations of bitslip and tap and chooses setting in the center of the largest stable region
- A tab /bit slip combination is stable if the correct link word has been received 128 times in a row
- If e.g. at the same bit slip, taps 10-30 are stable, we have a stable region of 21 taps for this bit slip. The center of the window is then tap 20
- After changes a very stable link status 4 is obtained with or without CTF on all HDMI ports

#### NIM trigger and multiple test pulses



- For trigger in and trigger out now the "polarity" of the digital signal can be set via the slow control
- Trigger input can be given out on trigger output
- Alternatively, trigger output can be configured to occur at any time in the cycle
- Michael's "Registering trigger timestamp feature" unchanged, just checkbox removed, as soon as the trigger input is activated in the slow control, timestamp is sent out
- Instead of starting the acquisition directly after clicking "ACQ ON" in the slow control, feature to only start the acquisition with the arrival of the first NIM trigger
- It is now possible to have several internal test pulses at defined times

PEC1         Send       Paders FEC         10002       FEC1         Rest Warnings       Paders FEC         Address FEC       Paders FEC         10002       FEC1         NAM       VAM         VI       V         VI       V         VI       V         VI       V         VI       VI         VI       VI         VI       VI         VI       VI         VI       VI         VI       VII         VIII       VIIII         VIIII       VIIIII         VIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Slow Control Calibration	Logging Testing				
Seen d       P address FEC         I 00.02 FEC P       HOMI 2         HOMI       VMM 1         VMM 1       VMM 2         G       0.0.02 FEC P         I 1 2 3 4       Postion 7 8         Acquasiton/Test pulse       VMM 1         Acquasiton/Test pulse       Postion 8         Acquasiton/Test pulse       Postion 0         Postion 0       Postion 0		FEC 1				
Bend         P advess FEC           Send         DUM 2           Nome         Dum 2           Hond         VMM         VMM         VMM           VIM         VMM         VMM         VMM         VMM           VIM         VIM         VIM         VIM         VIM         VIM         VIM           C         AcquisitonTest pulse         VIM	pen Communication					
Send         HOM 2           Reset Warnings         10.00.2 [FEC/P] 10.00.8 DAD/P         Hybrid           I 10.00.2 [FEC/P] 10.00.8 DAD/P         Hybrid         VMM V MM 2           C         Acquisition/Test place         Hybrid           I 10.00.2 [FEC/P] 2.2 [10.00.8 DAD/P         Hybrid         VMM V MM 2           C         Acquisition/Test place         Hybrid I 1/2 [ Postion         Postion         C           Acquisition/Test place         Hybrid II 1/2 [ Postion         Postion         C         C           Acquisition/Test place         Hybrid III 1/2 [ Postion         Postion         C         C           I 10.0 g dise fear IT Tree debug data format         Adamset Strings         C         C         FeadADC         44 565 1/2 (1)         C         C         FeadADC         44 565 1/2 (1)         C         FeadADC         <		IP address FEC				
0.000       0.00.0 DD /P       Hohid       Hybrid 1         HDMI       YMA       VMA       VMA         HDMI       YMA       VMA       VMA         C       Acquisition/Test pulse       Adarced Strings       S20 b       S20 b </td <td>unre</td> <td></td> <td>HDMI 2</td> <td></td> <td></td> <td></td>	unre		HDMI 2			
HDM       I       VIAI       Carread Settings       Charnel Settings       Chare       Chare       Charn	Send		Hubrid			
Reset Warnings       I V 2 3 4         I V 2 3 4         S 6 7 8         Acquisition/Test pulse         Acquisition/Test pulse         Acquisition/Test pulse         Acquisition/Test pulse         Acquisition/Test pulse         Acquisition/Test pulse         Acquise channel Settings         Position 0         Action Cannel Settings         Bebrage tablemany			Typha	Hybrid 1		
Reset Warnings       1 1 2 3 4       4         1 1 2 3 4       4         2 4       6 6 7 8       8         2 4       reset       Jatancy TP         3 6 6 6 7 8       8       10 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		HDMI		VMM	VMM 1 VMM 2	
C       Acquisition/Test poles       Position         41       Acquisition/Test poles       Axis       X         42       figst       Axis       X         42       figst       Axis       X         43       X       Position       Axis       X         44       figst       Position       Position       Position       Position         44       figst       Position       Position       Position       Position       Position         44       figst       Position       P	Reset Warnings	1 2 3 4				
C       Acquisition/Test pulse       Position       Position       Analog (Channel) Monitor Test pulse       SC SL ST STH SM 0 mV + 0 ms + 0 mt + 1         1       4 c		5 6 7 8		✓ 1 ✓ 2	General Settings Advanced Settings	
C       Analog (Channel) Montor Temperature sensor       Sk: Sk: Ski: Ski: Ski: Ski: Ski: Ski: Sk	_			Position	Input charge polarity negative -	
1       Aus	C	Acquisition/ lest pulse			Analog (Channel) Monitor Temperature sensor	SC SL SI SIH SM U mV + SMX U mV + U ns + U m +
12       ada latency maximum       Position 0       1       0 <t< td=""><td>1</td><td></td><td></td><td>Axis X •</td><td></td><td>0 0 mV - 0 mV - 0 mV - 0 mV - 0 m' -</td></t<>	1			Axis X •		0 0 mV - 0 mV - 0 mV - 0 mV - 0 m' -
13       14000\$ maximum         14       6       data latency error         15       data latency error       12C         14       15       0 mW + 0 mW	2	intericy		Position 0	Gain (sg) 3.0 mV/fC *	
14       6       deta latency error       Pack time (st)       20 ns       1         15       1       0 mV + 0 mV					TAC Slop Adj (stc) 60 ns 👻	
14       Image error       Hybrid ID       Hybrid ID       ReadADC       44 8649 °C       Image All Peak         15       66       63       1atency TP       ReadADC       44 8649 °C       Image All Peak         16       100       offset first TF       ReadADC       1atency TP       0mV + 0mV	3	data latency		I2C	Peak time (st) 200 ns	
5       0 doub dual domain         6       1 doub dual domain         7       100 0 dota domain         7       100 0 dota first TF         100 0 dota first TFs       S6         1 0 runs pris       S6         1 0 runs pris       S6         1 0 runs pris       CKBC 40MHz *         Aco on       CKBC 40MHz *         Aco on       CKBC 40MHz *         Aco on       CKBC 0 on s *         S6       CKBC 0 on s *         Aco off       CKBC 0 on s *         First trigger       CKBC 0 on s *         S6       CKBC 0 on s *         S6 ACC (Pirect out) 25 ns       100 *         Co on V + 0 on V + 0 on V + 0 on V + 0 on S * 0 m *         Test Pulse       CKDT 180 MHz *         Vidit 128/22*       Polarity Positi*         Vidit 128/22*       Polarity Positi*         Apply to all VIMMs       30 0 mV + 0 mV	4	error		Hybrid ID 🔹		
16       63       1atency TP         7       100       offset first TF         18       100       offset first TF         100       offset first TF         100       offset first TF         100       offset first TF         110       umber of         110       trigger law         110       offset first TF         1100       offset first TF         11000       offset	5	debug data format			ReadADC 44.8649 °C +	
77       100 w diskty fr       Read         88       100 w diskty fr       S6         1 w Trys of diskt first TF       S6         1 w Trys of diskt first					SRAT Mode Timing At Peak 👻	
100 ° offset first TF       S6         1 ° unwber of TFS       CKBC 40MHz *         1 ° unwber of TTS       CKBC 0 · o mv *         1 ° unwber of TTS       CKBC 0 · o mv *         1 ° unwber of TTS       CKDT 180 MH: *         0 ° unvber of TTS       0 ° mv *       0 ° mv *		63 📮 latency TP		Read		
38       1       • member of Tres         20 for all FECs       0 move of tres       0 m/v       0 m/v <td< td=""><td>7</td><td>100 🗘 offset first TF</td><td></td><td>66</td><td>Neighbor Trigger (sng) Disable At Peak</td><td></td></td<>	7	100 🗘 offset first TF		66	Neighbor Trigger (sng) Disable At Peak	
Q for all FECS       I to s       offset next TPs mext Tps inset trigger Out starts ACQ       VI 1       CKBC 40MHz *       ADC         First trigger starts ACQ       I innomal *       Trigger Out Tigger Out Tigger Out       VI 1       CKBC 40MHz *       ADC         ACQ On       VI 1       CKBC 0 0n s *       Bb ADC (Jinet out) 25 n s *       III *       0 mV * 0 ms * 0 m* *         ACQ Off       0 mV * 0 ms * 0 m*       0 mV * 0 ms * 0 m* *       0 mV * 0 ms * 0 m* *         ACQ Off       0 m 0 m       0 mV * 0 ms * 0 m* *       0 mV * 0 ms * 0 m* *         Ming file       CKDT 180 MH: *       CKDT 180 MH: *       Dual Clock 8-bit         Warn Int FEC       System Parameters       Test Pulse       Threshold DAC 250 ‡ 225 mV       III * 0 mV * 0 ms * 0 m* *         System Parameters       Clear info       0 mV * 0 ms * 0 m* *       0 mV * 0 ms * 0 m* *       0 mV * 0 ms * 0 m* *         Apply to all VMMs       20 * 0 mV * 0 mV * 0 ms * 0 m* *       0 mV * 0 mV * 0 ms * 0 m* *       0 mV * 0 mV * 0 mV * 0 ms * 0 m* *	8	number of		50	Analog tristates Sub Hysterisis	
ACQ Off       Off       CKBC 40MH2         ACQ Off       Off       CKBC 00 ns *         ACQ Off       Off       CKDT 180 MH2         ACQ Off       Off       CKDT 180 MH2         Pic Status       CKDT 180 MH2       Dual Clock ART Dual Clock Dats Dual Clock 6-bit         Pic Status       Test Pulse       Test Pulse         Vidth 128/2*       Polarity Positi*       Test Pulse         Apply to all VMMs       0 mV + 0 mv + 0 ns + 0 m*         30 0 mV + 0 mv + 0 ns + 0 m*       0 mV + 0 ns + 0 m*         Acq Off       Off         Pic Status       CKDT 180 MH2*         Apply to all VMMs       0 mV + 0 ns + 0 m*		TPs				11 0 0 mV + 0 mV + 0 mV + 0 m + 0 m +
First trigger starts ACQ       Immed imigger lui       CKBC 400/m2 *         ACQ On       CKBC 00 ns *         ACQ Off       CKBC 00 ns *         ACQ Off       OmV *       OmV *       OmV *       OmV *       OmV *         ACQ Off       Om       OmV *       OmV *       OmV *       OmV *       OmV *         ACQ Off       Om       Om       OmV *       OmV *       OmV *       OmV *       OmV *         ACQ Off       On       Off       CKDT 180 MH **       CKDT 180 MH **       Dual Clock 5-bit       Dual Clock 5-bit       Dial Clock 5-bit       OmV *	Q for all FECs				ADC	12 🛛 🖉 💭 OmV 🕶 OmV 🕶 Ons 🕶 Om) 💌
Internal * Trigger Out       Skew       0 00 ns *         ACQ Off       0 mV *       0 mV * <t< td=""><td></td><td>next IPs</td><td>⊻ 1</td><td>CKBC 40MHz *</td><td>ADCs on/off 8-bit Conv. Mode</td><td>13 🛛 🗧 💭 0 mV 🕶 🖉 0 mV 🖛 0 ns 💌 0 m' 👻</td></t<>		next IPs	⊻ 1	CKBC 40MHz *	ADCs on/off 8-bit Conv. Mode	13 🛛 🗧 💭 0 mV 🕶 🖉 0 mV 🖛 0 ns 💌 0 m' 👻
starts AČQ       normal ~ Trigger Out       CKBC       0.00 ns ~       CKBC       0.00 ns ~         ACQ On       Trigger Out       Skew       0.00 ns ~       6b ADC (Direct out)       25 ns ~       16       0 mV ~       0	- First trigger	invert 👻 Trigger In			10b ADC (Ampl) 200 pc	14
ACQ On		normal x Triagor Out				
ACQ On       Image: Status       Status       Status       CKDT 180 MH: *       Dual Clock Case       Dual Clock 6-bit       D mV + 0 mV +				CKBC 0.00 ns *	6b ADC (Direct out) 25 ns *	
ACQ         Off         CKDT         Dual Clock         Dual Clock         Iff         Iff         Iff         Off	ACO On	40 Time		skew	8b ADC (Time) 100 ns 👻	
ACQ Off       On       Off       CKDT       180 MH+*       Dual Clock ART       Dual Clock 5-bit       20       0 mV +       0 mV	Add on					
On         Off         CKDT         100 MH: *         Dual Clock ART         Dual Clock 6-bit         21         0 mV *         0 mV * <th< td=""><td></td><td>ACQ</td><td></td><td></td><td>Dual Clock</td><td></td></th<>		ACQ			Dual Clock	
FEC Status       Fest Pulse         Warm init FEC       Test Pulse         System Parameters       Skew Ons *         Width 128/21*       Polarity Positin*         Polarity Positin*       Apply to all VMMs	ACQ Off	On Off		CKDT 180 MH; -	Duel Cleak ABT, Duel Cleak Date, Duel Cleak & bit	
FEC Status     23     0 mV + 0 mV + 0 nm + 0 mN + 0					Dual Clock ART Dual Clock Data Dual Clock 6-bit	
Warm Int FEC         Test Pulse           Link Status         System Parameters           System Parameters         Skew Ons *           Ubdd         Ubdd           Load         D mV + 0 mV + 0 ms + 0 mh +		FEC Status				
Visit Rest         Dest Pulse         Threshold DAC         250         252 mV         250         0 mV +         0 mV + <t< td=""><td>nfig file</td><td>Warm Init EEC</td><td></td><td></td><td></td><td></td></t<>	nfig file	Warm Init EEC				
ybrid2         Link class         Skew Ons *         Test Pulse DAC 655 ‡ 714 mV DAC         26         0 mV * 0 mV * 0 ns * 0 m' *           System Parameters         Width 12b:2*         Polarity Positiv. *         Polarity Positiv. *         Apply to all VMMs         26         0 mV * 0 mV * 0 ns * 0 m' *           Load         0 mV * 0 mV * 0 ns * 0 m' *         0 mV * 0 nv * 0 nv * 0 mv *         0 mV * 0 nv * 0 nv *				lest Pulse	Threshold DAC 250 225 mV	
Clear Info         Width         128x2: *         28         0	iybrid2			Skew Ons -	Test Pulse DAC 959 1 714 mV DAC	
Load         28         0 mV + 0 mV + 0 ns + 0 mV +           Polarity Positin +         Apply to all VMMs         29         0 mV + 0 mV + 0 ns + 0 mV +           Load         0 mV + 0 mV				M/dth 128x21 -	800 mV pulse height	27 🔲 📕 💭 0 mV 🕶 0 mV 🖛 0 ns 👻 0 m' 👻
Load Apply to all VMMS 30 0 mV + 0 mV + 0 mV + 0 mV +		Oldar mild				28 🛛 💭 💭 🐨 💭 0 mV 🕶 🖉 0 mV 🕶 🖉 0 m' 🕶
Load 30 0 mV + 0				Polarity Positiv *	Apply to all VMMs	
	Load			Apply to all hybrids	Hard Reset	$30 \qquad \qquad$

#### Continuous data taking without window

- For the use at ESS (neutron time of flight measurements), we have to be able to take data all the time without regularly occurring dead time
- BC clock at ESS will be derived from facility clock and have fixed relation with proton pulse
- Problem so far has been the overflow of the BCID on the VMM
- As a 12 bit value, the BCID on the VMM only covers times between 0 and 102.4 us (at 40 MHz)
- Due to limited bandwidth, we do not add a higher order timestamp to the hits on the Spartan6, since then the hit size would considerably increase from 40 bits to >= 100 bits
- Higher order 42 bit timestamp with 25 ns resolution and a BCID overflow counter (offset) is added upon arrival of the hits on the FEC

Logging Testing				
cogging rooming				
FEC 1				
IP address FEC	HDMI 2			
10.0.0.2 FEC IP				
10.0.0.3 DAQ IP	Hybrid	Hybrid 1		
HDMI		VANA	VMM 1 VMM 2	
1 🗸 2 🗌 3 🗌 4		VMM		
5 6 7 8		✓ 1 ✓ 2	General Settings Advanced Settings	Channel Settings
		Position	Input charge polarity negative -	SD SZ010b SZ08b SZ06b
Acquisition/Test pulse			Analog (Channel) Monitor Temperature sensor 🔻	SC SL ST STH SM 0 mV * SMX 0 mV * 0 ns * 0 m' *
47 atency		Axis X 👻		0 0 mV - 0 mV - 0 mV - 0 m' -
intency		Position 0	Gain (sg) 3.0 mV/fC -	1 0 0 mV - 0 mV - 0 mV - 0 mV -
4000 Cata latency maximum			TAC Slop Adj (stc) 60 ns 👻	2 0 mV - 0 mV - 0 ns - 0 mV -
6 Cata latency error		I2C	Peak time (st) 200 ns 👻	3 0 0 mV - 4 0 mV - 0 m
61101		Hybrid ID *	ReadADC 44.8649 °C	5 0 0 WV + 0 WV + 0 mV + 0 mV +
debug data format			SRAT Mode Timing At Peak *	6 0 mV - 0 mV - 0 mV - 0 m' -
63  Clatency TP		Read	Citer Mode Inning Act eak	7 0 mV - 0 mV - 0 mV - 0 mV -
100 🗘 offset first TF			Neighbor Trigger (sng) Disable At Peak	$8 \qquad 0 \text{ mV} \neq 0  $
		S6	Analog tristates Sub Hysterisis	9 0 0 mV - 0 mV - 0 mV - 0 mV - 10 mV - 10 mV - 0 m
1 TPs				11 0 0 mV - 0 mV
1000 Confiset			ADC	12
IIII IIIII	✓ 1	CKBC 40MHz *	ADCs on/off 8-bit Conv. Mode	13
invert 👻 Trigger In			10b ADC (Ampl) 200 ns -	$14 \qquad 0 \qquad mV \neq 0 \qquad mV \qquad mV = 0 \qquad mV \neq 0 \qquad mV = $
normal 👻 Trigger Out			6b ADC (Direct out) 25 ns -	15 0 0 mV + 0 mV + 0 mV + 0 mV + 16 0 mV + 0
40 Trigger Out		CKBC skew 0.00 ns *		17 0 mV + 0 mV + 0 mV + 0 mV + 1 mV + 1
Time			8b ADC (Time) 100 ns 🔹	18
ACQ			Dual Clock	19 0 mV - 0 mV - 0 mV - 0 mV -
On Off		CKDT 180 MH: -		20 0 mV + 0 mV + 0 mV + 0 mV + 21 0 mV + 0 m
			Dual Clock ART Dual Clock Data Dual Clock 6-bit	21 0 mV - 0 mV - 0 mV - 0 mV - 22 0 mV - 0 m
FEC Status				23 0 0 mV - 0 mV
Warm Init FEC		Test Pulse		24 0 0 mV - 0 mV - 0 ns - 0 m' -
Link Status			Threshold DAC 250 225 mV	25 0 mV - 0 mV - 0 mV - 0 m' -
System Parameters		Skew Ons *	Test Pulse DAC 858 + 714 mV DAC 800 mV pulse height	26 0 mV -

Apply to all VMM

Hard Rese

brightness

VMM3 - SRS DCS

Open Commu

Reset Wa

FEC

5 6

7 8 ACQ for all FE

> First trigg starts AC

> > ACQ O

ACQ (

Config file

hybrid2

Load

Save

Clear Info

Width 128x2! -

Polarity Positiv \*

Apply to all hybrids

Sen

) 🔲 0 mV 🔻

0 mV ·

#### Continuous data taking without window

• Challenge: Since the data is read out out from the VMM via the Spartan6 and the HDMI in a serial fashion, there is a large difference between hits arriving with minimum and maximum latency

~

- One solution to ensure data integrity is to use a acceptance window as before
- New solution:
- The FEC has a clock counter (TRG) that counts for each BC clock frequency from 0 to 4095
- At the beginning of the acquisition, the BCID on the VMMs is reset (soft reset), and the S6 FIFO is emptied
- The moment, at which the reset is sent, can be determined with the field "reset latency"
- In the new debug data mode, the value of the FEC clock counter, at which the hit arrived, is sent out in the data instead of the ADC and TDC
- Two steps to set things up:
- The "reset latency" has to be set in such a way, that the BCID and the TRG in Wireshark show the same value (please pulse only one channel)
- If TRG and BCID show the same value, but the BCID too large or too small (e.g. 105 instead of 100), then the "TP latency" has to be increased or decreased

SR	S Header											
	Frame Cou	nter: 26028 (-85510)										
	Data Id: VMM3a Data FEC clock counter at which hit arri											
	FEC ID: 2		unter at which hit arrives									
	UDP Times	tamp: 86917232 (-27161085500)										
	Offset overflow last frame: 12											
>	Hit: 1,	offset: 4, vmmID: 2, ch: 0, bcid: 100,	trg: 99, latency: -1									
>	Hit: 2,	offset: 5, vmmID: 2, ch: 0, bcid: 100,	trg: 99, latency: -1									
>	Hit: 3,	offset: 6, vmmID: 2, ch: 0, bcid: 100,	trg: 100, latency: 0	)								
>	Hit: 4,	offset: 7, vmmID: 2, ch: 0, bcid: 100,	trg: 101, latency: 1									
>	Hit: 5,	offset: 8, vmmID: 2, ch: 0, bcid: 100,	trg: 101, latency: 1									
>	Hit: 6,	offset: 9, vmmID: 2, ch: 0, bcid: 100,	trg: 99, latency: -1									
>	Hit: 7,	offset: 10, vmmID: 2, ch: 0, bcid: 100,	, trg: 100, latency:	0								
>	Hit: 8,	offset: 11, vmmID: 2, ch: 0, bcid: 100,	, trg: 100, latency:	0								
>	Hit: 9,	offset: 12, vmmID: 2, ch: 0, bcid: 100,	, trg: 101, latency:	1								
>	Hit: 10,	offset: 13, vmmID: 2, ch: 0, bcid: 100,	, trg: 99, latency: -	1								
>	Hit: 11,	offset: 14, vmmID: 2, ch: 0, bcid: 100,	, trg: 100, latency:	0								
>	Hit: 12,	offset: 15, vmmID: 2, ch: 0, bcid: 100,	, trg: 100, latency:	0								
>	Marker:	1, VMM ID 2, SRS timestamp: 8153088	50									
>	Marker:	2, VMM ID 3, SRS timestamp: 8153088	30									



#### Continuous data taking without window

- The maximum latency setting now depends on the CKDT setting
- With 180 MHz DDR one hits arrives every 5th 40 MHz clock cycles (yeah!! Thanks to Patrick!!)
- If the 4 hit deep FIFO exists, the maximum latency is 64 x 4 x 5 clock cycles
- If all 64 channels are pulsed 4 times in quick succession, the maximum latency is thus 1280 clock cycles
- Last setting needed is "latency error". We can see that there is a bit of jitter, sometimes a hit that normally arrives at 0 latency will arrive at -1 or +1. This might be due to the internal test pulses (let's do measurements with external pulsers)
- Algorithm for higher order time stamp:
- Everything is set so that a single hit (minimum latency) arrives within the latency error at the same value of the FEC clock counter (TRG) as its BCID (after gray decoding)
- TRG > = BCID and TRG BCID < = maximum latency: current offset
- TRG < BCID and BCID TRG <= latency error: current offset
- TRG < BCID and BCID TRG <= 4096 maximum latency: previous offset
- Other cases: invalid



/	SR:	S Head	er												
		Frame Counter: 32717 (-78821)													
		Data Id: VMM3a Data													
		FEC ID: 2													
	UDP Timestamp: 140136765 (-25830597175)														
	Offset overflow last frame: 12														
	>	Hit:	1,	offset:	9,	vmmID:	2,	ch:	0,	bcid:	100,	trg:	100,	latency:	0
	>	Hit:	-	offset:	-		з,	ch:	0,	bcid:	101,	trg:	100,	latency:	-1
	>	Hit:	з,	offset:	9,	vmmID:	з,	ch:	1,	bcid:	101,	trg:	105,	latency:	4
	>	Hit:	4,	offset:	9,	vmmID:	2,	ch:		bcid:	100,	trg:	105,	latency:	5
		Hit:		offset:			з,	ch:		bcid:	101,	trg:	110,	latency:	9
	>	Hit:	-	offset:	-		з,	ch:	з,	bcid:	101,	trg:	-	latency:	14
		Hit:	-	offset:			2,	ch:	-	bcid:	100,	trg:	110,	latency:	10
		Hit:	-	offset:			-	ch:		bcid:	-	trg:	120,	latency:	19
		Hit:	-	offset:			-	ch:	-	bcid:		trg:	-	latency:	15
		Hit:	-	offset:				ch:	-	bcid:	-	trg:		latency:	24
		Hit:		offset:			-	ch:		bcid:	-	trg:	120,	latency:	20
		Hit:	-	offset:			-	ch:		bcid:	-	trg:		latency:	25
		Hit:	-	offset:			-	ch:	-	bcid:	101,	trg:	130,	latency:	29
		Hit:	-	offset:			2,	ch:	-	bcid:	101,	trg:	130,	latency:	29
		Hit:	-	offset:			з,	ch:	7,	bcid:	101,	trg:	135,	latency:	34
		Hit:		offset:				ch:	-	bcid:	101,	trg:	135,	latency:	34
		Hit:		offset:				ch:		bcid:	-	trg:	-	latency:	40
		Hit:		offset:			з,	ch:	8,	bcid:	101,	trg:	140,	latency:	39
	>	Hit:	-	offset:	-		2,	ch:	9,	bcid:	100,	trg:	-	latency:	45
		Hit:		offset:			-	ch:	-	bcid:	101,	trg:		latency:	44
		Hit:	-	offset:	-		-		-	bcid:	101,	trg:	150,	latency:	49
	>	Hit:		offset:					-	bcid:	100,	trg:	150,	latency:	50
		Hit:		offset:						bcid:	101,	trg:	155,	latency:	54
		Hit:	-	offset:			-		-	bcid:	101,	trg:	155,	latency:	54
		Hit:	-	offset:			-		-	bcid:	-	trg:	160,	latency:	60
		Hit:	-	offset:	-		-		-	bcid:		trg:		latency:	59
		Hit:	-	offset:	-		-		-	bcid:	-	trg:	-	latency:	64
		Hit:		offset:			-		-	bcid:	-	trg:	-	latency:	64
		Hit:		offset:						bcid:	101,	trg:	170,	latency:	69
		Hit:		offset:						bcid:	-	trg:	170,	latency:	69
		Hit:	-	offset:			-		-	bcid:		trg:	175,		74
		Hit:	-	offset:						bcid:		trg:	175,	latency:	74
	>	Hit:	-	offset:			-		-	bcid:	101,	trg:	-	latency:	79
		Hit:	-	offset:	-				-	bcid:	-	trg:	180,	latency:	79
		Hit:	-	offset:			-		-	bcid:	101,	trg:	185,	latency:	84
		Hit:	-	offset:						bcid:	101,	trg:	185,	latency:	84
	>	Hit:	37,	offset:	9,	vmmID:	2,	ch:	18,	bcid:	101,	trg:	190,	latency:	89
						_			-					-	

#### How cool, a new hit every 5 cycles !

#### Continuous data taking without window

- If hits belong to previous offset, offset -1 is added as timestamp
- Only problem arising if offset on the FEC is 0, and a new marker has already been generated
- Then -1 is sent as offset
- This means the 5 bit offset is not a unsigned number any more with valid entries going from 0 to 31, but a signed number with a valid range from -1 to 15
- -16 is used as indicator for a hit that violates the latency conditions, these hits can be discarded by the DAQ (or directly on the FEC if needed)



>	Hit:	436,	offset:	15,	vmmID:	2,	ch:	11,	bcid:	4001,	trg:	4055,	latency:	54
>	Hit:	437,	offset:	15,	vmmID:	з,	ch:	11,	bcid:	4001,	trg:	4055,	latency:	54
>	Hit:	438,	offset:	15,	vmmID:	2,	ch:	12,	bcid:	4000,	trg:	4060,	latency:	60
>	Hit:	439,	offset:	15,	vmmID:	з,	ch:	12,	bcid:	4001,	trg:	4060,	latency:	59
>	Hit:	440,	offset:	15,	vmmID:	2,	ch:	13,	bcid:	4000,	trg:	4065,	latency:	65
>	Hit:	441,	offset:	15,	vmmID:	з,	ch:	13,	bcid:	4001,	trg:	4065,	latency:	64
>	Hit:	442,	offset:	15,	vmmID:	2,	ch:	14,	bcid:	4001,	trg:	4070,	latency:	69
>	Hit:	443,	offset:	15,	vmmID:	з,	ch:	14,	bcid:	4001,	trg:	4070,	latency:	69
>	Hit:	444,	offset:	15,	vmmID:	2,	ch:	15,	bcid:	4000,	trg:	4075,	latency:	75
>	Hit:	445,	offset:	15,	vmmID:	з,	ch:	15,	bcid:	4001,	trg:	4075,	latency:	74
>	Hit:	446,	offset:	15,	vmmID:	2,	ch:	16,	bcid:	4000,	trg:	4080,	latency:	80
>	Hit:	447,	offset:	15,	vmmID:	З,	ch:	16,	bcid:	4001,	trg:	4080,	latency:	79
>	Hit:	448,	offset:	15,	vmmID:	2,	ch:	17,	bcid:	4001,	trg:	4085,	latency:	84
			offset:	-		-		-		-	-	-	latency:	84
>	Hit:	450,	offset:	15,	vmmID:	2,	ch:	18,	bcid:	4001,	trg:	4090,	latency:	89
		-	offset:	-		-		-		-	-	-	latency:	89
>	Hit:	452,	offset:	15,	vmmID:	2,	ch:	19,	bcid:	4001,	trg:	4095,	latency:	94
		-	offset:	-				-				4095,	latency:	94
	Marke		1, VMM 1		·					516236				
			2, VMM :							516236				
	Hit:	1						-		-			latency:	99
	Hit:	1		-				-		4001,		-	latency:	99
	Hit:	1		-				-		4001,			latency:	104
	Hit:	1	offset:	-				-		4001,		-	latency:	104
	Hit:	1	offset:	-				-		4001,		-	latency:	109
	Hit:	1	offset:	-				-		4001,			latency:	109
	Hit:	1	offset:	-				-		4001,		-	latency:	114
>		1	offset:	-				-		4001,			latency:	114
>		1	offset:	-				-		4001,		-	latency:	119
	Hit:	1		-				-		4001,			latency:	119
	Hit:	1		-				-		4000,			latency:	125
>	Hit:	465	offset:	-1,	vmmID:	з,	ch:	25,	bcid:	4001,	trg:	29,	latency:	124

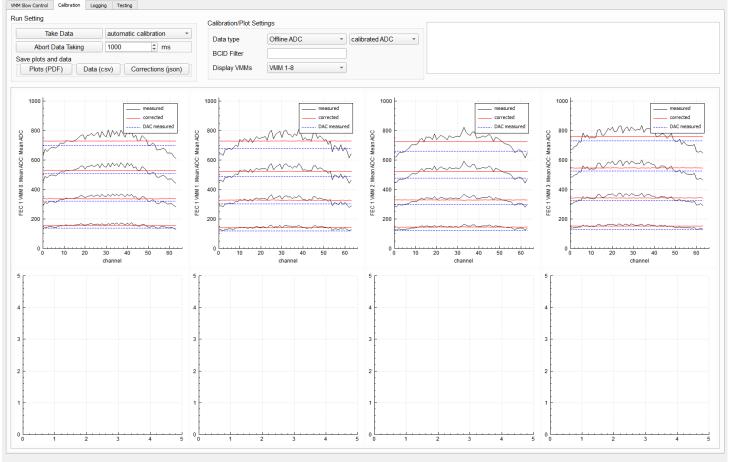
Offset now 5bit signed number, to cover cases where hits arrive after generation of new marker

VMM3 - SRS DCS nev

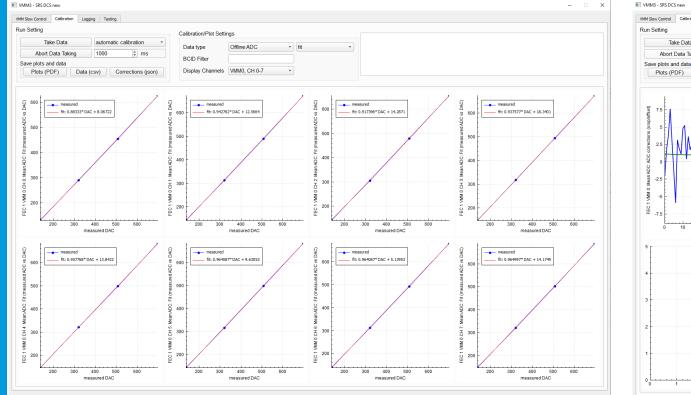
#### New algorithm

- •Pulse all channels with internal test pulses
- •For 4 different pulse heights, measure ADC
- •Measure the actual level in mV of the pulser DAC (observation: using the same DAC values, different VMMs have quite different pulse heights)
- •Fit per channel with pulse height in mV on x-axis, ADC on y-axis and determine slope and offset off the fit
- •Calculate corrections per channel

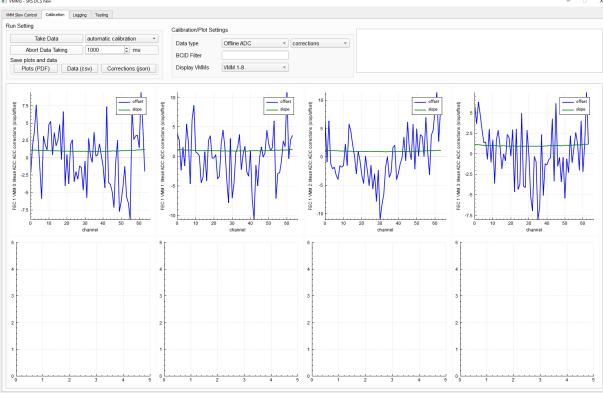




#### Fit and corrections



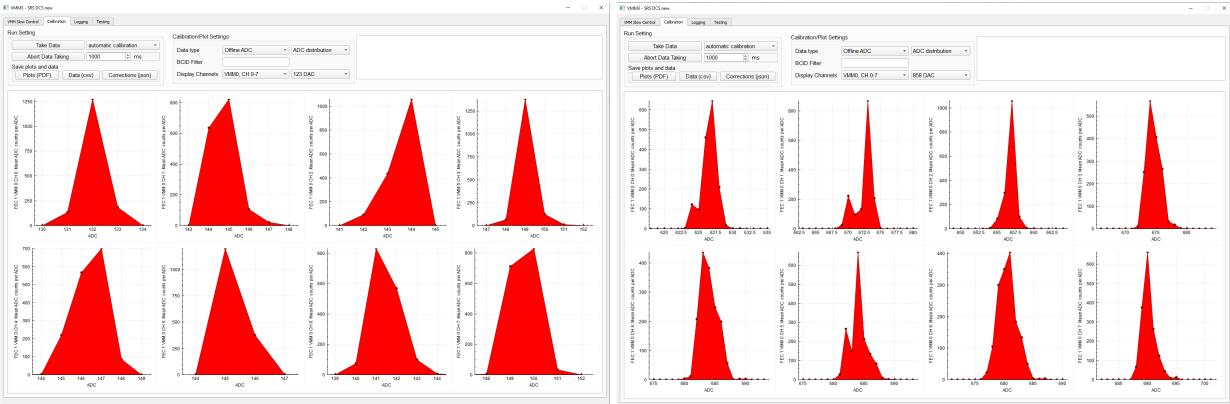
brightness for the second seco



Fit to determine offset and slope corrections Plot per channel Offset and slope corrections Plot per VMM

## brightness

#### ADC distribution

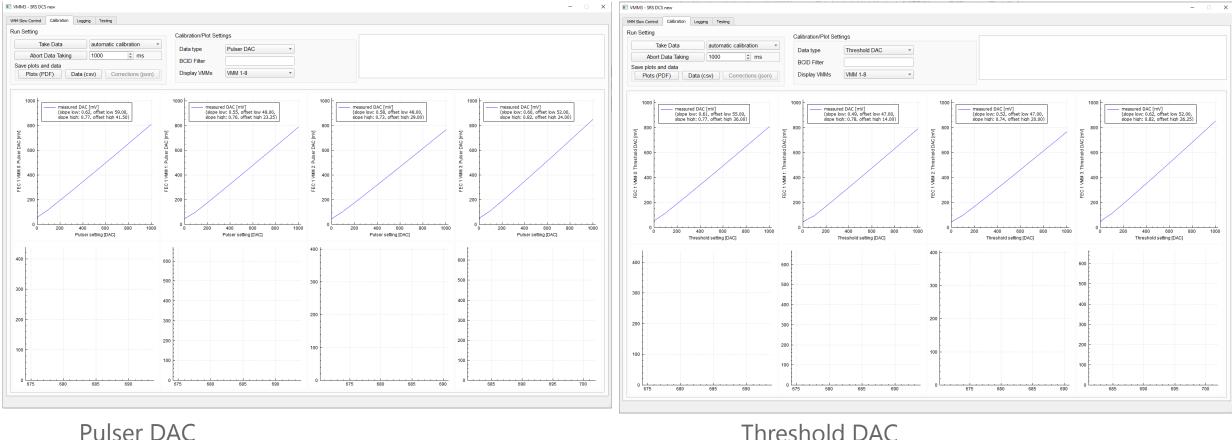


ADC distribution for DAC setting 123 Plot per channel ADC distribution for DAC setting 858 Plot per channel

### Pulser and Threshold DAC



#### Measurement of levels [mV]



Plot per VMM

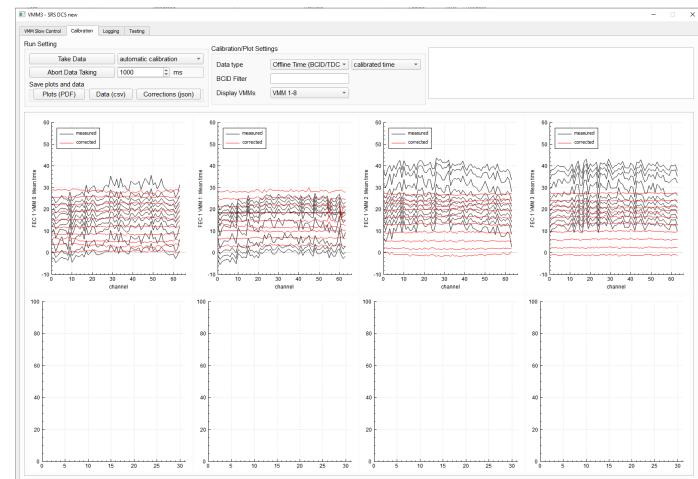
Threshold DAC Plot per VMM

Both DACs have piece-wise two different slopes!

### New algorithm

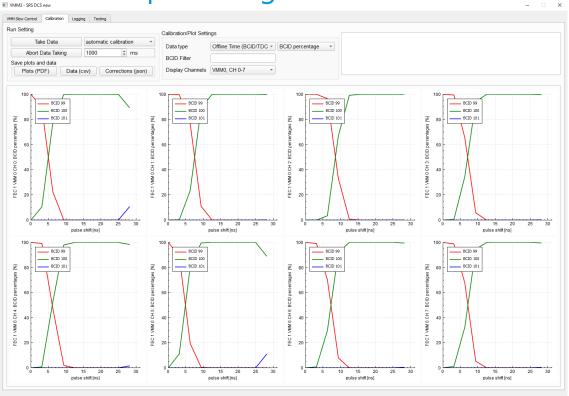
- •Pulse all channels with internal test pulses
- •Shift test pulse between 0 ns and 31.25 ns
- •Measure TDC and the BCID for every channel
- •Look for the time shift where 50% of hits have BCID n and 50% have BCID n+1
- •At this point one has the largest TDC values for BCID n+1 and the smallest TDC values for BCID n





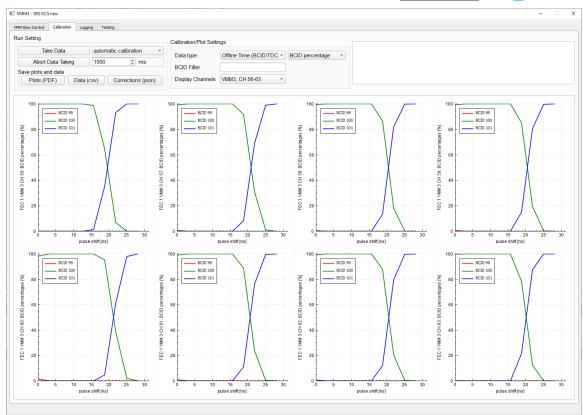
Setting 40 MHz Bc clock, TAC slope 60 ns, shaping time 200 ns

#### **BCID** percentages



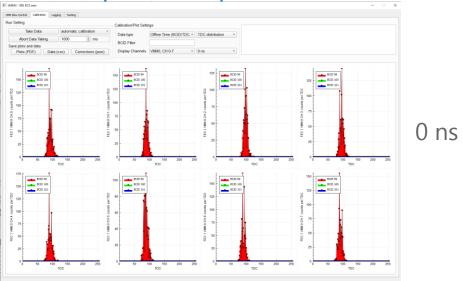
BCID percentage VMM0 (BCID 99-100)

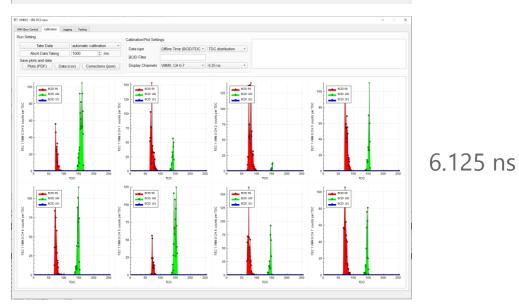


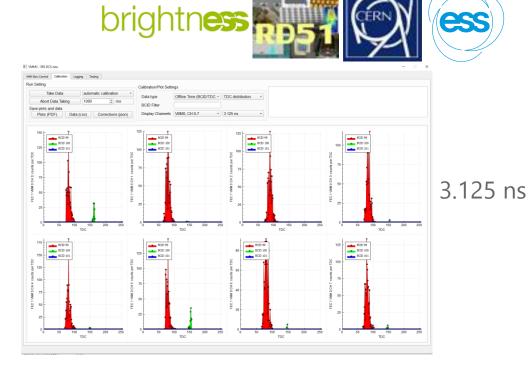


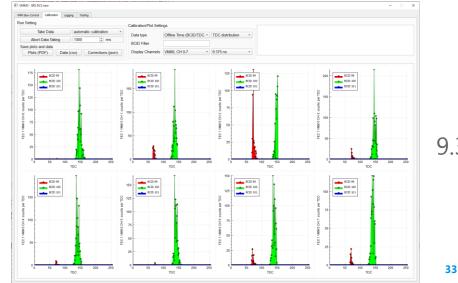
BCID percentage VMM3 (BCID 100-101)

#### TDC spectrum per BCID



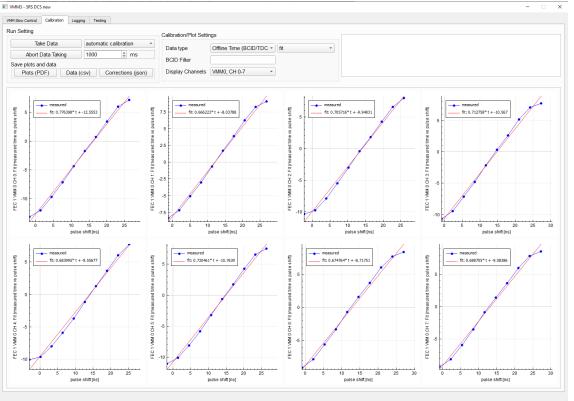




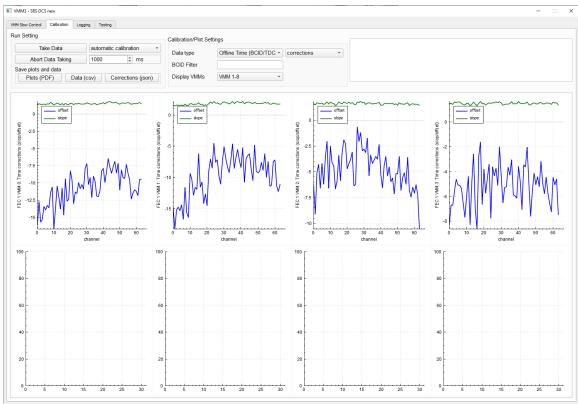


9.375ns

#### Fit and corrections







Fit to determine offset and slope corrections Plot per channel Offset and slope corrections Plot per VMM

#### To Do: compare different TAC slopes, shaping times, test whether corrections are stable over time

S-curve

threshold setting

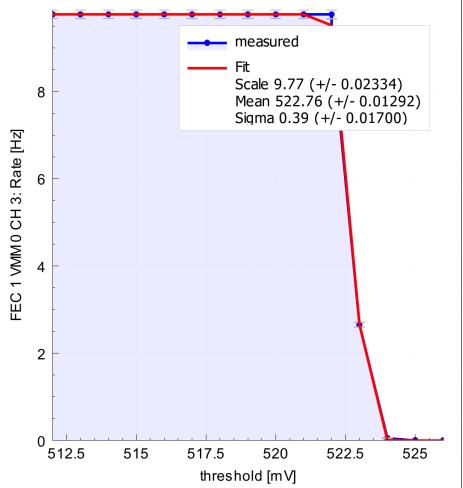
#### •Fit complementary error function to data (alglib: nonlinear regression using function values and gradient)

•Pulse all channels with internal test pulses

•Count the number of hits per channel per

•Shift the global threshold in steps of one DAC

- •On Windows, work only for a few channels at a
- time, otherwise rates do not reach 10 kHz
- •On Linux, works for a whole VMM (64 channels)
- Problem: A step of 1 DAC is equivalent to about 0.8 mV, this is very coarse for channels with low noise, fit not always good for steep drop in rates







### EUROPEAN SPALLATION SOURCE