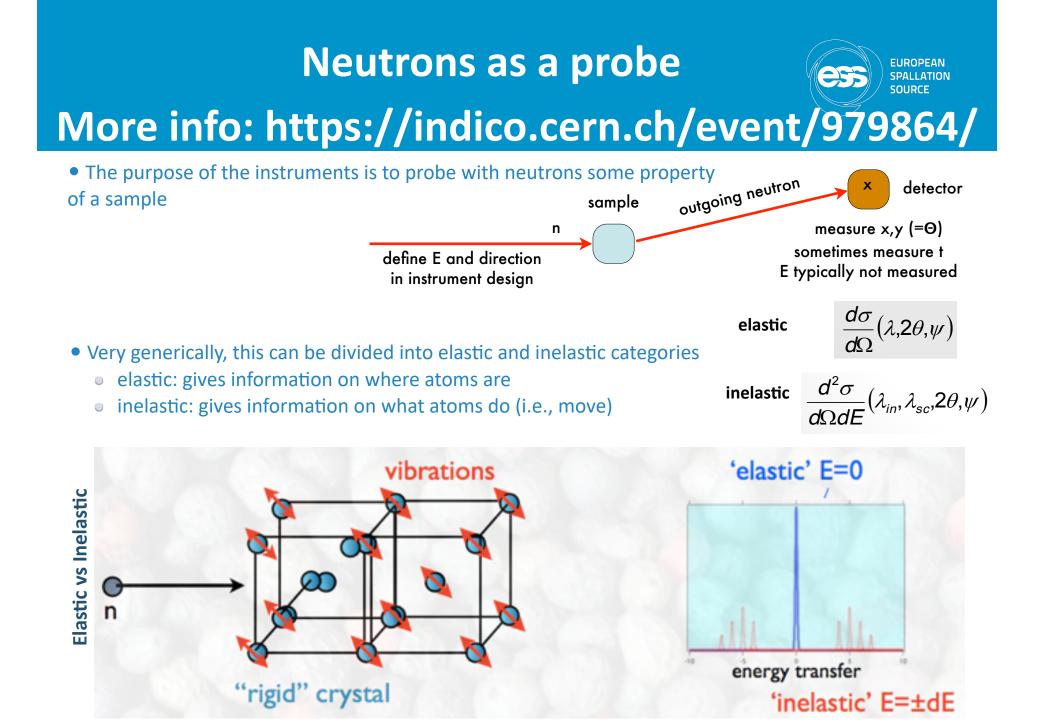


Detector Electronics at ESS for Neutron Scattering

RD51 Mini-Week WG 5 Meeting

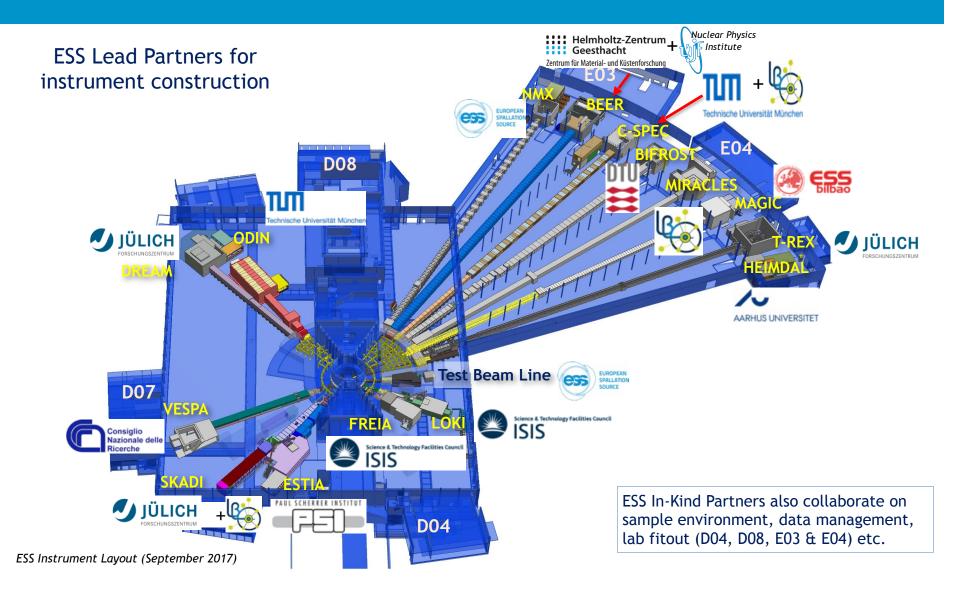
February 15th 2021

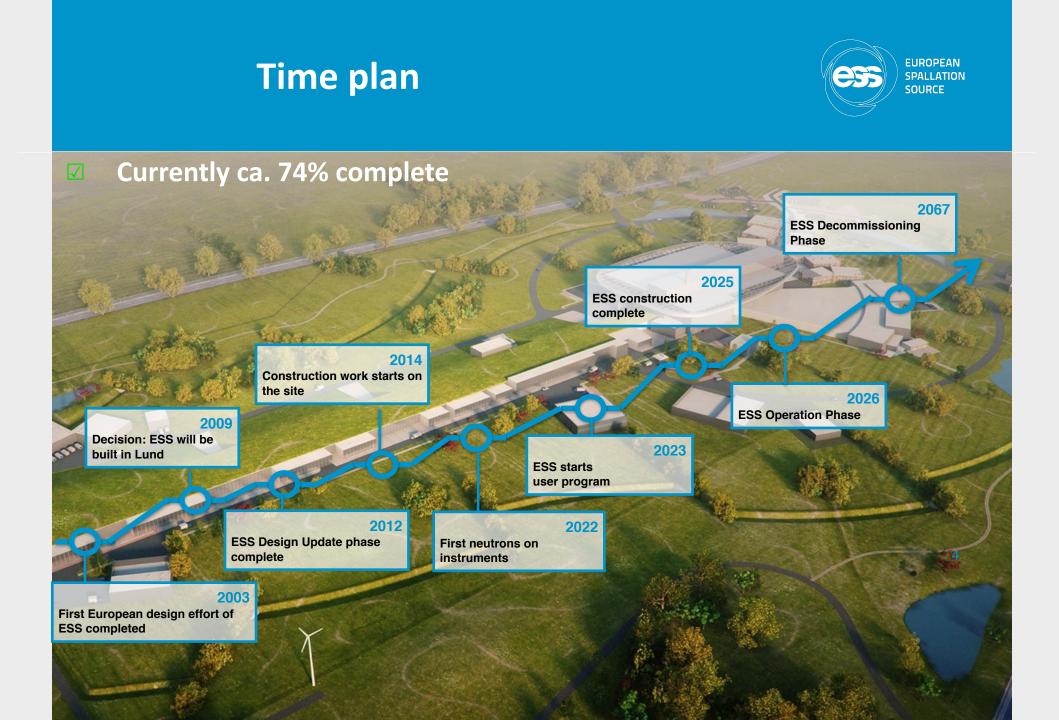
<u>Dorothea Pfeiffer (ESS/Milano-Bicocca/CERN)</u> Steven Alcock (ESS) Richard Hall-Wilton (ESS/Milano-Bicocca)



NSS Project scope: 15 neutron instruments + test beamline + support labs







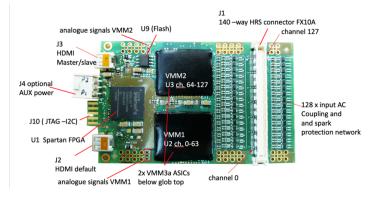


Front End Electronics: VMM3A ASIC



brightness

- VMM3a is the 4th version of an ASIC developed by Brookhaven National lab for the ATLAS New Small Wheel upgrade at CERN
- ASIC developed to read out Micro Pattern Gaseous detectors (MPGD)
- ASIC is high rate, sub-ns time resolution
- RD51 VMM3A hybrid common ESS-CERN project: successful integration of the VMM3a ASIC into the CERN Scalable Readout System (SRS) during BrightnESS
- 7.3 Mhits/s per VMM3a ASIC
- Per single VMM3a channel 4 Mhits/s
- Works well also for wire-based gaseous detectors

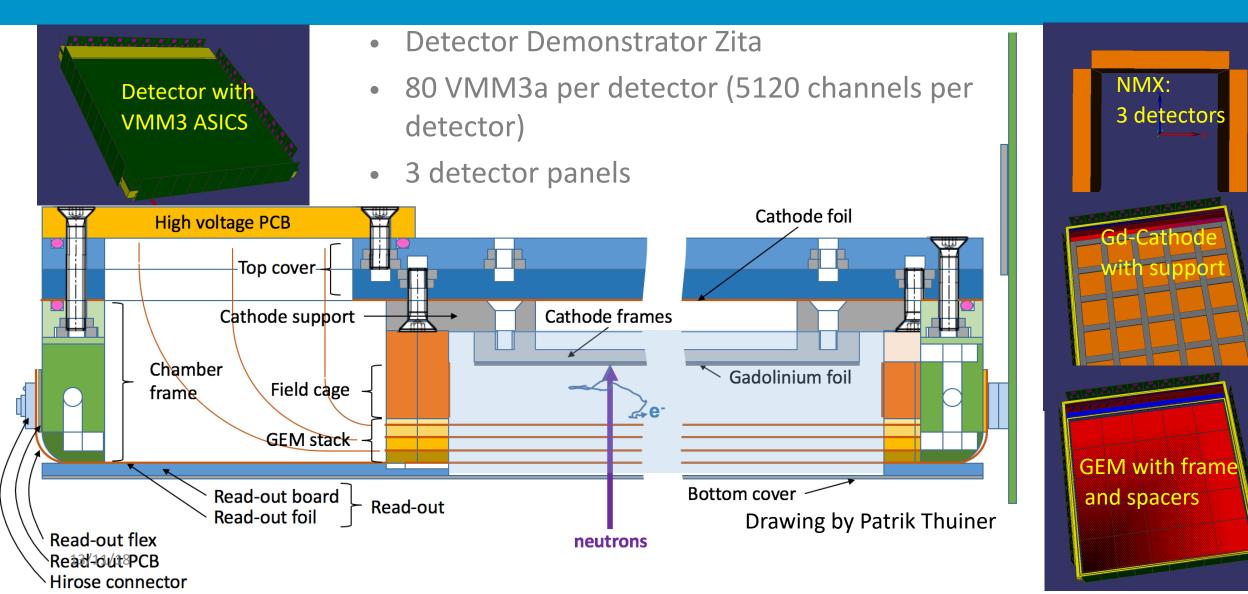


- First 57 available now
- 75% yield of highest quality hybrids
- Use initially for 5 instruments
 + testbeam line



VMM3a Gd-GEM for NMX

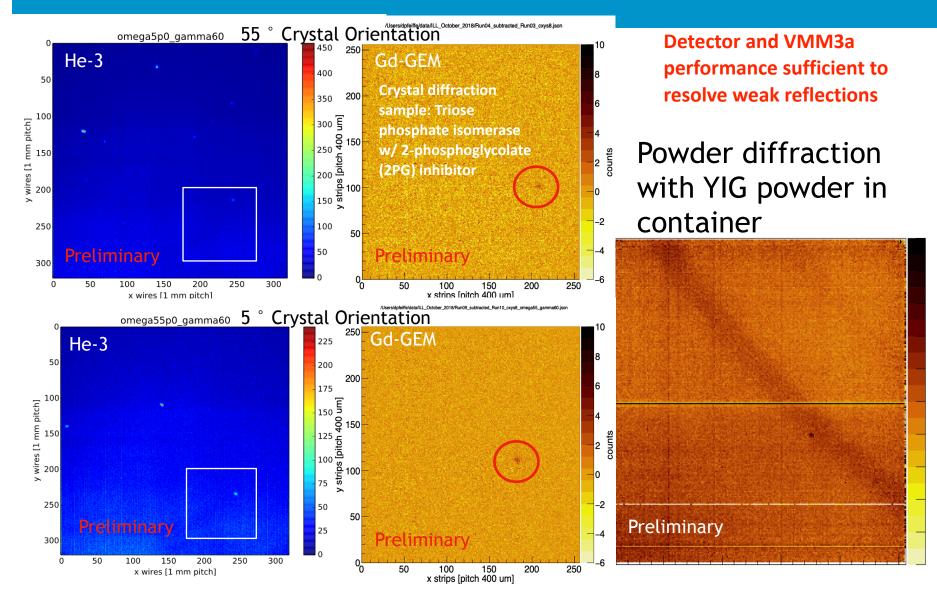






Gd-GEM Detector Demonstrator

EUROPEAN SPALLATION SOURCE



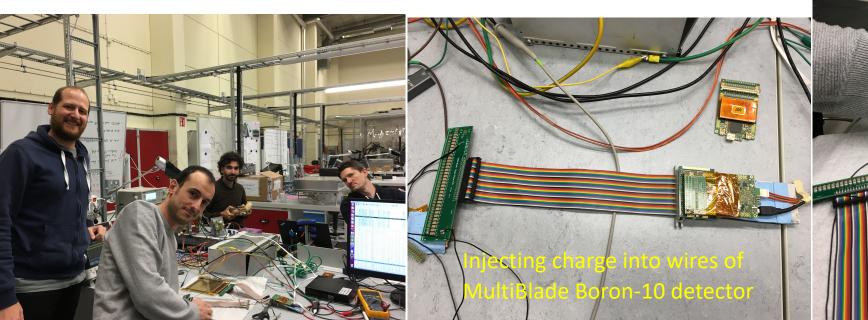
ratio

VMM3a Multiblade test at Utgard December 2018



EUROPEAN SPALLATION SOURCE

- Successful test of VMM3a hybrid with MB
- MB: Charge injection into:
 - Wires (negative polarity, AC coupled)
 - strips (positive polarity, DC coupled)
- Successfully read out with VMM3a via analog monitoring output and digital data in continuous mode
- Gain 1 mV/fC , 200 ns shaping time

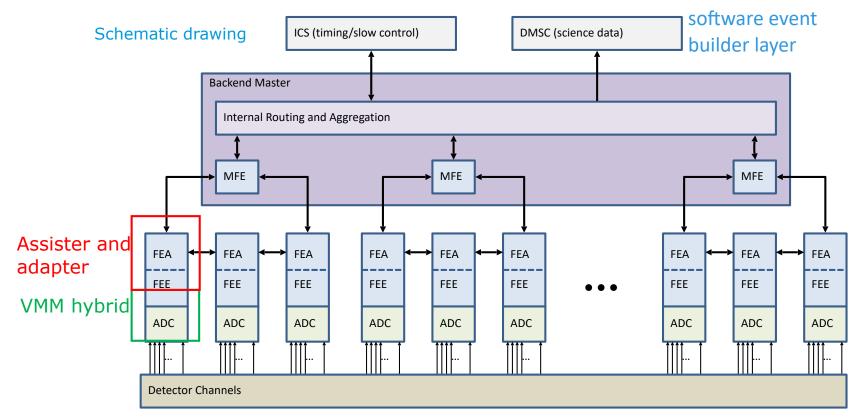




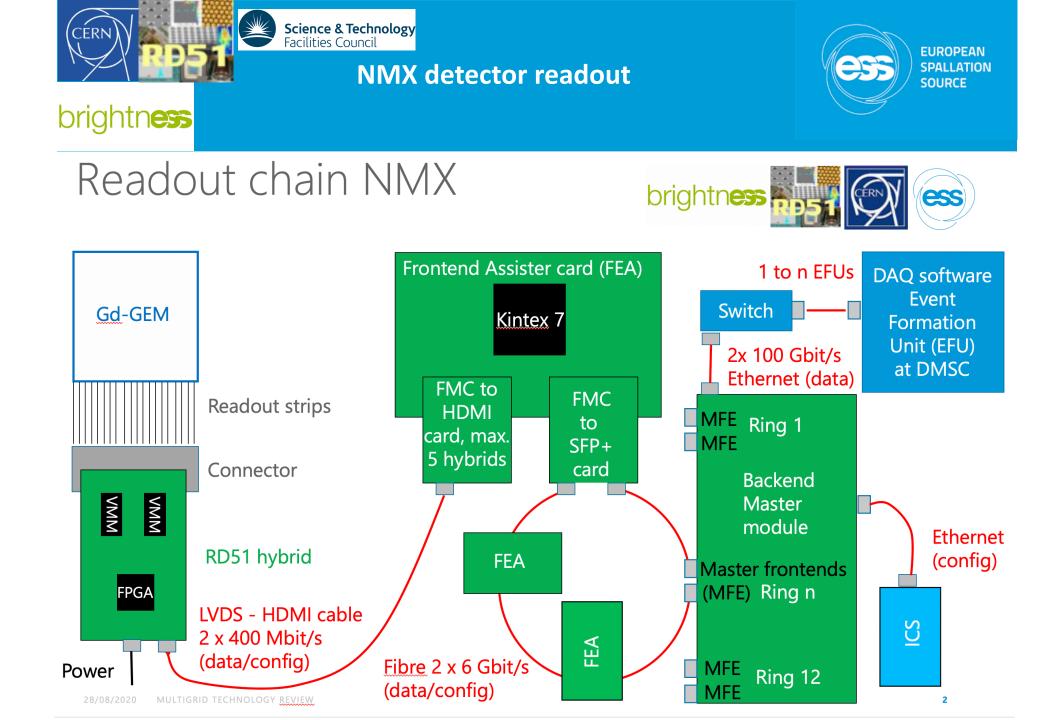
Detector Electronics



- Typical neutron instrument today maximum 100s of electronics channels
- Instruments at ESS > 10k electronics channels



Readout Architecture is described in BrightnESS Deliverable D4.1: https://dx.doi.org/10.17199/BRIGHTNESS.D4.1

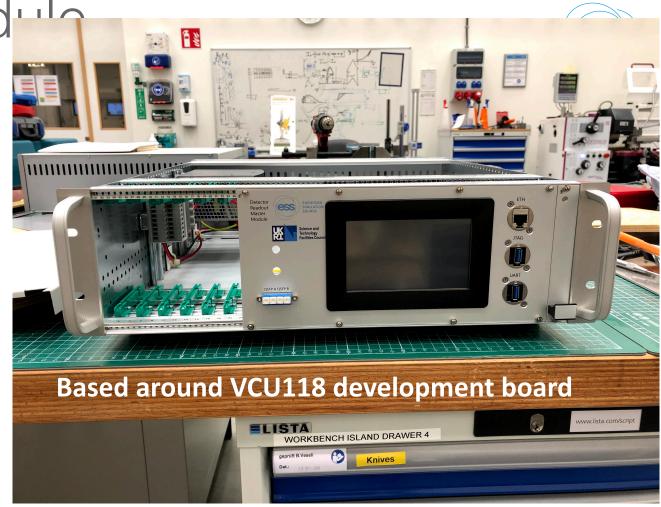


Hardware: Master Modula

Back end electronics (ESS/STFC)

Final Back End Electronics crates being assembled - 5(+1) Master Module readout crates as prototypes for real items





Next:

Integration of front end electronics for instruments Stress testing for 3-4 months Production for instruments by end 2021

Timing distribution in rings

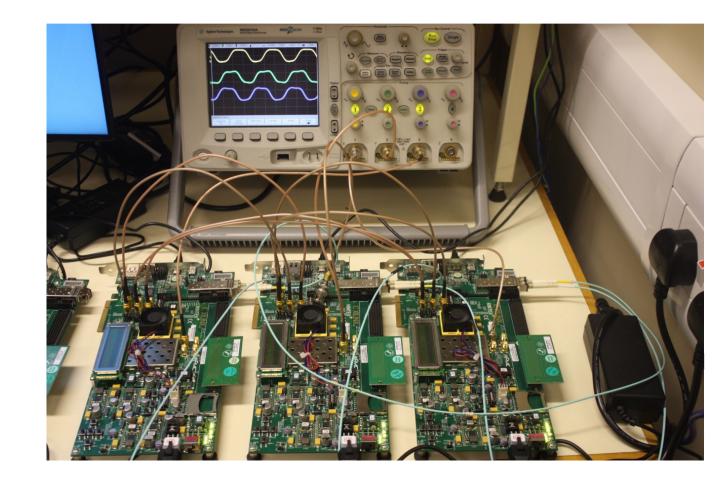




EUROPEAN SPALLATION SOURCE

- Front ends (FEA/FEE) connected to Master (MFE) via 8b/10b encoded SFP+ links.
- ESS clock used to generate these links

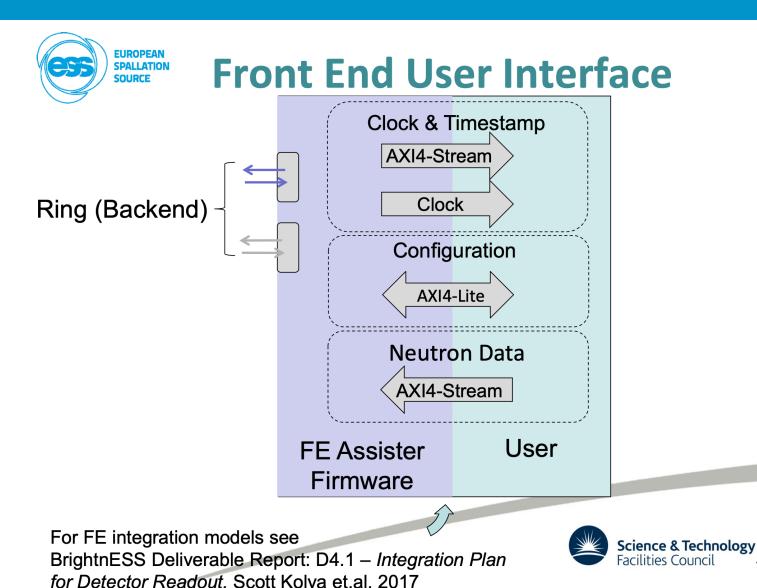
 can be recovered and forwarded by each front end (similar concept to Synchronous Ethernet).
- The ESS timestamp can therefore be forwarded to all the front ends, forming a single distributed synchronous system.



FE user interface



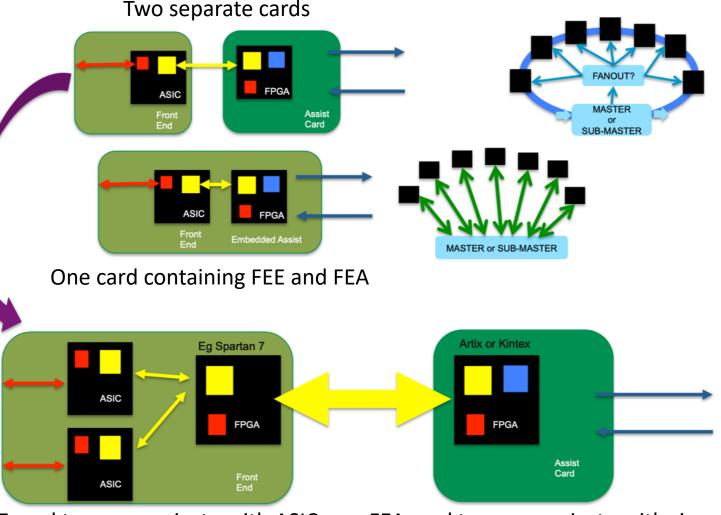
- FEA (front end assister) firmware communicates with the ring/backend
- FEE (front end user firmware) communicates with frontend ASIC like VMM3a or ADC
- FEA and FEE part of firmware communicate via AXI4 streams



Frontend (FEE) and assister (FEA): hardware and firmware modules



- Frontend FEE with firmware communicating with ASIC
- Frontend assister FEA with firmware to communicate with ring
- Could be in one FPGA and one card, or two FPGAs and two cards
- Advantages for two card solution: RD51 hybrid already exists, form factor of FEE card can stay small, heat dissipated on FEA card away from FEE



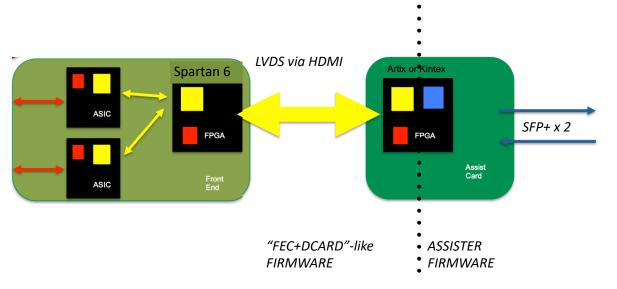
FEE card to communicate with ASIC

FEA card to communicate with ring

Step 1 (existing RD51 hybrid with Spartan6): Improve hybrid firmware, develop assister firmware

Start immediately

- Use existing RD51 VMM3a hybrid with Spartan 6
- RD51 hybrid firmware objectives:
 - Support high rate operations
 - Structure, clean up and document
- Use FPGA development board as assister platform
- Develop firmware for assister Artix7 FPGA



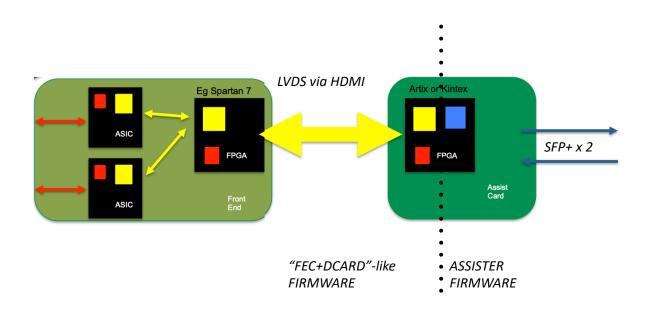


Step 1b (use dedicated assister hardware):



Within the next six months

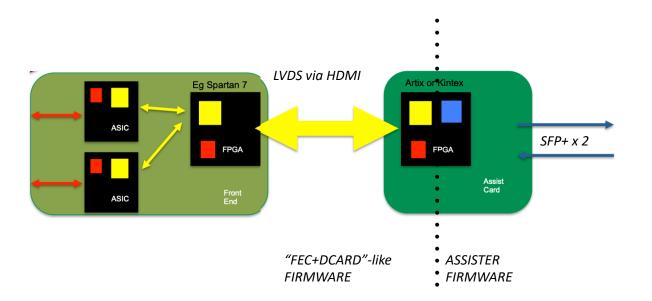
- Use dedicated assister hardware
- But ... we probably won't do this at least initially
 - Happy with KC705 development board as the assister so far ...



Step 1c (upgrade RD51 hybrid with Spartan7 or Artix7):

More longterm

- Explore options to upgrade RD51 hybrid to use Series 7 FPGA
- Believe that prototype hybrid design modified by Alex exists
- We are very interested in this for future production
- Port firmware to Series 7 FPGA
- ESS is happy to fund this port / do it ourselves: discussions ongoing





ESS VMM3a status



- Received 46 hybrids from 2020A production run
- Just received 50 hybrids from 2020B production run
- Use outcome to determine yields and quality
- Quality Yield: 70-80% hybrids perfect according to our QA metrics
- Lower quality chips can be used for some purposes.

- 54 hybrids/wafer maximum
- Understand that 50 hybrids/wafer is Hans/Alex's recommendation
- Therefore we have decided that we will count on 32 perfect hybrids/wafer
- We have assumed a 64% yield and hope to be pleasantly surprised.
- We want to order enough wafers/hybrids that we do not have to come back to top up in coming years.

ESS VMM3a expected numbers



Total Requirements:

• Known needs today:

Instrument	Initial Scope	Full Scope	Future Upgrade	Total (num of hybrids)
ESTIA	48	0	48	96
AMOR	6	0	0	6
CREMLINPlus	6	0	0	6
FREIA	32	0	0	32
CSPEC	108	54	48	210
TREX	48	72	0	120
NMX	120	0	0	120
Total	368	126	96	<u>590</u>

Wafer Quantites



- We assume that we will need all the existing wafers for R&D and integration activities
- We need ca. 600 perfect quality hybrids.
- Ca. 19 wafers
- Therefore, we want to order 25 wafers in 2021. i.e. 1 unit of an engineering run.
- Happy to modify this by a small number to help out RD51, if it helps the order process.
- We would like to make this order ASAP
- Delivery by EoY? Need to get started ASAP
- ESS happy to help Hans and RD51 with the technicalities of this order.
- Question: is there likely to a further wafer order in 2022?
- Worry: its really important to get going with this order. Last order took >1year ...
- Wafer storage needs thought ...





- We are interested in Series 7 hybrids for all our applications so that we are not supporting series 6 and 7 operationally
- We need ca. 600 perfect quality hybrids: That means ca. 1000 hybrids
- We would like to receive these by end 2022 or 2023Q2
- For the first production run of series 7 hybrids, want to order a moderate amount in case of modifications being needed
- Important for us to determine the expected production run schedule
- Indicative, assuming 2 production runs/year:

Production	2021	2022-A	2022-В	2023-A	Total
run					
Number of	100	300	300	300	1000
hybrids					

• Worry: again, its really important to get going with this order. Admin, finances, production take some time





- ESS has established that VMM3a works for wire chambers: VMM3a fulfills requirements for ESS detectors
- Frontend card is the collaboratively developed RD51 hybrid with Integration of RD51 hybrid into ESS readout
- Worry about VMM3a wafer production: need to start now
- Worry about timescale for next hybrid order: need to start now
- Its really important to get both 2021 orders and plan for 2022 production in place.
- Important to start now ...
- Needs thought: there maybe more than1 cooling solution needed
- We need to power our hybrids independently to HDMI cable