NEXT charge-integrating SiPM readout with SRS, status und future

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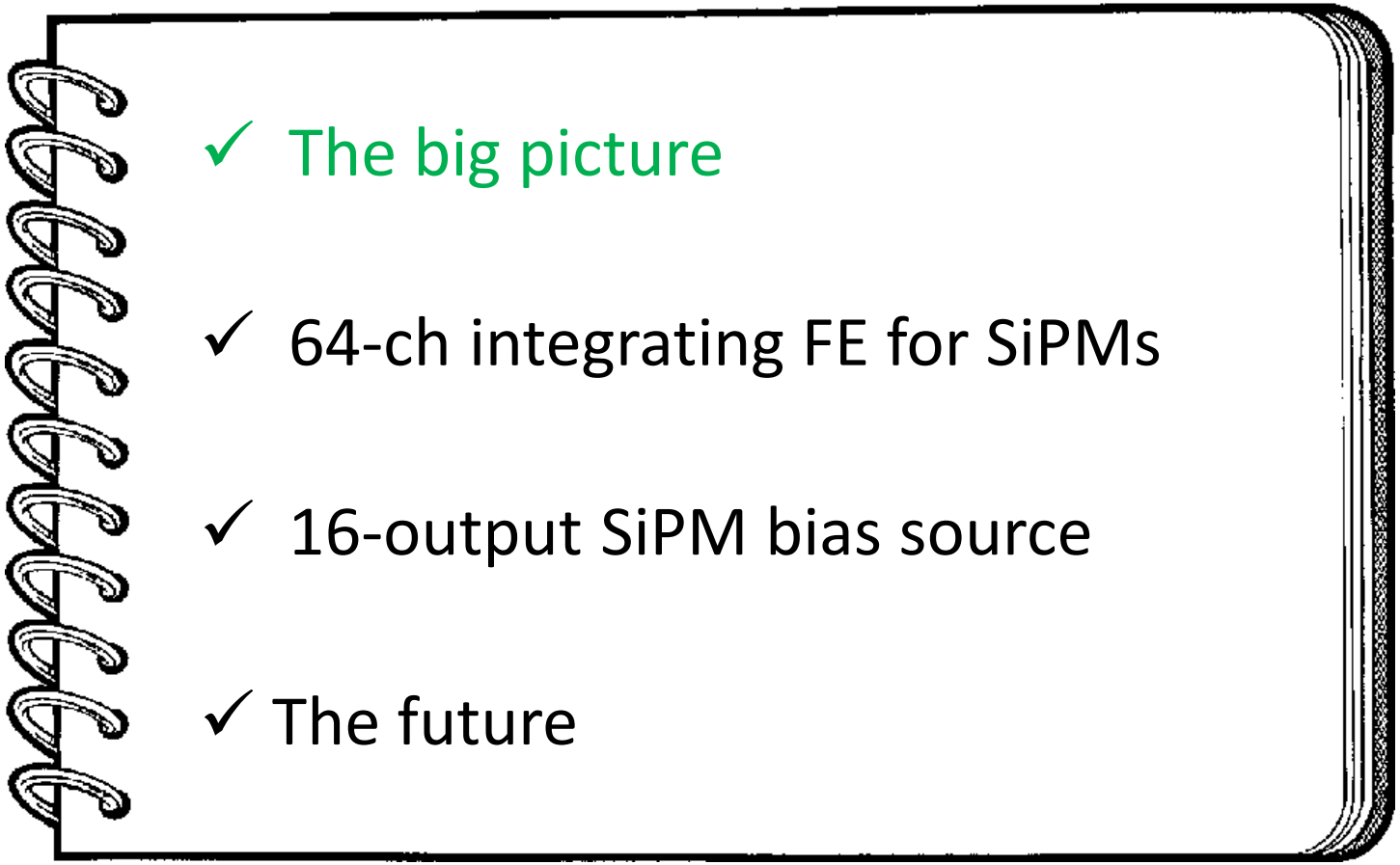
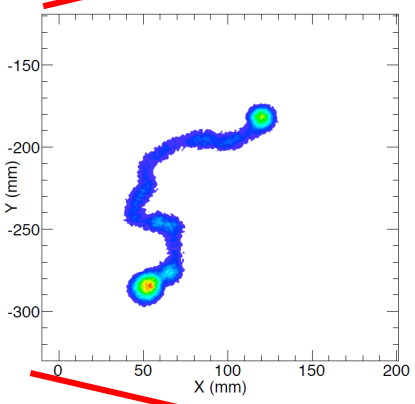
NEXT Collaboration

Outline

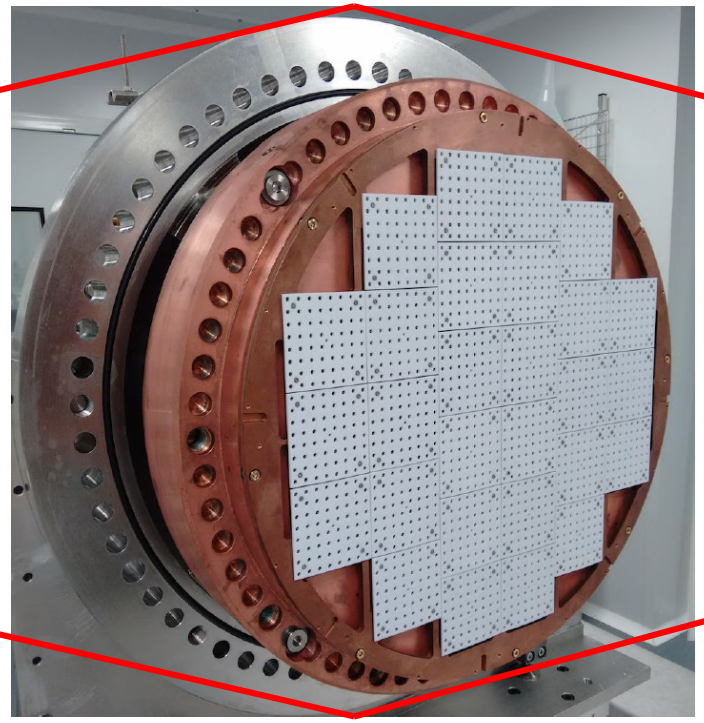


- ✓ The big picture
- ✓ 64-ch integrating FE for SiPMs
- ✓ 16-output SiPM bias source
- ✓ The future

The big picture



2ββ tracking in x,y,z
(i.e. x,y, time)

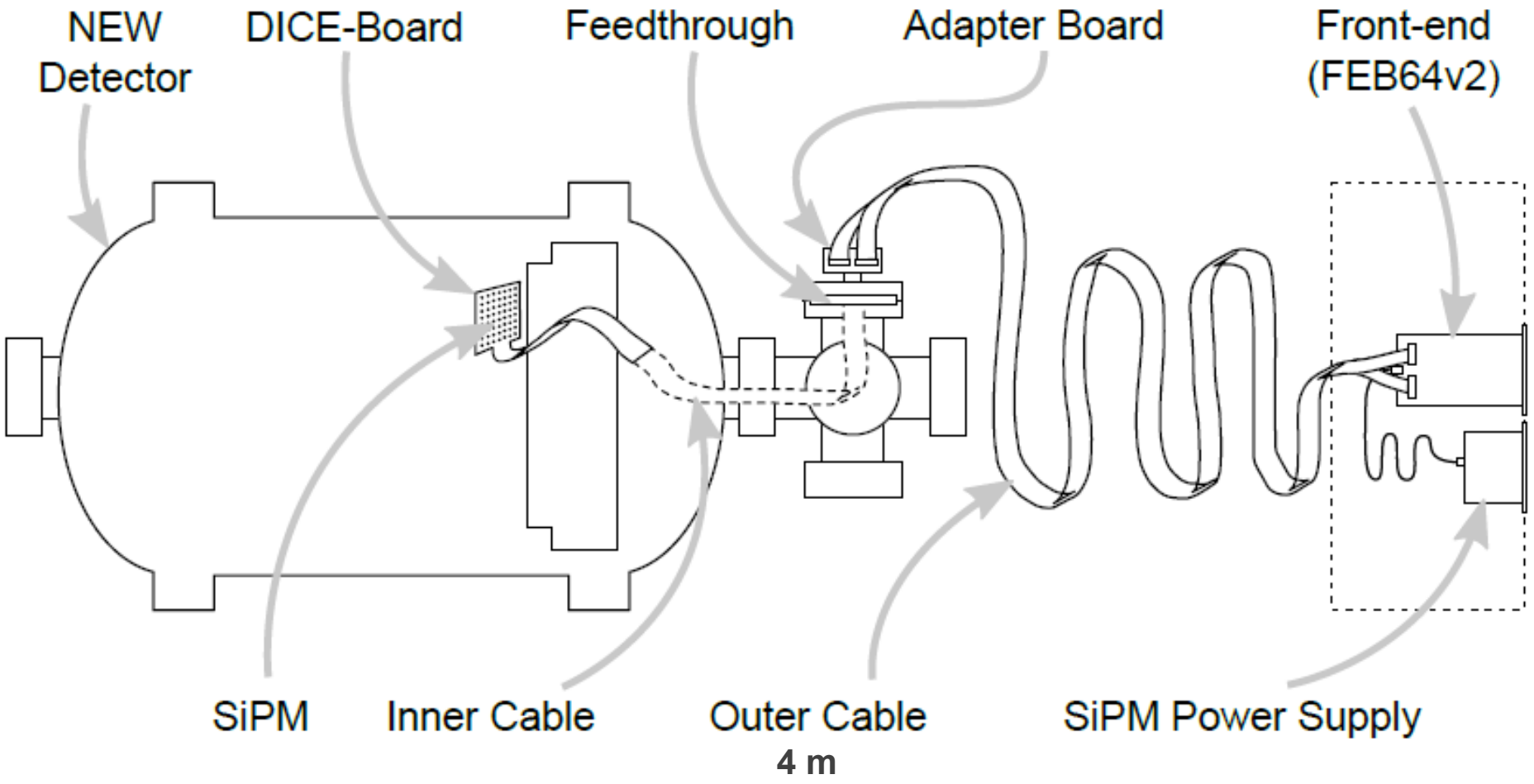


1800 SiPMs in 28 8x8 arrays
OnSemi MicroFC-10035-SMT

NEXT-NEW mid-sized gas Xe detector for 2ββ–0ν experiment

Design goal can be summarized as: “How many photons reach each SiPM each microsecond?”

The big picture



The big picture

Slow controls PC

PMT HV

DAQ PCs
running DATE

ATCA-SRS DAQ

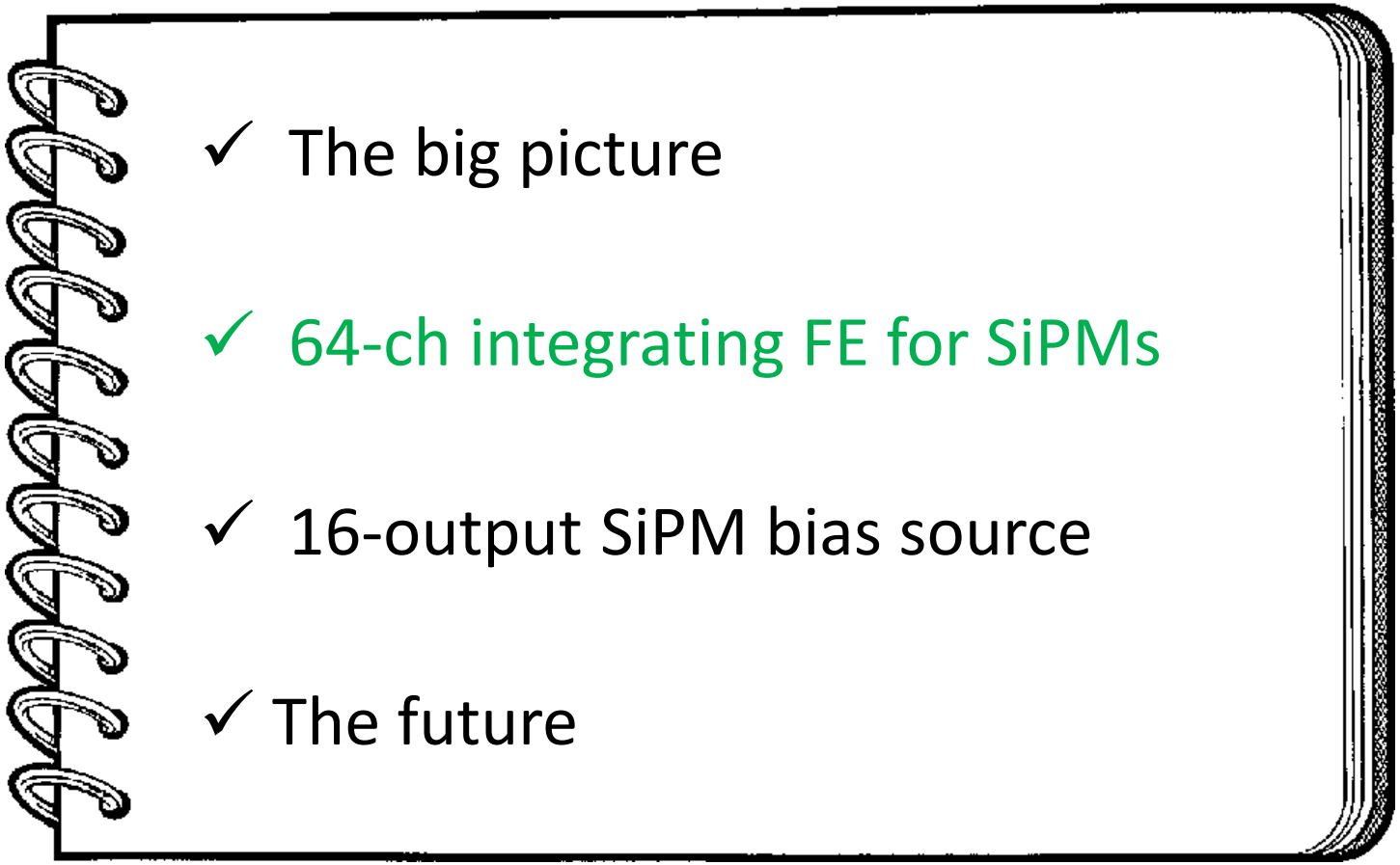
PMT FE
(not shown)

Power supplies for 28
SiPM FE boards

UPS

28 FE bords for 1792 SiPM ch
3 SiPM bias sources in 3 x 19”
3U crates

Outline



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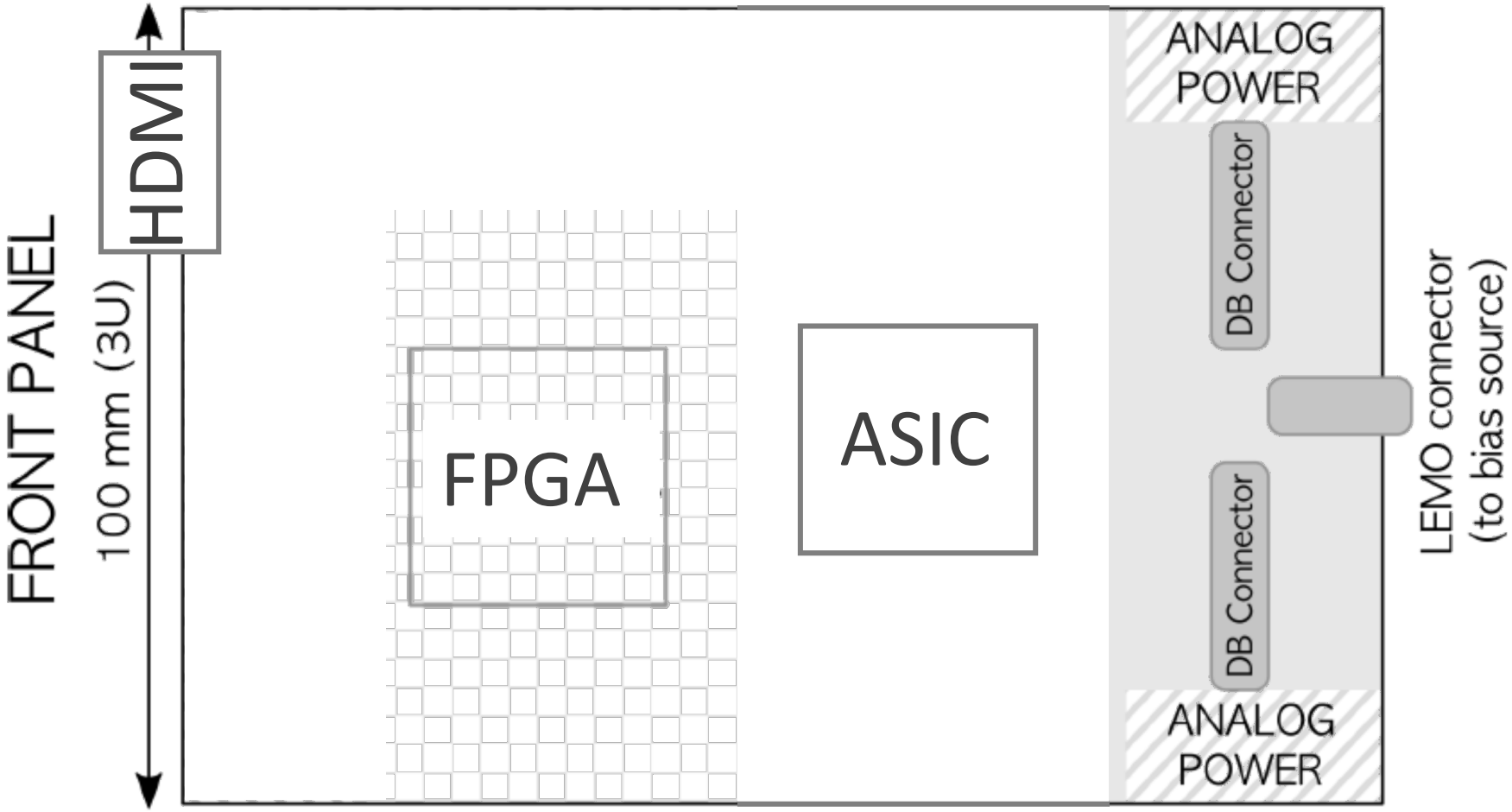
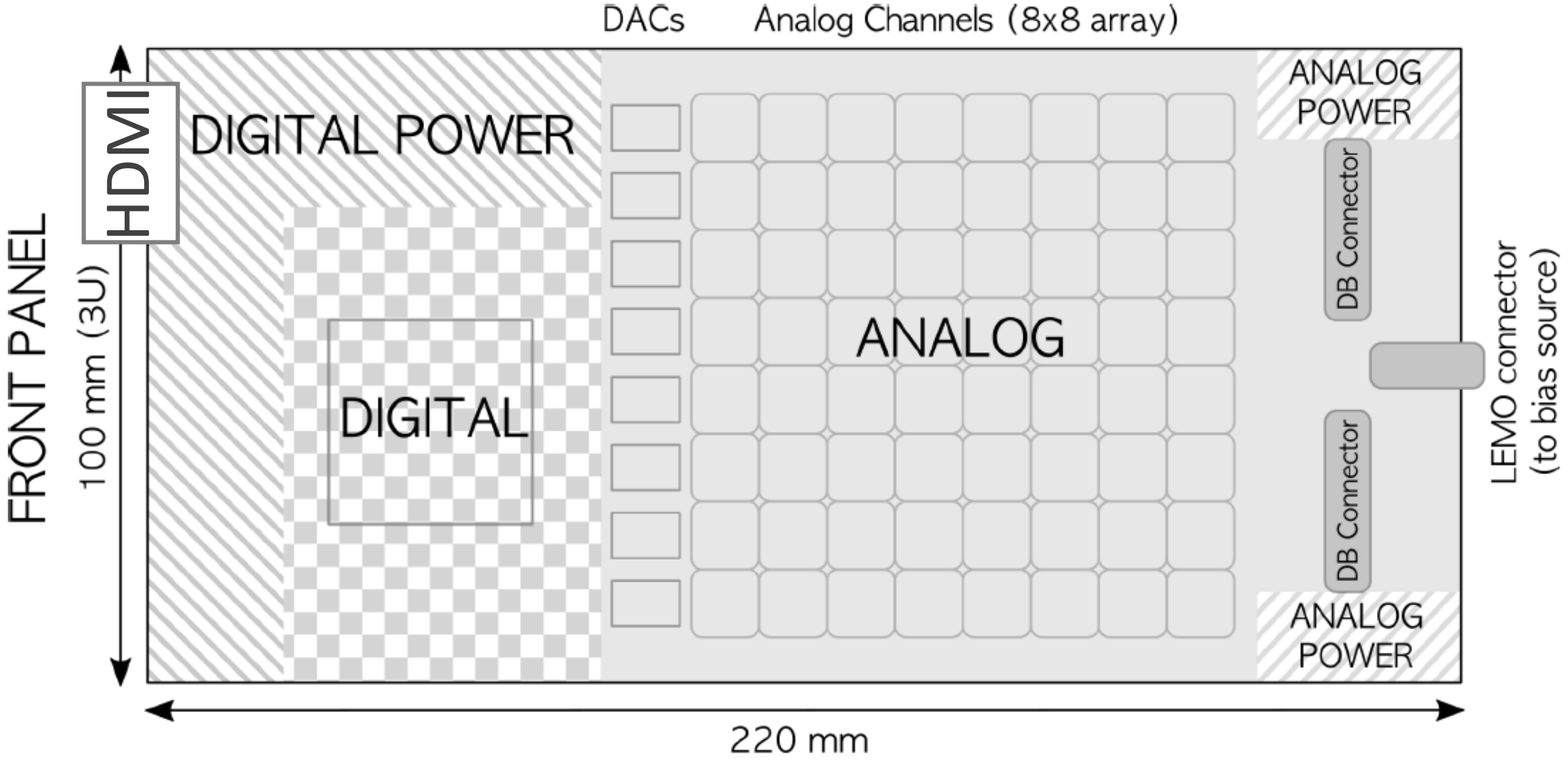
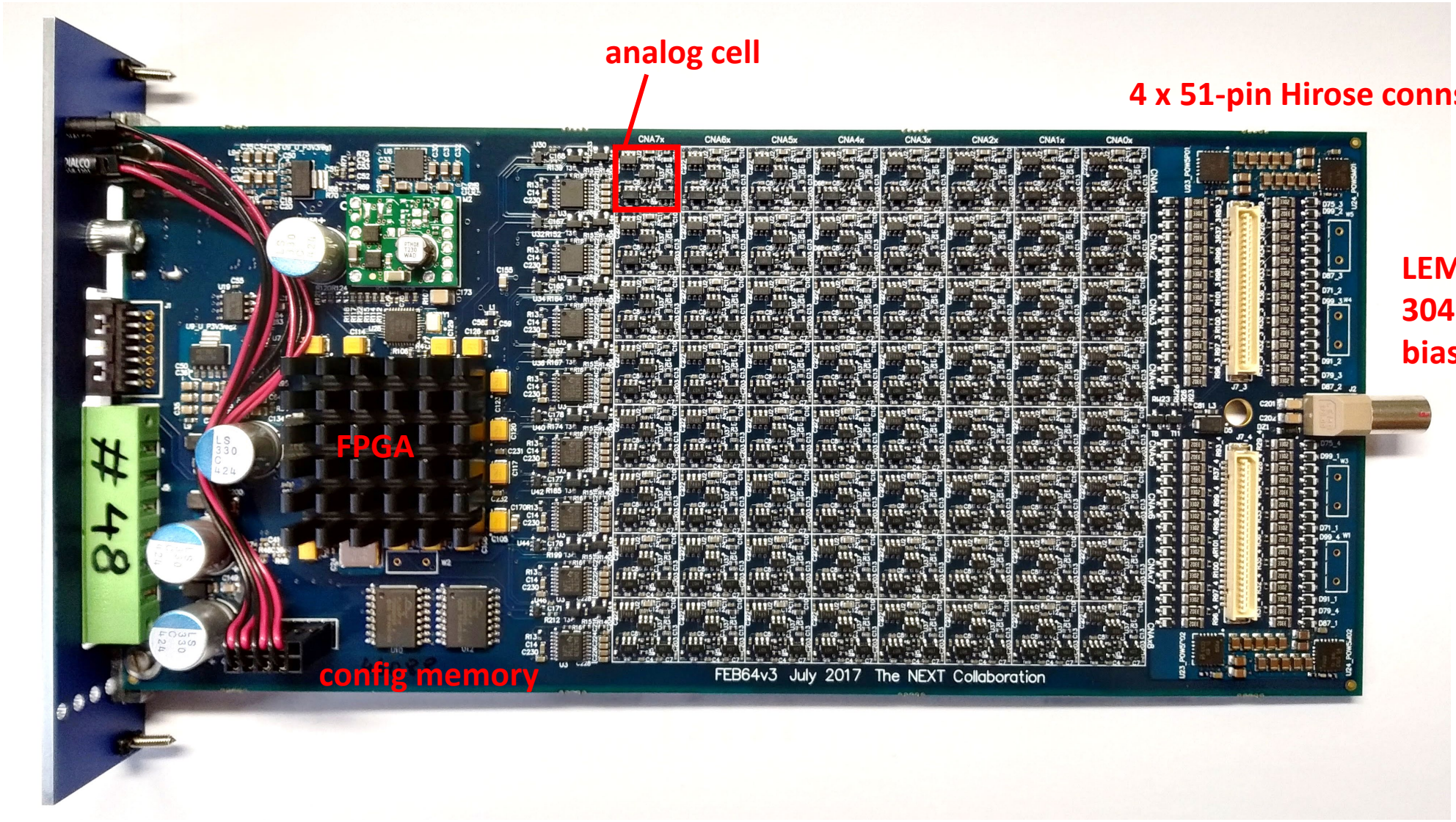
This is what you want: an integrating ASIC and a small FPGA interface



This is what you get when you cannot find the right ASIC: larger FPGA and 64 COTS analog cells



The FE board (v3) – 3U x 220 mm



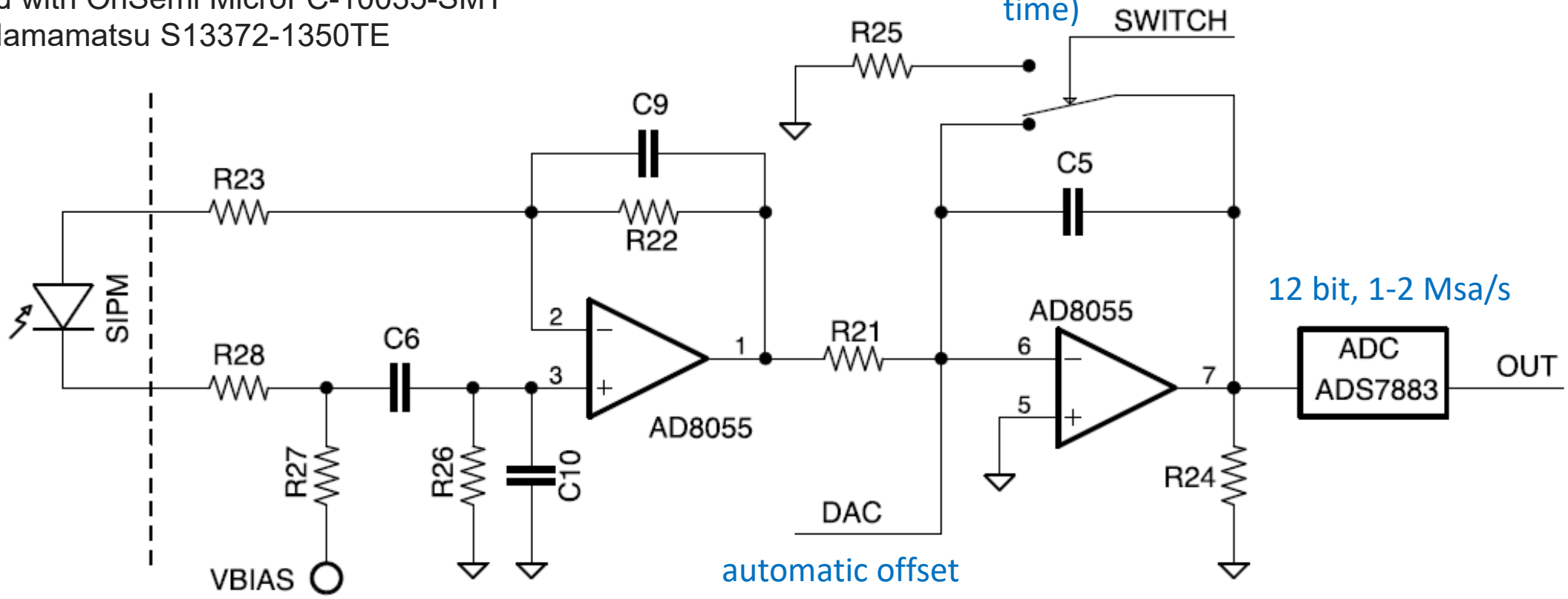
Each analog channel: amp + gated integrator + ADC

Our settings: 1 MHz operation (960 ns integration + 40 ns for C5 discharge)

Dynamic range: spe resolution, up to ~200 pe/μs with current gain

Tested with OnSemi MicroFC-10035-SMT and Hamamatsu S13372-1350TE

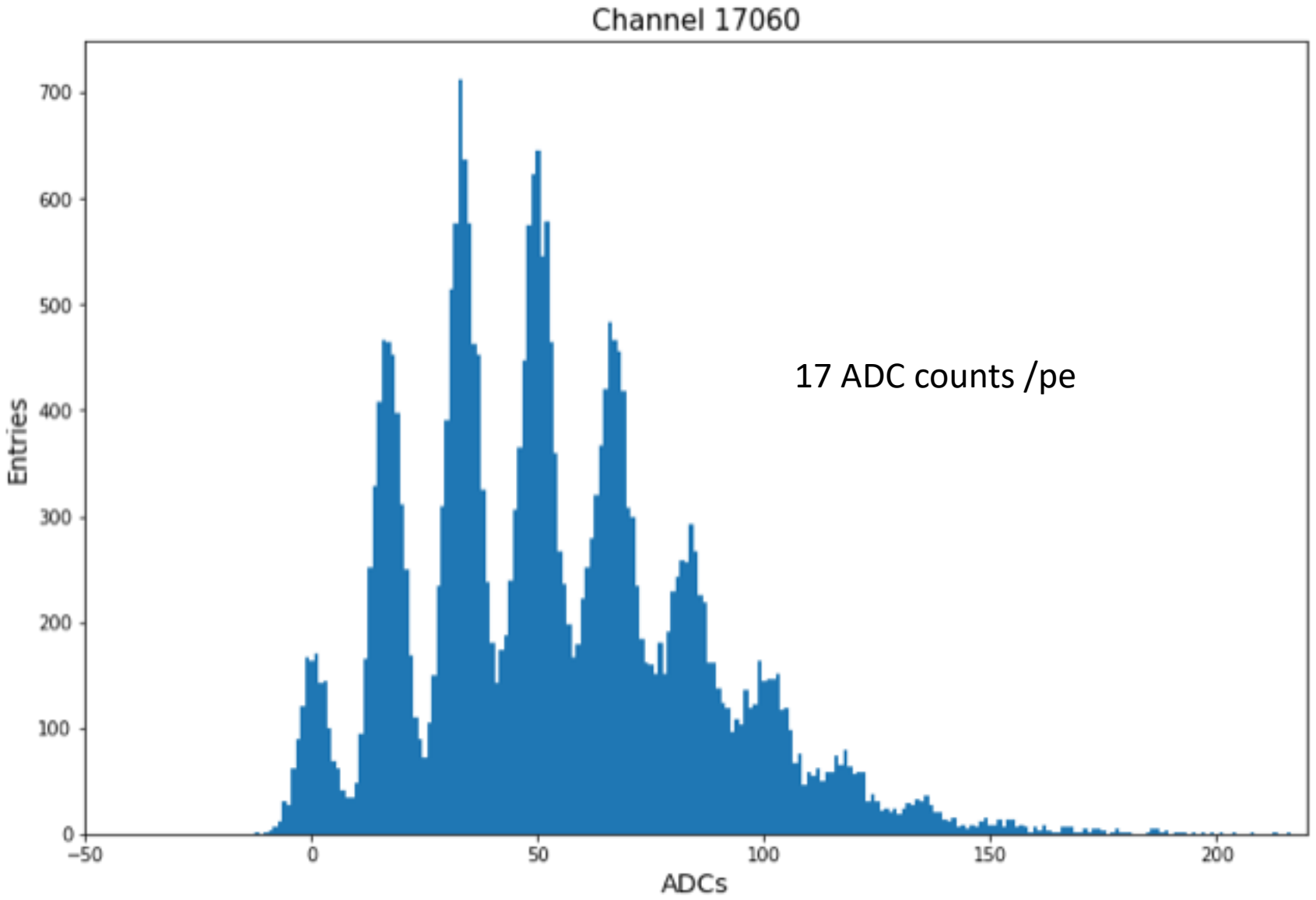
ADG719 FPGA-controlled switch (40 ns discharge time)



12 bit, 1-2 Msa/s

automatic offset compensation (FPGA)

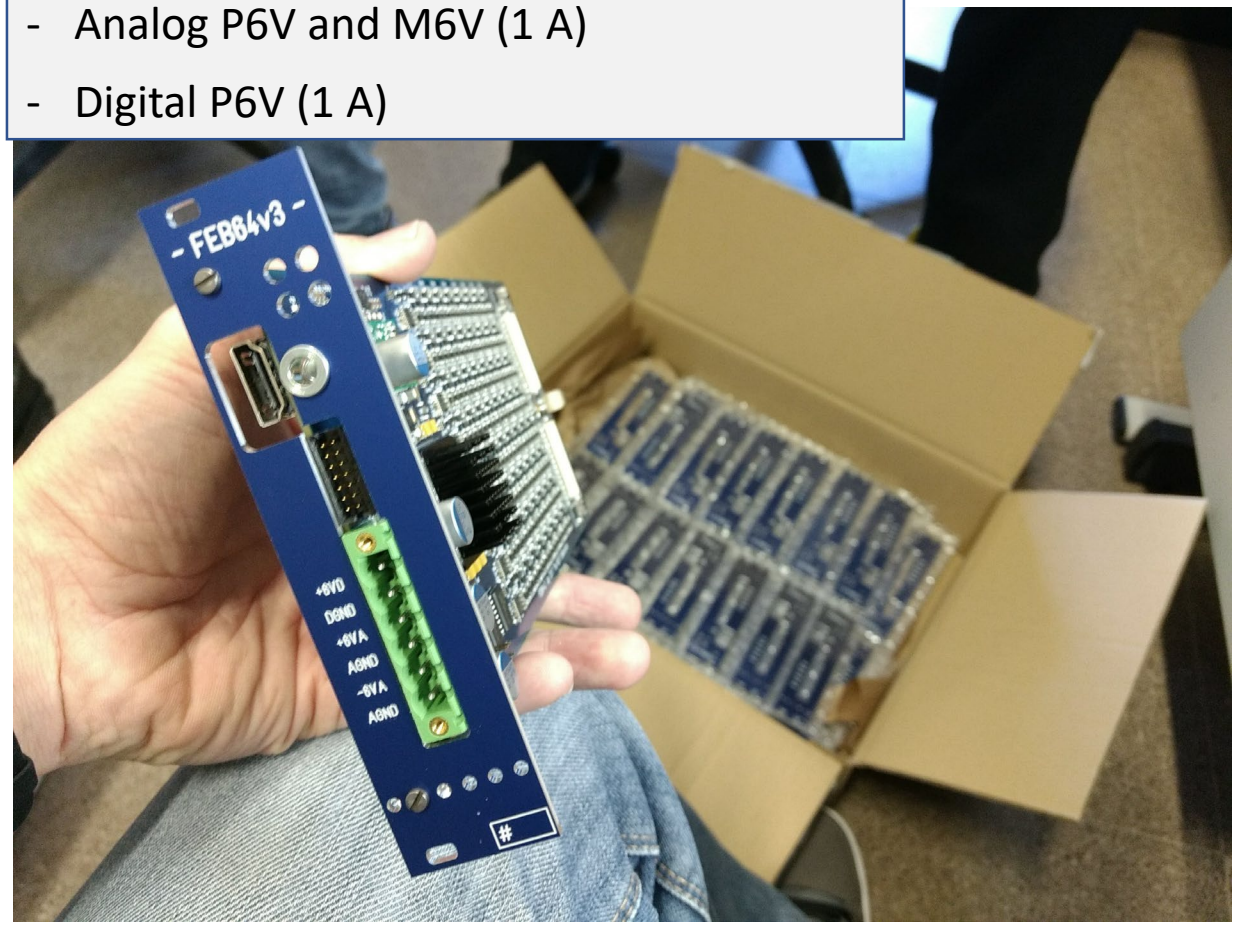
Performance – data from NEXT-NEW detector operation



The FE board (v3) front panel with HDMI lock

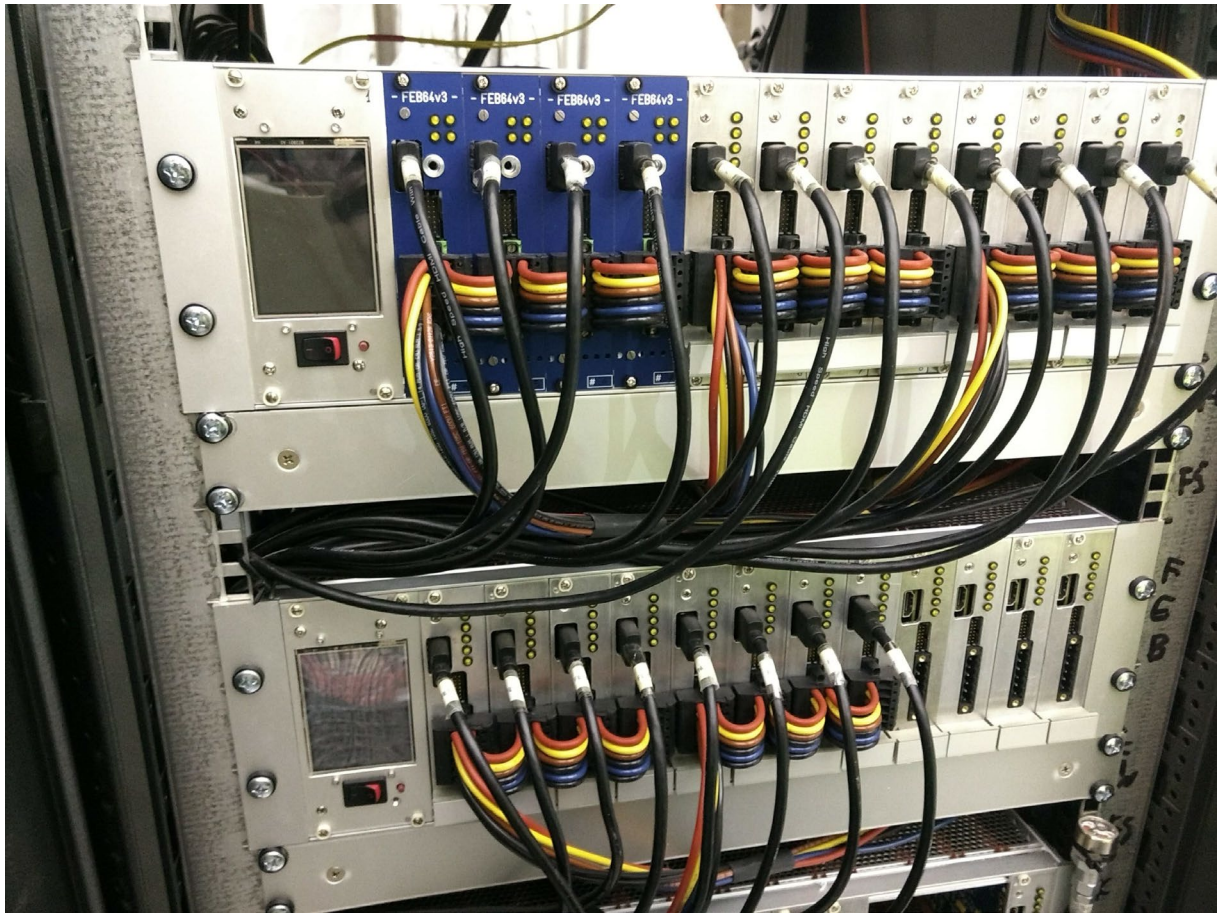
Power requirements (external power conn)

- Analog P6V and M6V (1 A)
- Digital P6V (1 A)



HDMI lock in the FEv3 front panel to avoid disconnections

4 FE boards share power wires (in Daisy chain) from the PS

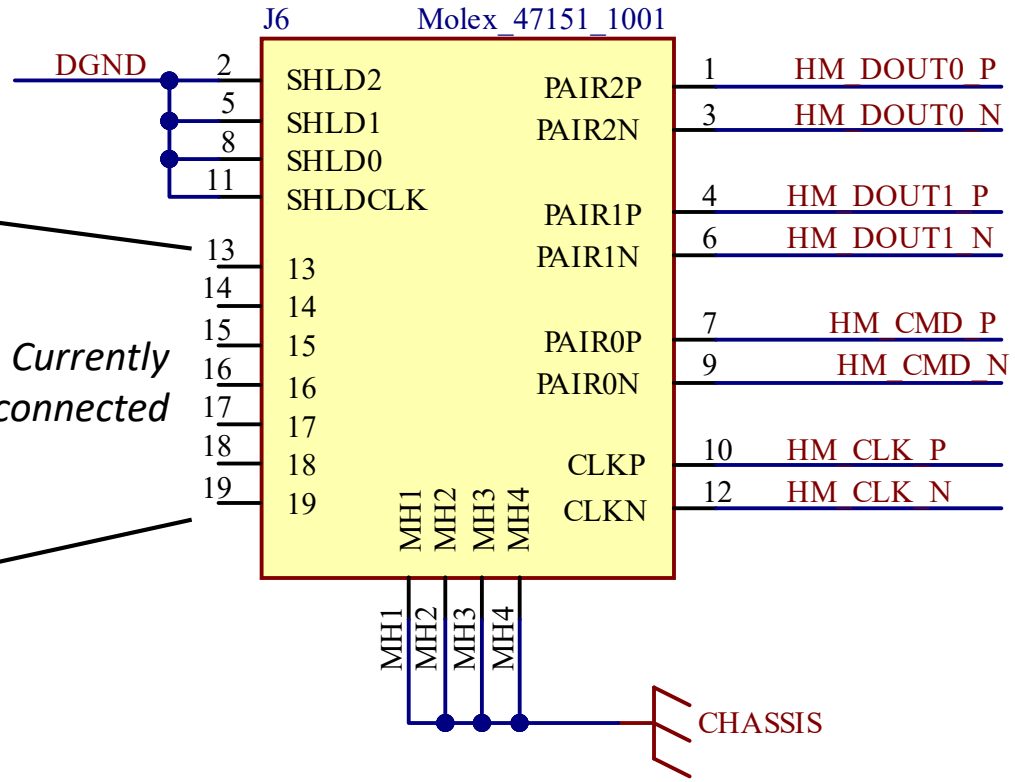


12 FE boards (768 SiPM ch) + 1 SiPM bias source in a 19” rack

SRS compliance: works with FECv6 and SRS-ATCA

Our FW differs from standard SRS

Also use 8b/10b but different data format



13: SRS M/S: can be connected to jumper

15: I2C SCL : can be connected to board

16: I2C SDA: can be connected to board

Currently unconnected

17: power GND: unused

18: P1 power : unused

14&19: P2 power pair : unused

SRS DATA-1M uplink ✓

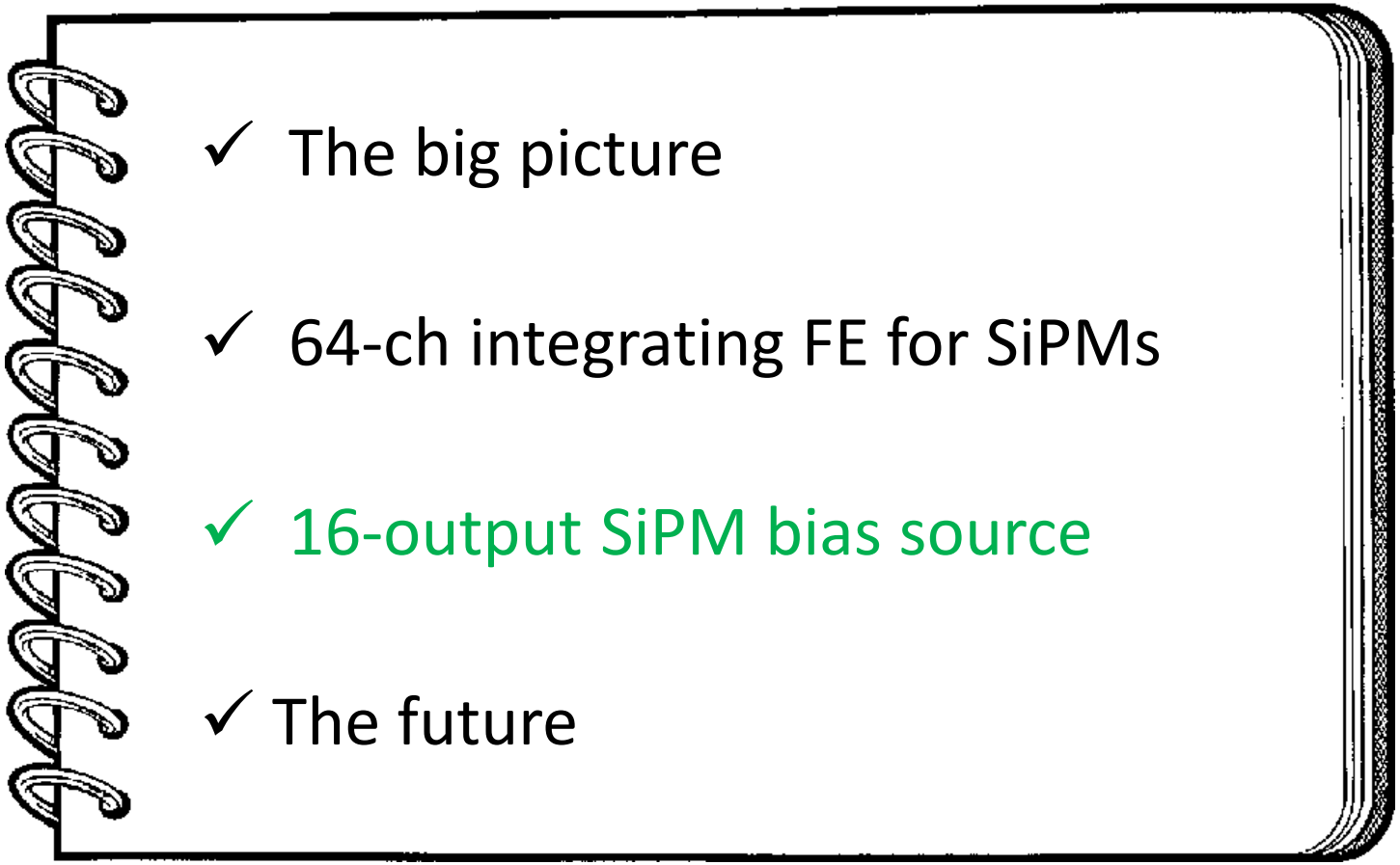
SRS DATA-2M uplink ✓

SRS controls downlink ✓

SRS CLK downlink ✓

We use 100 MHz instead of 40 MHz, need to change PLL settings

Outline



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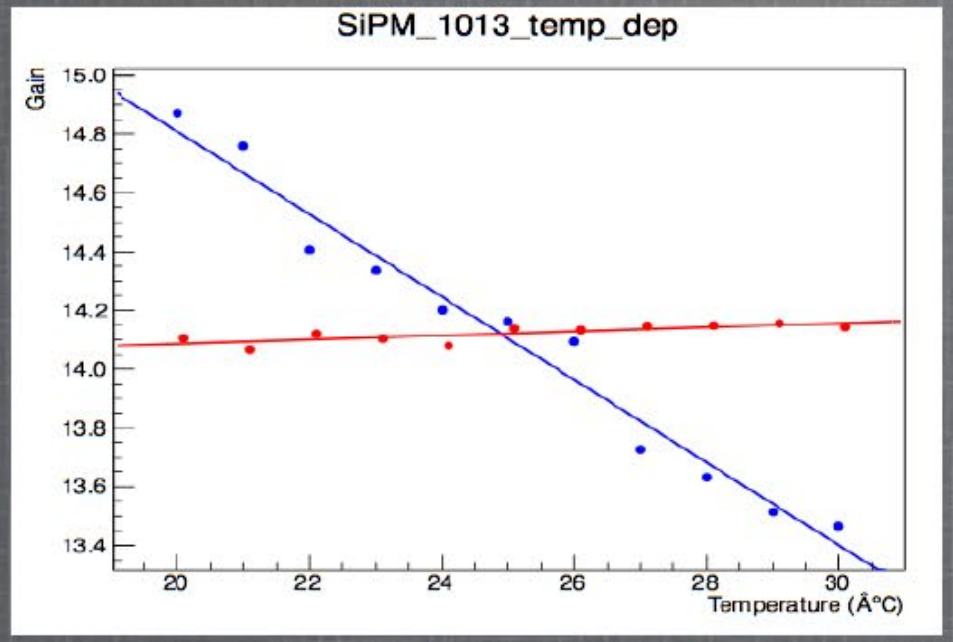
NEXT SiPM bias unit

- 16 LEMO outputs
- Up to 85 V and 5 mA per oputput
- Noise < 4 mV_{pp}, current monitoring (12 µA error)
- Controlled rise and fall slopes
- Overcurrent & overvoltage protection
- Automatic voltaje compensation (remote SiPM temperature monitorization) for stable SiPM gain

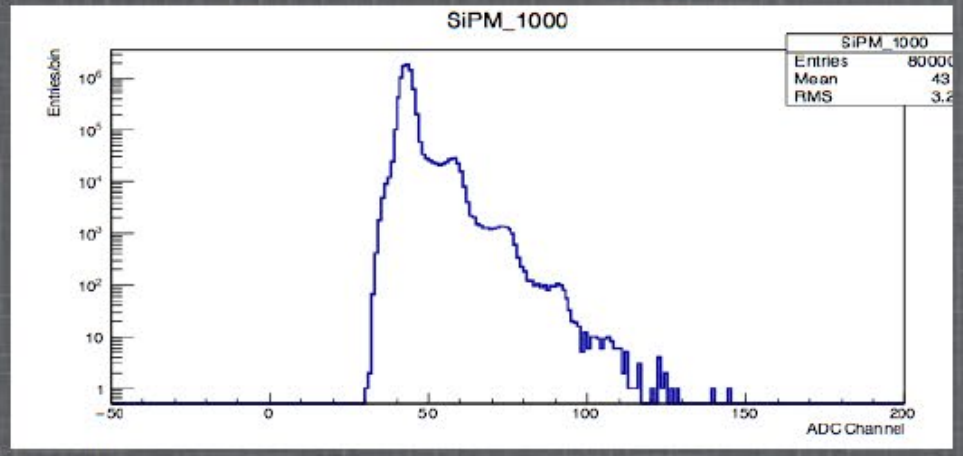
- 3.2” touch screen for manual operation
- Ethernet interface for slow controls, SSH protocol
- LabView SubVI available

- 12 V power input (5 W typ, 29 W max)
- FW in USB memory (replaced with SD in current versión for enhanced reliability)

NEXT SiPM bias unit (from IWORID16 presentation)



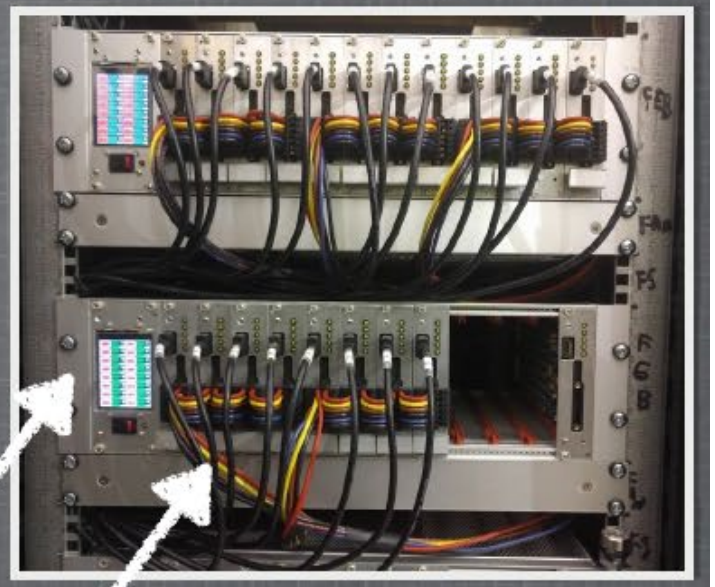
Gain vs Temperature without compensation (Blue) and with compensation of 22mV/ºC (red).



SiPM Dark noise spectrum

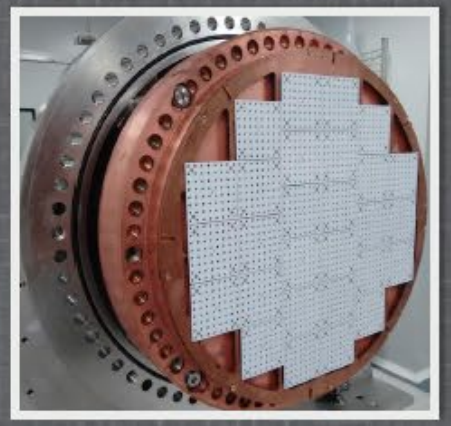
SiPM GAIN STABILIZATION

- System capable of stabilizing the temperature.
- Temperature sweep 15-35ºC.
- SiPMs gain stabilization of 0,5% (11,56% without compensation).



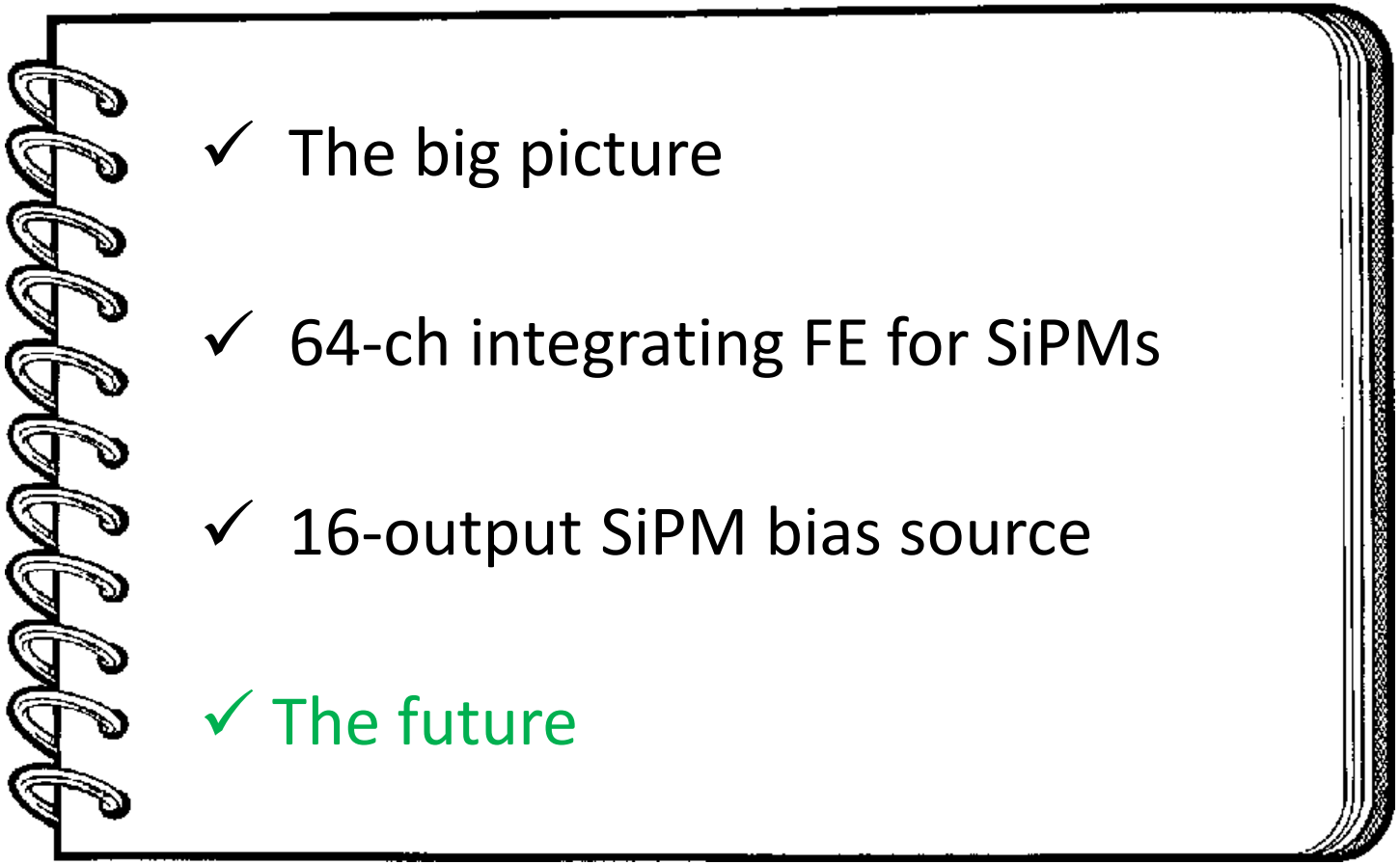
One 16CH Bias Source powers 16x64 SiPMs channels.

FEE electronics for the 1.8-kchannels SiPM tracking Plane in the NEW Detector.



With 3 SiPMs Bias Sources, ~1800 SiPMs are supplied.

Outline



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If there’s enough interest…

- In the FE board:
  - Let’s discuss the possibility to ugrade the FPGA: XC6VLX195T-1FFG784C now.
    It might be wise to move to a modern device with CERN step prices!
  - We can discuss in more detail your requirements. We have a sound and long-term (several years) tested system, including slow controls and DAQ
- In the bias source: let’s dicuss how to organize production

In 2-3 years from now…

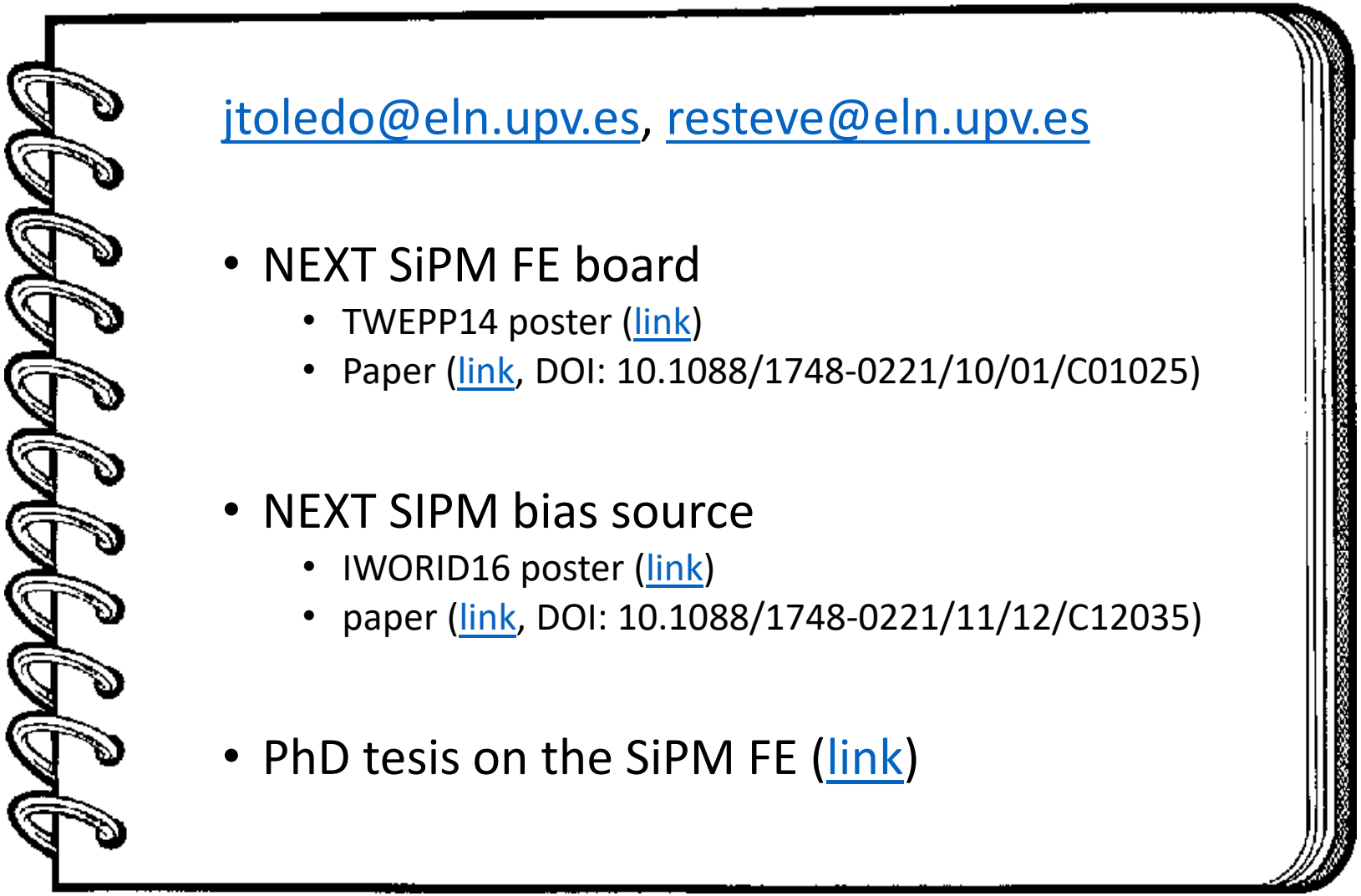
- NEXT-100 upgrade plans suggest we should move FE into the detector

- So, we need a much more compact solution:

  - ASIC?
  - Minimalistic shaping&amp + ADC?
  - Still, same requirements: microsecond-scale charge integration
  - Also, radiopurity requireements

Not an easy challenge!

Reference documents & contact info



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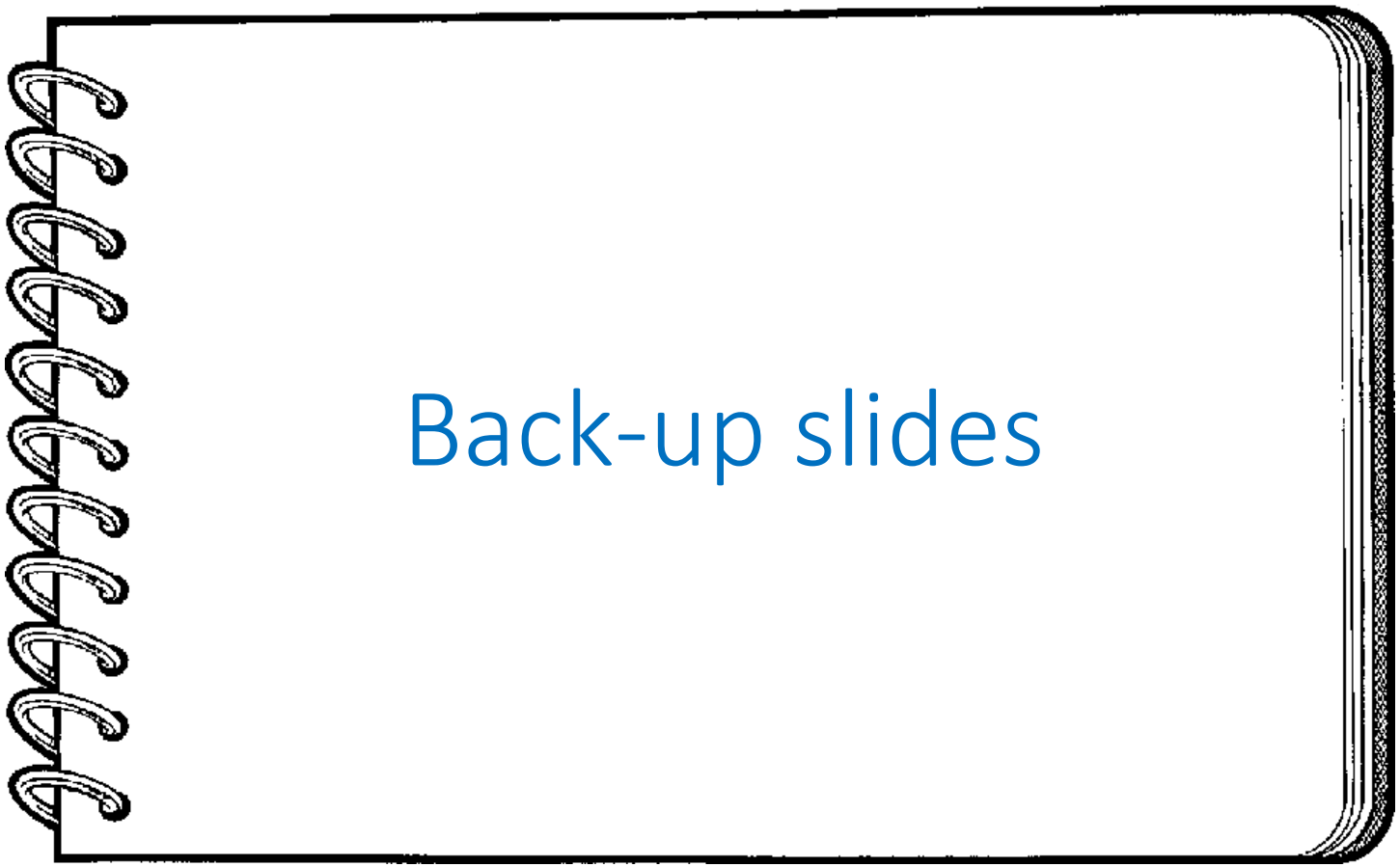
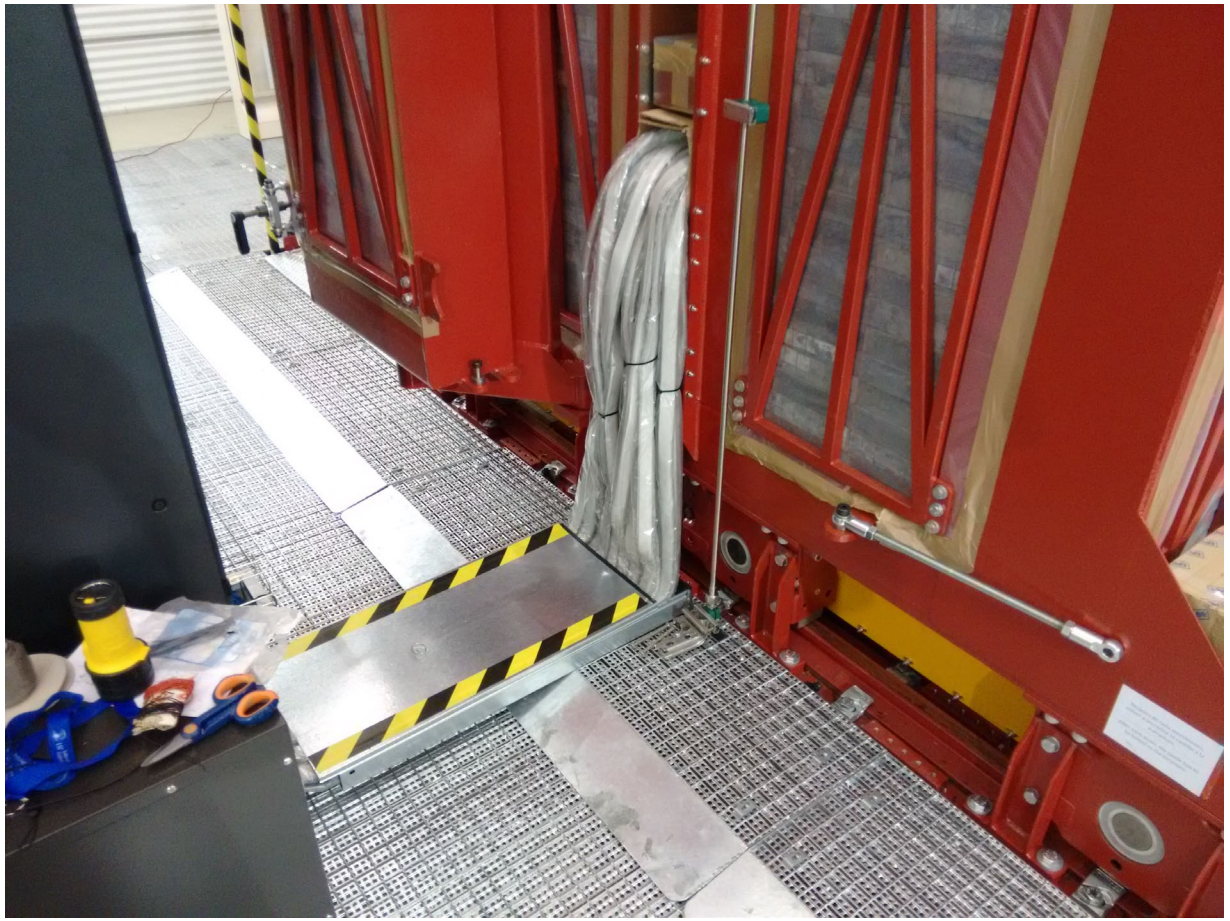
- NEXT SiPM FE board
  - TWEPP14 poster (link)
  - Paper (link, DOI: 10.1088/1748-0221/10/01/C01025)
- NEXT SIPM bias source
  - IWORID16 poster (link)
  - paper (link, DOI: 10.1088/1748-0221/11/12/C12035)
- PhD tesis on the SiPM FE (link)


Back-up slides

External cable bundles (ribbon cables + mesh shielding)



3D-printed HDMI locks to avoid disconnections