

3D Microfabricated Ion Trap and Integrated Optics

Jakob Wahl
ECCTI, 29.06.2022

ETH zürich

JOANNEUM
RESEARCH 

 universität
innsbruck

 infineon

Agenda

1 Infineon Technologies

2 3D PIEDMONS Project

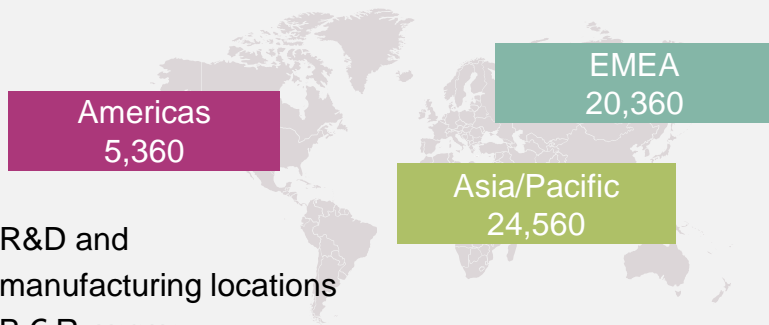
3 OptoQuant Project

Infineon is a Leading Semiconductor Player

leading player

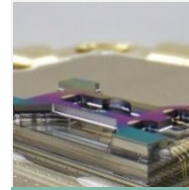
in automotive, systems for power, sensors, secure systems and many more

~50,280
employees



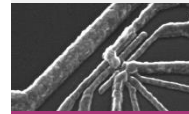
56 R&D and
20 manufacturing locations
11 B € Revenue
as of 30 September 2021

Quantum Computing at Infineon



Villach
Munich

Trapped Ions



Dresden
Munich

Silicon Quantum Dots



Regensburg
Munich

Superconducting Resonators

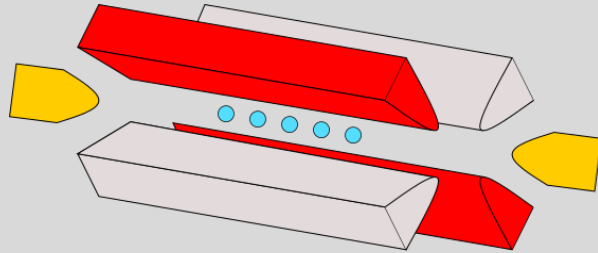


Villach
Munich

SiC / NV Color Centers

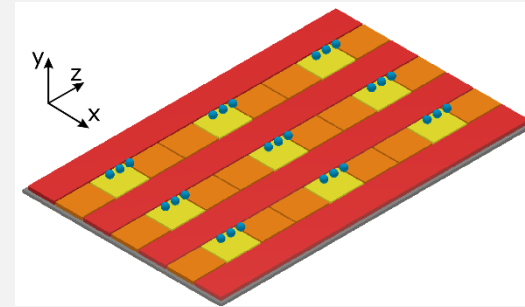
Scaling Towards 1000 Ions

Linear Ion Traps



More ions

Surface Ion Traps



- + Strong confinement
- + Reliable ion trapping / long lifetimes
- + High optical access
- + Room temperature operation

- Limited control of single ions.
- Free space optics only.

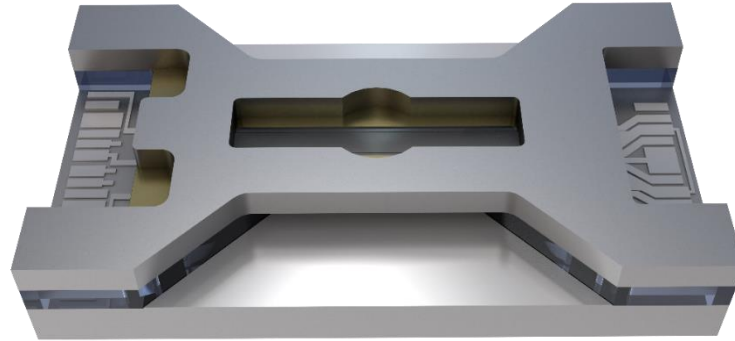
- + Scalable
- + Complex trap layouts
- + Individual control of single ions
- + Reproducible fabrication

- Weak confinement potential of around 100 meV

Agenda

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- 3 OptoQuant Project

3D Microfabricated Trap Designed for High Optical Access



Industrially microfabricated ion trap with 1 eV trap depth

S Auchter^{1,2,*,6} , C Axline^{3,*,6} , C Decaroli³ , M Valentini¹, L Purwin², R Oswald³,
 R Matt³, E Aschauer², Y Colombe² , P Holz⁴ , T Monz^{1,4} , R Blatt^{1,4,5} ,
 P Schindler¹ , C Rössler²  and J Home³ 

¹ Institut für Experimentalphysik, Universität Innsbruck, Technikerstraße 25, A-6020 Innsbruck, Austria

² Infineon Technologies Austria AG, Siemensstraße 2, A-9500 Villach, Austria

³ Institut für Quantenelektronik, ETH Zürich, Otto-Stern-Weg 1, CH-8093 Zürich, Switzerland

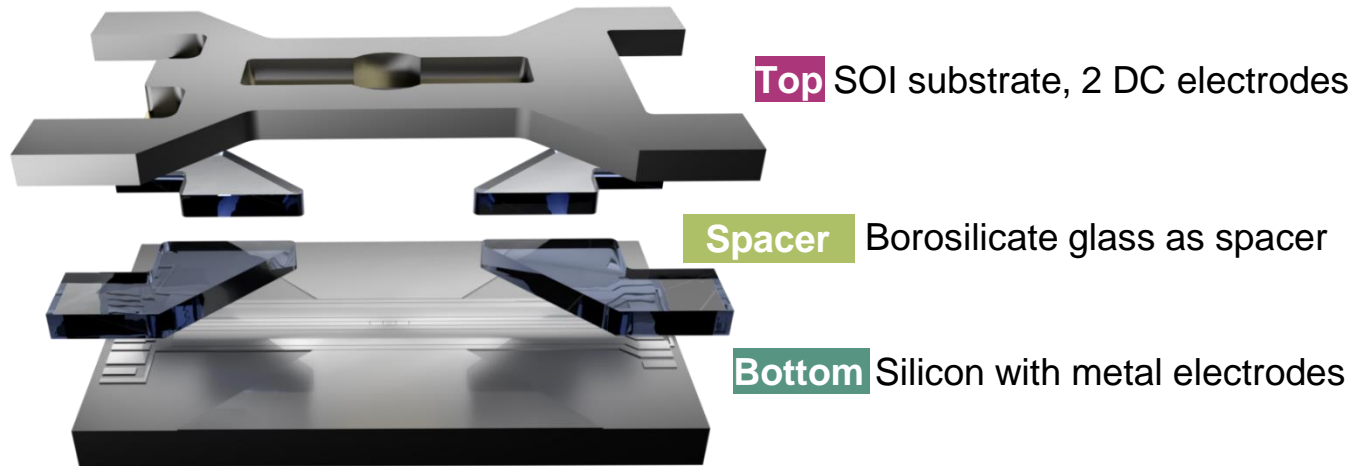
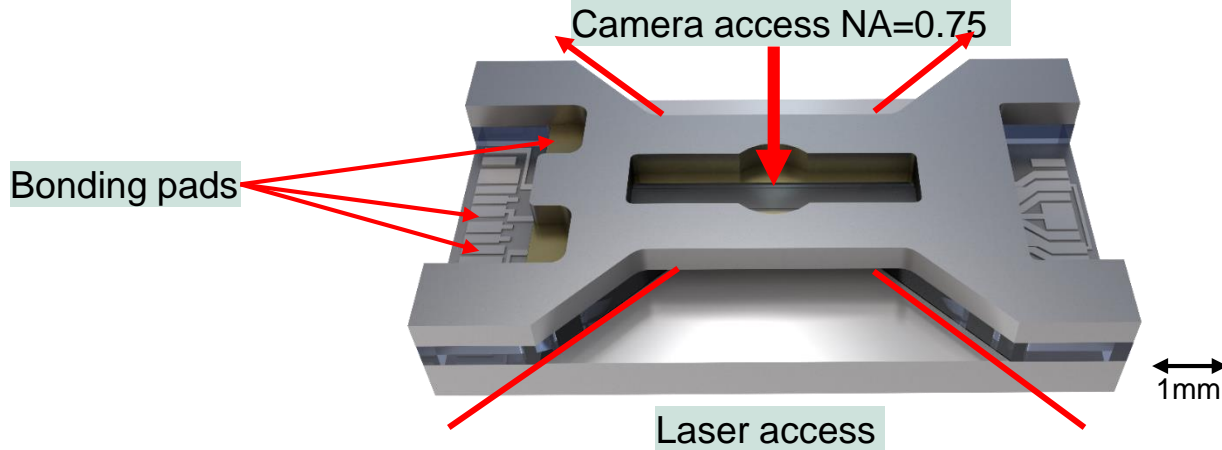
⁴ Alpine Quantum Technologies GmbH, Technikerstraße 17/1, A-6020 Innsbruck, Austria

⁵ Institut für Quantenoptik und Quanteninformation, Österreichische Akademie der Wissenschaften, Technikerstraße 21 A, A-6020 Innsbruck, Austria

* Authors to whom any correspondence should be addressed.

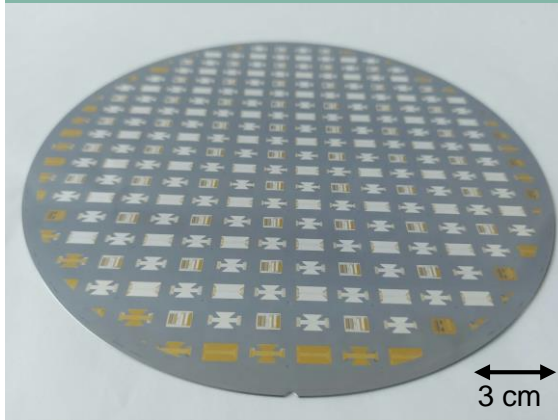
⁶ These authors contributed equally to this work.

3D Microfabricated Trap with High Optical Access



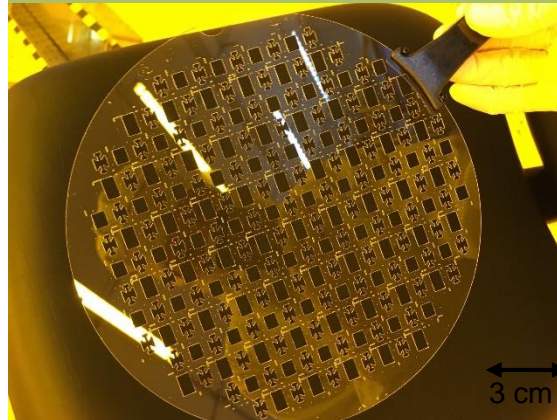
Trap Fabrication on Wafer Level

Bottom Wafer



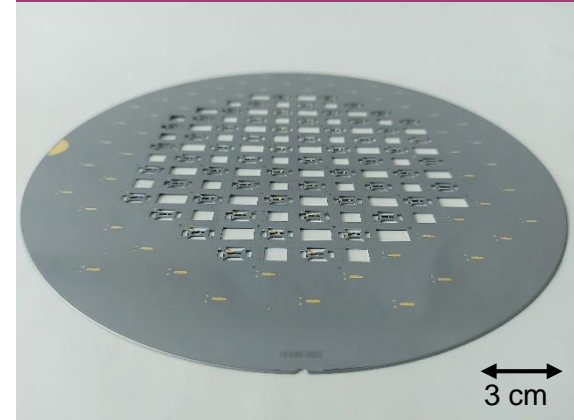
- > 725 μm
- > Silicon substrate
- > Three metal layers separated by SiO_x

Spacer Wafer



- > 400 μm
- > Borosilicate glass
- > Structured by isotropic wet etch

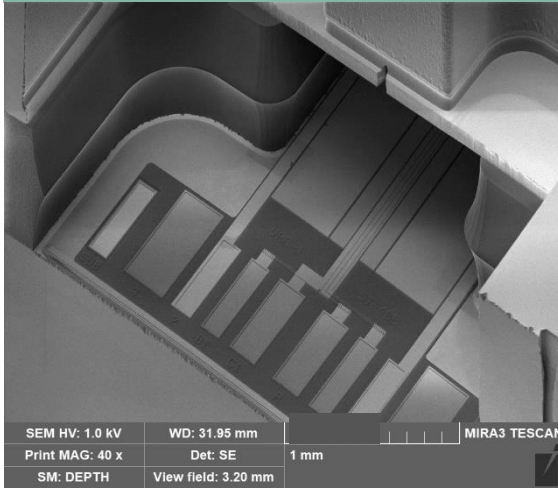
Top Wafer



- > 445 μm
- > SOI (silicon on insulator)
- > Gold coating via shadow mask evaporation

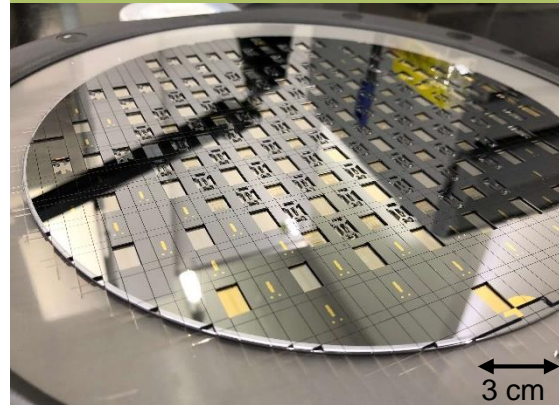
From Wafer to Module

Wafer Bonding



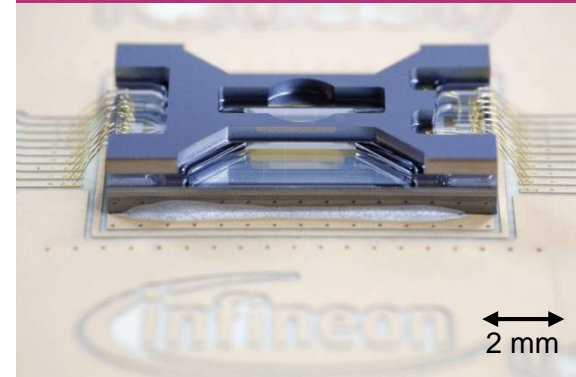
- > Anodic Wafer Bond

Dicing



- > Mechanical Dicing
- > 150µm wide dicing blade, 1.5 mm thick wafer stack

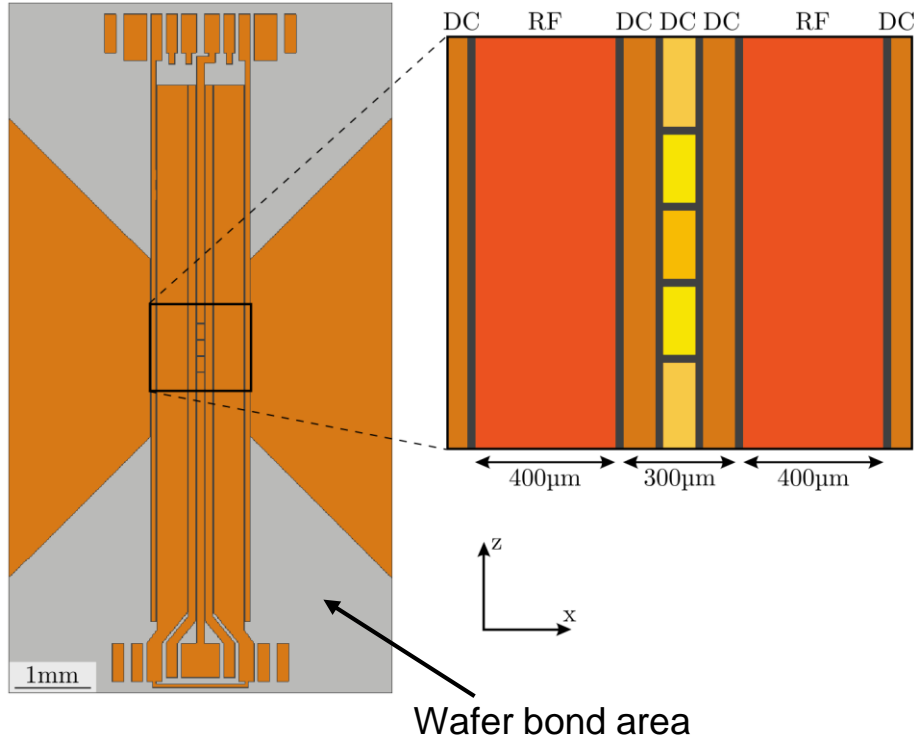
Packaging



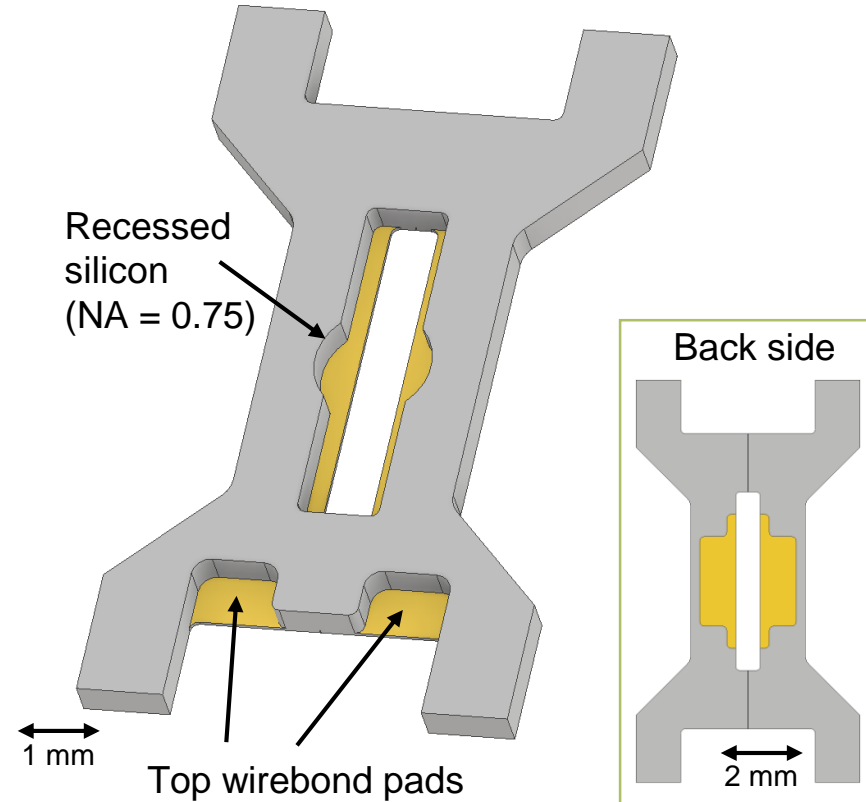
- > Glue to chip carrier
- > Automatic wire bonding

Trap Geometry for 1eV Trap Depth

Bottom Wafer



Top Wafer



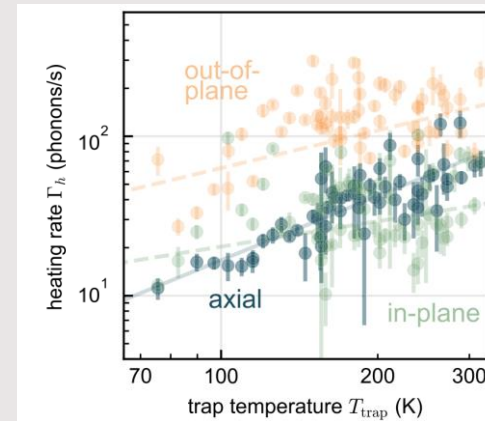
Ion Trap Operation at ETH

Trap Parameters



- > $V_{RF} = 180 \text{ V @ } 20.6 \text{ MHz}$
- > Secular frequencies
axial: 1.5 MHz
radial: (2.6 / 2.9) MHz

Heating Rate



Heating rate measurement: $\Gamma_h = 40 \text{ quanta/s}$

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Agenda

1

Infineon Technologies

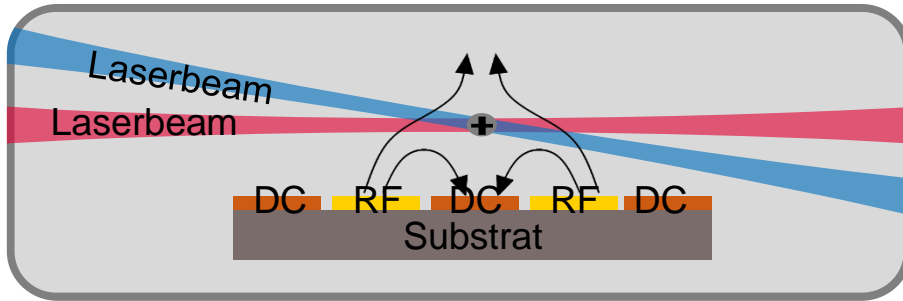
2

3D PIEDMONS Project

3

OptoQuant Project

Integration of Optics: OptoQuant Project

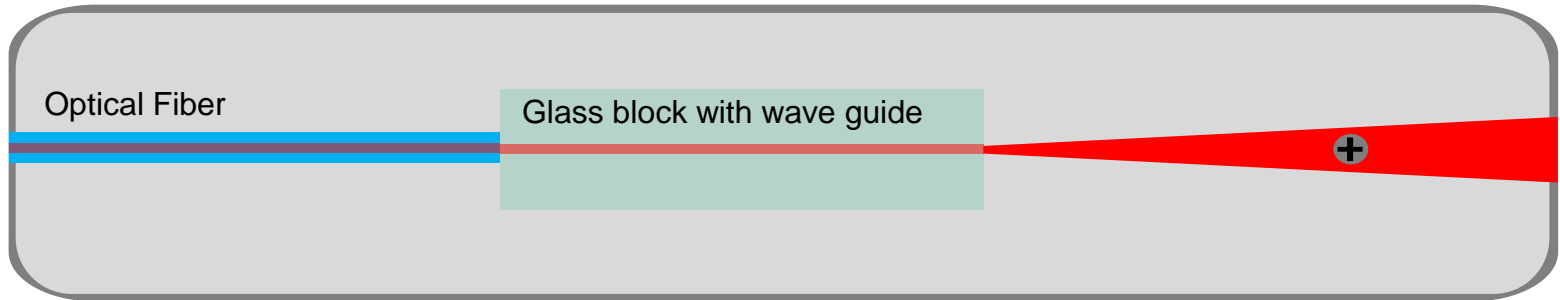


State of the art: free space optics

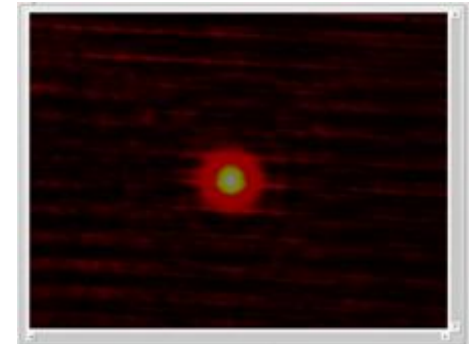
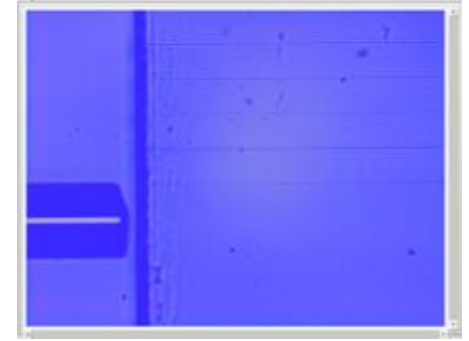
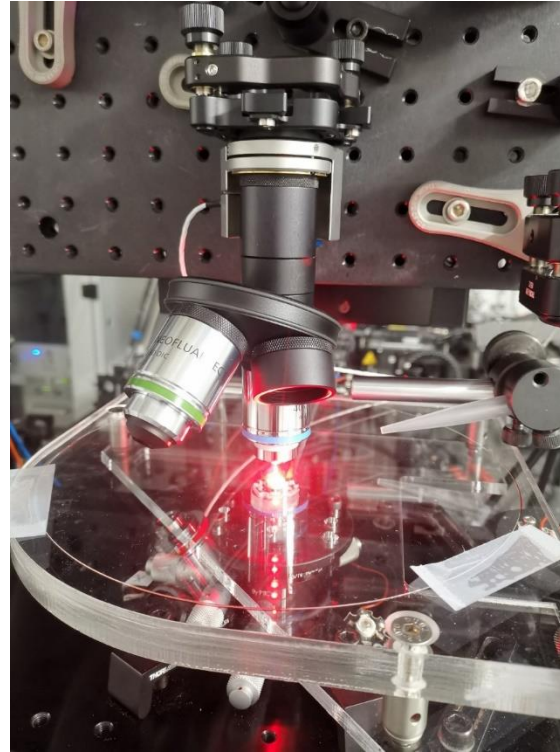
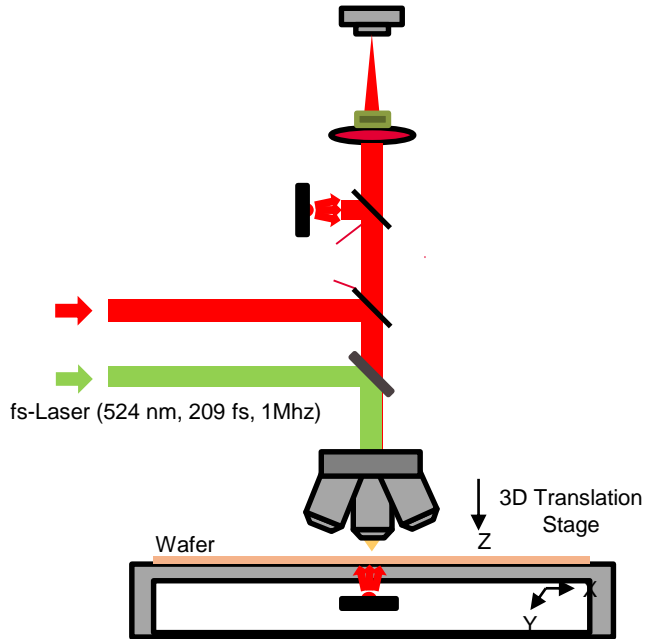
- > Beam pointing errors, crosstalk
- > Limited scalability



Goal: on-chip light guiding and ion addressing



Waveguide Scribing in Glass: Outlook

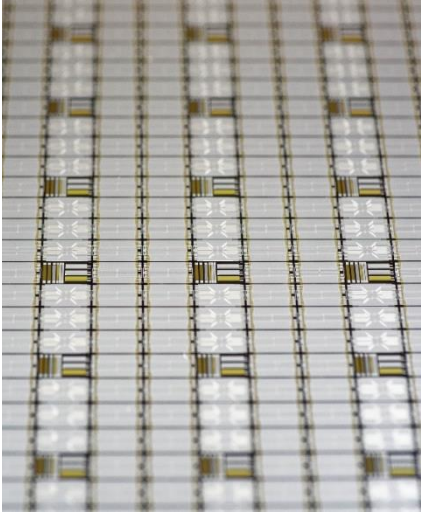
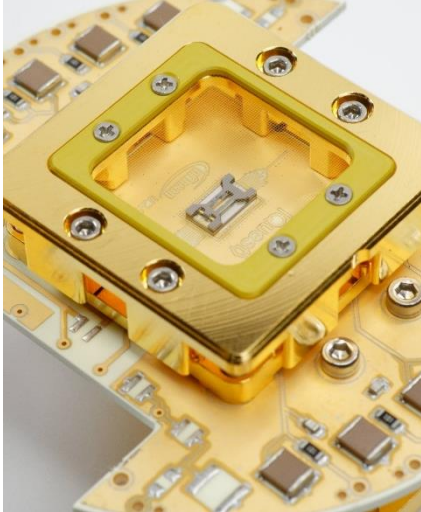
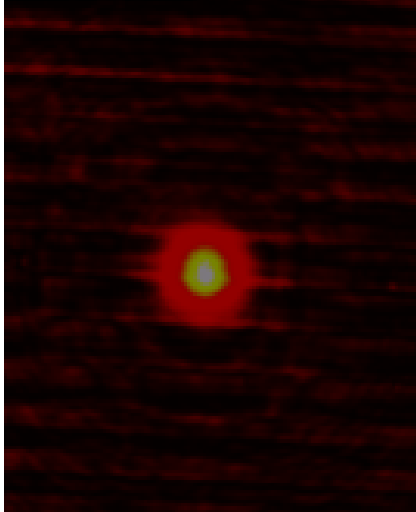


Images by Bernhard Lamprecht (JR)

Researchers



Summary

Infineon Ion Traps	3D PIEDMONS Trap	Integration of Optics
Aiming for Scaling	Microfabricated 1eV Trap	Ongoing work
		



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