Contribution ID: **72** Type: **Poster**

Demonstrating a logical qubit on a surface ion trap

Tuesday, 28 June 2022 18:21 (3 minutes)

The Ion Quantum Technology group has proposed a scalable quantum computing design made up of modular surface ion traps which slot together. One of the main challenges in realizing this design is demonstrating fault-tolerant error correction on a surface trap. We use an X-junction trap which has designated zones for trapping, performing quantum gates and reading out results. It uses surface electrodes to 'shuttle'ions around the chip and embedded B-field gradient coils with global microwave fields to perform quantum gates. We are working towards good shuttling control of our ions and demonstrating high-fidelity qubit gates. However, to demonstrate quantum error correction, we also need to translate error-correction schemes into shuttling protocols which are achievable on our chip. We aim in the long-term to demonstrate the 17-qubit surface code.

The poster will discuss the implementation of the 5-qubit error-correcting code on an X-junction with a focus on compilation. We outline a set of compiler stages between the error-correction protocol and the physical implementation. The error-correction protocol will look like a set of quantum gates acting on physical qubits, and the physical implementation will look like a shuttling routine of ions around the chip interspersed with quantum gates. The compilation involves two main translation stages: from logical qubits to computational qubits, and from computational qubits to physical qubits. Crucially, our ion qubits are distinguishable only through their location, unlike the computational qubit which are simply labelled 0, 1, 2 etc. We will present our progress in tackling these compilation stages using the quantum framework ProjectQ, and the application of the generated routines on our X-junction chips.

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Session Classification: Posters