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Dielectric Properties of Plasma Oxides for Microfabricated Ion Traps

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The upcoming revolution in computation - quantum computing - will open up new avenues to efficiently solve classically hard problems, like quantum simulation and optimization tasks. A leading implementation of a feasible quantum processor is realized by trapped ions, where electronic states in stored ions represent physical quantum bits (qubits) [1]. The microfabrication of ion traps [2, 3] is a necessary step towards upscaling of qubit numbers, which will ultimately enable error corrected quantum computing.

Microfabricated ion traps employ structured metal layers isolated by dielectrics that are deposited via plasma enhanced chemical vapor deposition (PECVD). Surface electrodes produce an electromagnetic stray field, which confines the ions a few tens of micrometers above the trap. During trap operation involving radiofrequency (RF) fields of about 20 MHz, the charging of parasitic capacitances inside the metal-oxide structure causes heat dissipation by two major mechanisms. First the RF field in the dielectrics leads to dipole relaxation losses, which is quantified by the dielectric loss tangent. Second the currents needed for capacitor charging cause Ohmic losses in the metal leads. This effect is proportional to metal resistivity and to the total capacitance between RF electrodes and RF ground.

This work investigates dielectric properties of various dielectrics available at Infineon, both in the regime of optical- and radio frequencies. On the one hand, chemical and structural properties are quantified via infrared spectroscopy. Ellipsometry provides additional information on the refractive index in the visible spectrum. On the other hand, the radio frequency responses of capacitor test structures were evaluated in a wafer probing setup at frequencies from 1 to 100 MHz. The main structural influencing factors on the permittivity, measured via infrared spectroscopy, are found to be the Si-OH peak height, the Si-O-Si peak width, as well as the time of thermal tempering and fluorine content. Within our experimental resolution, we determine an upper bound for dielectric losses in plasma oxides of $\tan\delta < 0.001$.

In a further analysis we find that replacing standard PECVD-deposited silane oxide with fluorosilicate glass would provide a reduction of dissipated power of up to 25% in future 1000 qubit ion traps. Finally, additional paths towards a lower overall power dissipation in large microfabricated ion traps are discussed.

[1] C. Bruzewicz et al., Trapped-Ion Quantum Computing: Progress and Challenges, Applied Physics Reviews (2019)
[2] P. Holz et al., 2D Linear Trap Array for Quantum Information Processing, Advanced Quantum Technologies (2020)
[3] R. J. Clark et al., A two-dimensional lattice ion trap for quantum simulation, Journal of Applied Physics (2009)

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