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TSV-integrated Surface Electrode Ion Trap for Scalable Quantum Information Processing

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Ion traps and their geometry have seen their complexity increase for several years. Examples of this trend are the integration of waveguides, photodetectors [1] and the design of array of trap [2][3][4]. To continue in this path, significant challenges for electric signal delivery must be solved. I will present a functional trap using Through Silicon Vias (TSV) electrodes connection (both Radio-Frequency (RF) and Direct Current (DC)) which is fully foundry compatible.

In this work, we report about design, fabrication and operation of a Cu-filled through silicon via integrated ion trap. With intrinsically small resistance, Cu-filled TSVs are used here as vertical connections between all the electrodes (including RF electrodes) and an interposer underneath. Besides, a standard CMOS process on a 12-inch wafer is used, facilitating high resolution and repeatability of trap fabrication. The integration of TSVs permit a significant reduction of electrode surfaces, decreasing the trap capacitance up to 90% in comparison to a wire bonded trap of same size. A low RF dissipation is achieved in spite of the absence of a screening layer. We evaluate the trap performances by loading and laser-cooling single 88Sr+ ions and by measuring the trap heating-rate using the technique of Doppler re-cooling [5]. The heating rate of the trap is evaluated at 250mK/s that corresponds to 17 quanta/ms for an axial frequency of 300 kHz. The lifetime of a laser-cooled ion in the trap is of the order of 30 minutes, compatible with the vacuum level.

This work pioneers the development of TSV-integrated ion traps, enriching the toolbox for scalable quantum computing. In particular the TSV approach is compatible with insertion of a ground screening layer to eliminate trap-heating, photonic circuit integration on which we are currently working, and in the future could be extended to glass substrates. In the future, further optimization of both TSV and multilayer metallization technologies (overlapping of alternate metal layers and dielectric materials beneath surface electrodes) is foreseen. However, a combination of the two techniques will be probably necessary to realize larger-scale ion traps with lower RF losses, and higher density of photonic components.

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[3] Niffenegger *et al.*, Nature **586**, 538–542 (2020)

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