203rd Meeting of the Machine Protection Panel

Injectors topics

January 29th, 2021 via Zoom

Participants:

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The slides of all presentations can be found on the website of the Machine Protection Panel and on Indico (203rd meeting).

Minutes from the 201st MPP meeting (Injectors topics)

Daniel recalled the actions from the 201st MPP meeting on the crystal installation for the SPS slow extraction. No comment followed and the minutes are approved.

SPS dI/dt: Status and interlocking strategy (Tom Levens)

Tom recalled the incident in August 2018 when fast beam losses appeared during a slow extraction, because the tune crossed the half-integer resonance. This resulted in a vacuum leak in MBB 331. A 48-hour downtime followed, including dose to personnel. OP requested to improve the beam instrumentation in the SPS to protect against such fast losses. Three beam instrumentation measures have been implemented: BPM interlocks, BLM software upgrade and the dI/dt interlock. The requirements are described in EDMS 2038204. The implementation status had been presented at the MPP workshop in 2019.

Two integration times are considered for the dI/dt system: 1 ms and 10 ms, with different loss thresholds each, respectively 3e11 p^+ and 1e12 p^+. The DCBCTs in LSS5 are used, as also un-bunched beam is measured by them, using redundant detectors and acquisition chains. The present DCBCTs in LSS5 provide analog outputs (calibrated in mV/1e10 charges), which are brought to 2 VME crates in BA5. This acquisition chain is too slow (200 samples per second). A new development using BI-standard VFC readout electronics, which can reuse many parts of the LHC dI/dt system, is proposed. The VFC will have an output to the CIBU.

The requested 3e11 p^+ in 1ms is at the limit of the detector analogue performance. Relaxed specifications were finalized and a 2 ms integration time (instead of 1 ms) has been accepted by OP. The threshold associated with this 2 ms integration time was specified at 5e11 p^+

instead of the original 3e11 p^+ in 1 ms. The plan is to install the first prototype of this new system during LS2.

In addition, a new 24-bit ADC module (as for the LHC) has been developed since the 2019 MPP workshop. The specified 3e11 p^+ in 1 ms correspond for this system to 15 mV with a bandwidth > 1kHz.

Because of the dump relocation project, the DCBCTs in LSS5 have been moved from 518 to 514. The new CIBU has been installed and the connections have been commissioned with TE-MPE. The VFCs are installed in VME crates located in BA5 and the 24-bit ADC module assembly is soon to be completed. The installation of a complete test system in BA5 is to be done soon. Both redundant DCBCT in LSS5 will be equipped with dI/dt systems. However, only one will be connected to the BIS, the second one will be used as hot spare and development system.

A BCT calibration pulse is sent before injection at each cycle. The signal is sampled and stored in two history buffers (one for each integration time). The samples in the buffers are compared, the dump signal to the CIBU is activated if either loss rate is exceeded.

The firmware has been tested in the lab. The spikes in the measured signal are coming from the modulation injected in the DCBCT. The spikes are reduced with the averaging of the samples from the history buffer. The test must be repeated in BA5 to account for the actual conditions (longer cables, additional noise, etc.).

Questions

- Jan asked about the sampling rate. Tom replied that there are 10 samples/ms and the measurement is the average of 8 samples for noise reduction. This can be adjusted.
- Kevin asked about the spikes in the signal. They come from the modulation frequency which is sent to the BCCT. Kevin commented that it should be easy to filter them out.

The DCBCTs in LSS5 have a hardware cross-check procedure running at the start of each cycle to verify that they are functioning correctly. At the end of the generated current pulse (increased steps), a large dI/dt will trigger the interlock (at around -300 ms). The beam permit would be removed systematically a few hundreds of milliseconds before injection. This has the advantage of checking that the dI/dt is working properly. However, to avoid disrupting the injection process, the CIBU user permit should not be changed between -450 ms to -300 ms and -250 ms to injection.

The proposal is to add a hardware mask from -900 ms to -275 ms to avoid removing the user permit during the cross-check pulse. The start of the mask would be the same LTIM event which triggers the calibration. The end of the mask would be after a 625 ms delay generated in the FPGA. Currently the cross-check is also sent during coast (triggered by the SX.ACQF900-CT event). Due to the dI/dt masking this would imply a 625 ms “dead” period in every timing cycle during coast. To avoid this issue, it is proposed to move the trigger to an injection referenced timing event (SIX.F1KFO-CT + 100 ms). That way, the cross-check and masking will not be triggered during coast. It should be checked in detail that it does not impact the use of the BCTs for the North Area personnel protection.

The following parameters are set to configure the interlock:

- Short window loss threshold (charges).

- Long window loss threshold (charges).
- Short window length (ms).
- Long window length (ms).
- Calibration factor (ADC bins / charge).

To allow operational flexibility, the specification requests that these thresholds can be modified on a PPM basis. These will be exposed in the FESA class as machine critical settings. This has impacts, for example if the FESA class crashes and does not write settings for the new cycle. If going from a cycle with high thresholds to low thresholds this could remove the protection. A hardware cross-check verifying that the settings are written is needed for each cycle. It is proposed that at the end of the masked period (at 275 ms prior to injection), it is verified that a dI/dt interlock has triggered at the end of the calibration pulse, and that the new settings are received from the FESA class. If this is not the case, the user permit is removed before injection.

Tom finished the presentation by summarizing the next steps:

- The hardware and firmware are well advanced.
- The work on the FESA class will start soon.
- More detailed tests must be done: simulation of various loss rates, gathering of statistics regarding the reliability of the system.
- The goal is to have a first prototype system ready to test during the SPS beam commissioning.
- The dI/dt CIBU channel will initially be disabled.

Discussion

Jan asked about the interlock masking: how can we make sure that the mask is removed? Tom replied that it comes from a hardware timing trigger in the FPGA, which is reliable. A software check could be foreseen. Jan added that it would be interesting to verify that the dI/dt triggers at the end of the cycle, *e.g.* if some beam is dumped. It can be checked for LHC beams with the fast extraction. Jan commented that the masking and checks prior to injection add complexity to the system which is robust in itself.

Daniel commented that the calibration pulses are triggered by the timing event and asked about failures from the decoding of the timing events which could affect the interlocking. Tom replied that receiving the timing pulse is crucial.
Kevin asked what stops the interlock mask. Tom replied that it is a counter in the FPGA. Kevin added that it seems to be safe enough.

Verena asked what would happen if the countdown timer gets stuck and if it is checked by another process. Tom replied that it is a hardware logic implemented in the FPGA. It could be made redundant. Jan added that it looks like added complexity.

What is the logic and justification behind the request to have PPM thresholds? Verena replied that it is due to the different beam types, for some of them, on purpose the beam is slowly extracted. The main difference is between the fast extraction and the slow extraction. Verena and Kevin commented that purely from a machine protection point of view, it would be possible to live with a single setting. Kevin commented that it is a limitation for operational flexibility.

Verena summarized that it appears that the main complexity comes from the calibration pulse at the beginning of each cycle: by design it will trigger an interlock at the wrong moment.

David asked about the personnel protection aspects of the DCBCT systems. Tom replied that it is a fully hardware system using the analog signal from the DCBCT. If the intensity exceeds a threshold, then a signal is sent to the CCR which inhibits the slow extraction. Jan asked how the slow extraction is prevented. Verena replied that the septum is tripped.

Daniel added that one should have a detailed look at the values of the different thresholds.

Daniel asked about the need to perform beam quality checks using the dI/dt system. Daniel added that on top of the PPM thresholds, one should also be able to define a "maximum" threshold which cannot be exceeded. Verena commented that this is doable.

Verena commented that the same system is used for three different purposes (intensity measurement, dI/dt and personnel protection). Verena asked if it is a possibility to have dedicated BCT system for each use cases. Tom replied that it is in principle possible, however it implies that additional BCTs would have to be installed (the existing ones in BA3 have higher noise level).

David commented that the beam dump should set the beam permit to false, so that it is false as an initial condition at the beginning of the cycle. It would then be enabled. A potential issue of this system is the dependency between the interlocks and the timing systems.

Daniel commented that a detailed summary of the thresholds values is needed (worst-case value for which the interlock should always be triggered for machine protection, and additional PPM values for beam quality and operation). In addition, these should be reviewed at the end of 2021 based on the operational experience.

Actions

1. Prepare table of expected operational thresholds to be used in the dI/dt during the different SPS cycles and add to specification document (Kevin Li).
2. Present first experience with dI/dt after commissioning period at the moment of activation of dI/dt BIS channel or at the end of the 1st year of operation (whichever is earlier) (Tom Levens, Kevin Li).

Summary of actions

The actions from the meeting are:

- SPS dI/dt: Status and interlocking strategy:
    1. Prepare a table of expected operational thresholds to be used in the dI/dt during the different SPS cycles and add it to the specification document (Kevin Li).
    2. Present first experience with dI/dt after commissioning period at the moment of activation of dI/dt BIS channel or at the end of the 1st year of operation (whatever is earlier) (Tom Levens, Kevin Li).