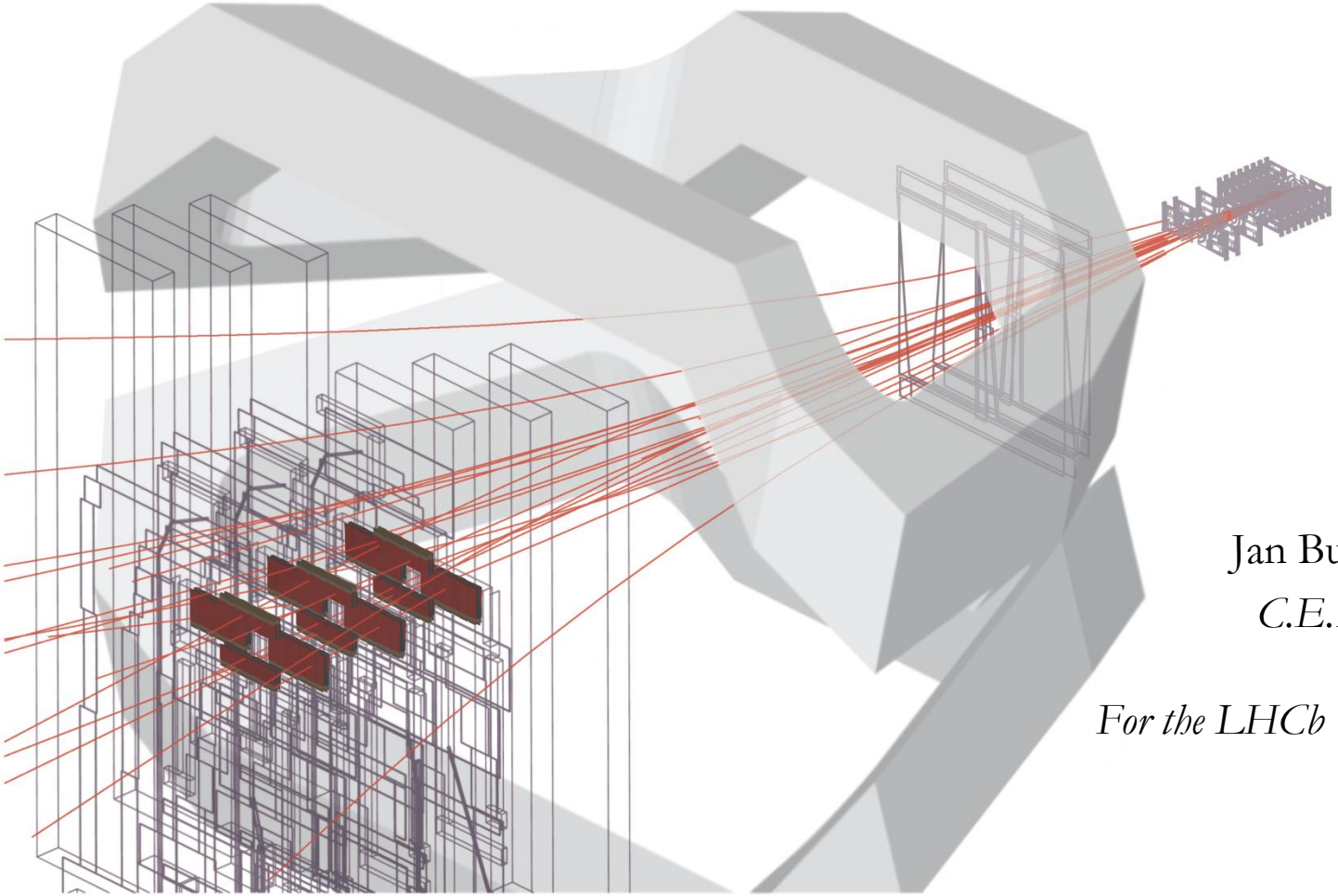
LHCb Vertex detector upgrade.

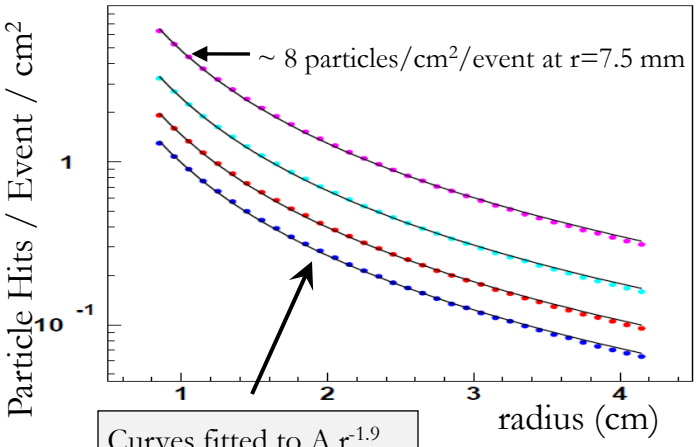


Jan Buytaert
C.E.R.N.

For the LHCb VELO Group.

Vertex detector environment.

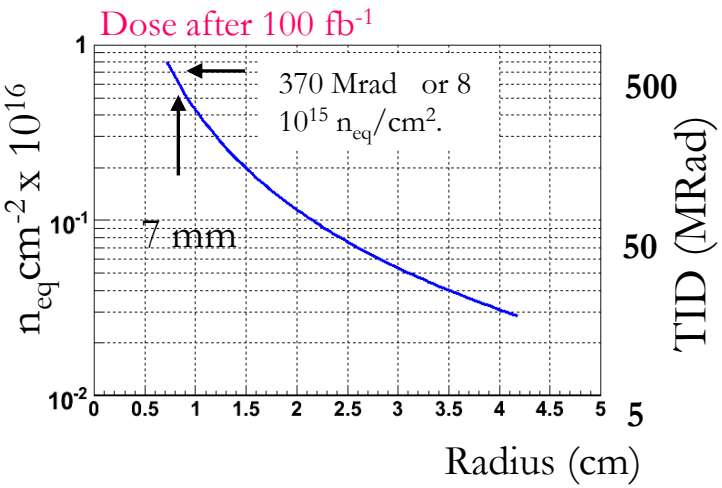
Particle occupancy per event (simulation)



Curves fitted to $A.r^{-1.9}$

Luminosity ($cm^{-2}s^{-1}$)	2.10^{32} Current	5.10^{32}	10.10^{32}	20.10^{32} Upgrade
A=	0.98	1.46	2.46	4.80

Severe & non-uniform irradiation damage.



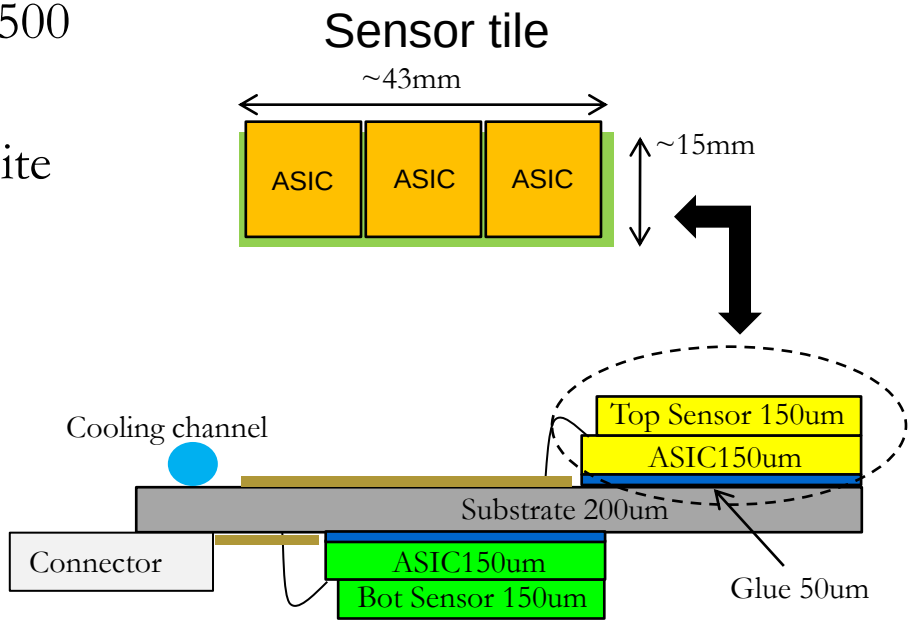
=> Danger of thermal run away !

=> Silicon must be cooled to -10 ^{0}C.

- The detector operates in 10^{-6} mbar vacuum.
- Access after installation is VERY difficult!

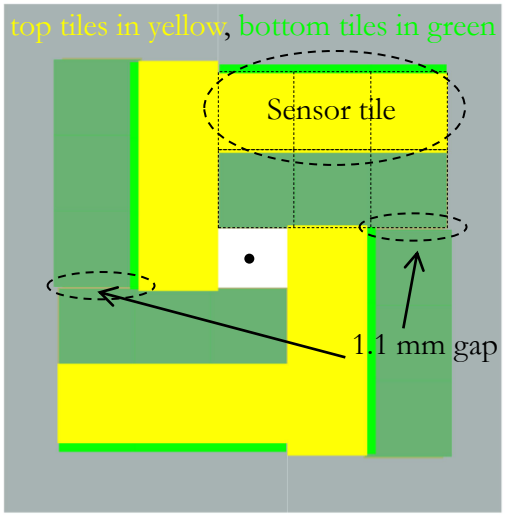
Pixel module.

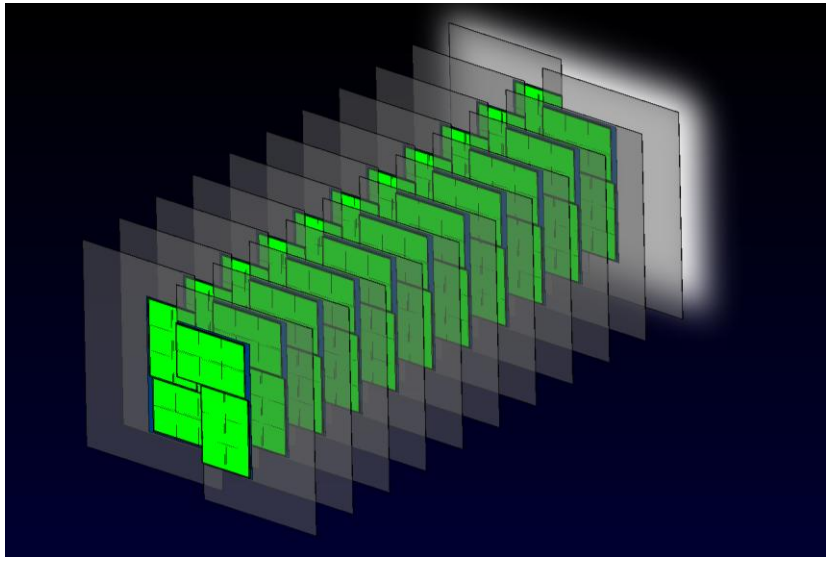
- Base design:
  - Sensor tiles: made of 3 readout asic's on a single sensor, with a guard ring of 500 um.
  - 2 sensor tiles are mounted on opposite sides of the substrate.
  - Substrate choices:
    - Diamond : excellent mechanical and thermal properties: => low mass
    - carbonfibre/TPG : as used for the present VELO.
  - Prototype work is starting using Timepix assemblies.
  - If the TSV technology becomes accessible soon, single sided modules could be possible.



Pixel module & Detector layout.

- A ‘station’ is made of 8 sensor tiles.
  - active area is near 100% (except small gaps).
  - Closest pixel is at 7.5 mm from the beam center.

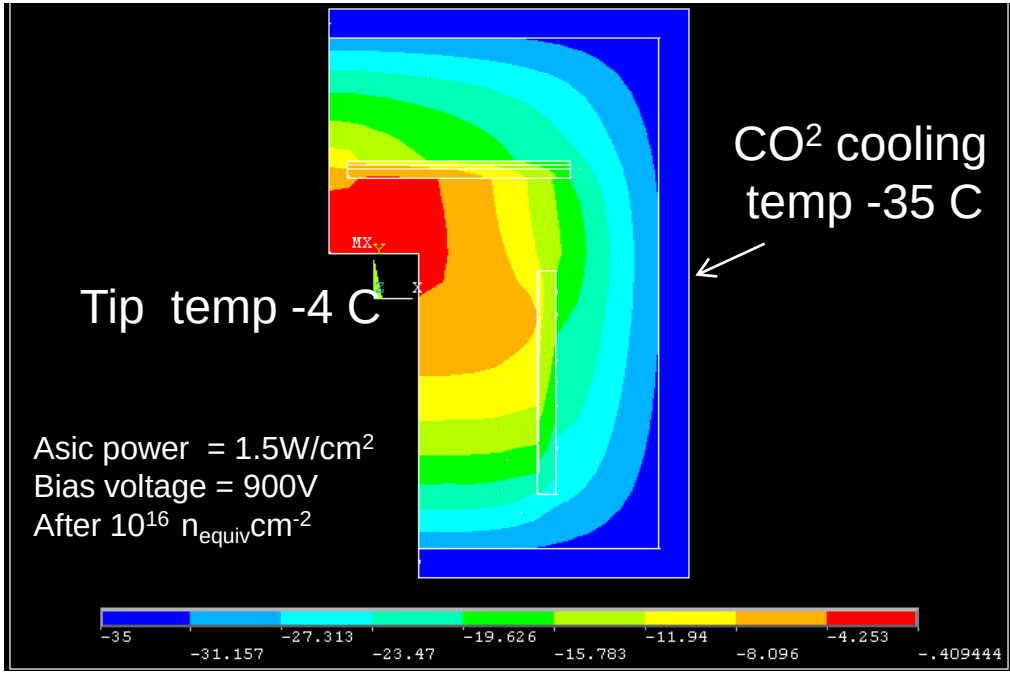




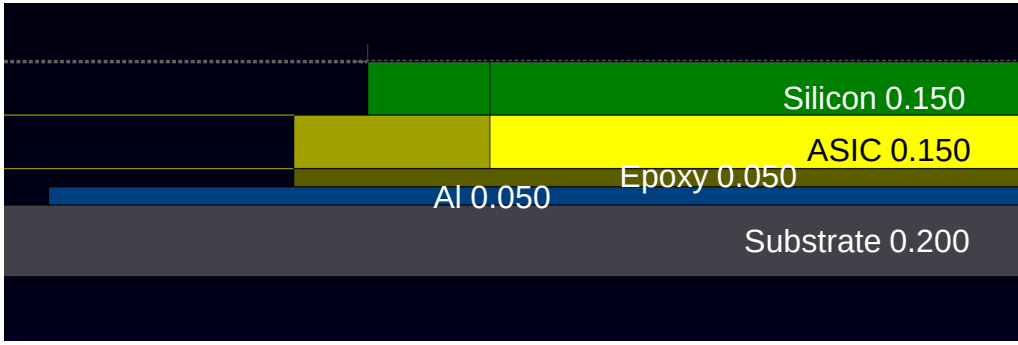
- The full detector is composed of 26 stations.
- The modules on either side of the beam are staggered to create overlap regions.
- This layout has been simulated to be fully efficient (4 hit per track) in the LHCb acceptance 250x300mrad.

Module Cooling.

- Initial ANSYS simulations done.
- Model includes radial ($r^{-1.9}$) and temperature dependent leakage power generated in Si.
- Extreme conditions are just OK...
- Verifications with thermal mockups are planned.



Material	Thermal Conductivity (W / m K)
Silicon	150
ASICs	190
Glue	1
Aluminum	200
CVD Diamond	1600



All dimensions in mm

ASIC development: analog

- We are collaborating with the Timepix2 design:
  - Analog requirements overlap ~100%:

Input charge	Bipolar (h+ and e-)
Leakage current compensation	YES (both polarities)
Peaking time	≤ 25ns
Preamp output linear dynamic range	< 40 Ke-
TOT linearity and range	<200 Ke- → Maximize linearity >200 Ke- → Monotonic response
ENC (σ_{ENC})	~75 e-
Detector capacitance	< 50 fF
Discriminator response time	< 2ns
Full chip minimum detectable charge	< 500 e-
Threshold spread after tuning	< 30 e-
Pixel analog power consumption	< 15-20 µW @ 1.2V

Full chip analog<1.3W

ASIC development: digital

- Timepix2:
  - Digital functionality :
    - Simultaneous Time-over-threshold and time identification.
    - sparse and data driven readout.
    - High speed output links >N x 500Mbit/s.
    - Still under discussion.
  - Peripheral logic and DAC's from Medipix3
  - Total power budget <1.5W/cm^2 @ 1.2 V. ⇔ <3W full chip
  - Radiation hardness TID 400Mrad, but not SEU.
- Final VELOpix will be derived from Timepix2 :
  - Only modifications in digital parts : Clustering, formatting & buffering, SEU protection.
  - Addition of multi-Gbit output links.

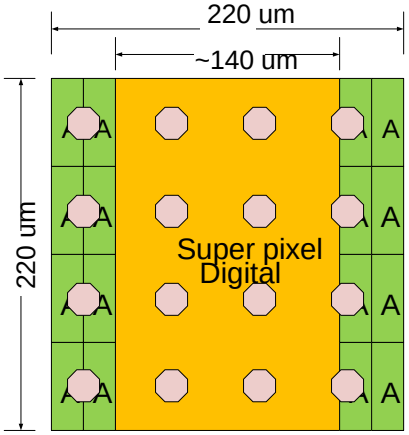
Data rates

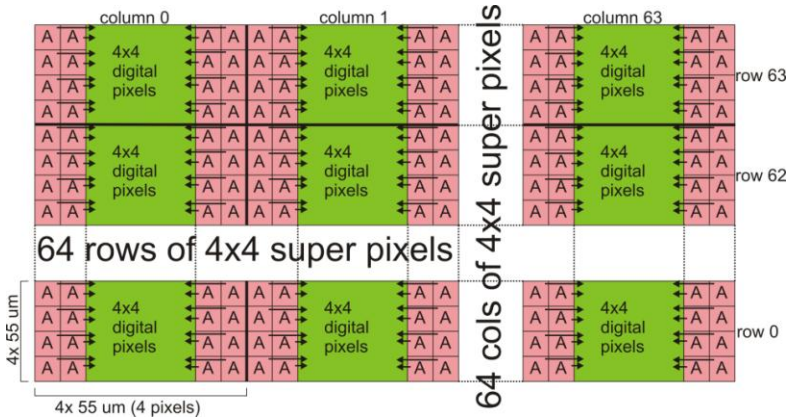
- Numbers at highest occupancies:
  - average particle rate per asic ~ 5 particles/25ns = 200MHz
  - average pixel cluster size ~3: (pessimistic assumption, 300um Si)
- Information bits per pixel : 32 !
  - 4 bit : Time over Threshold value.
  - 12 bit : bunch identification
  - 16 bit : pixel address.

  => Single asic data production can reach 19 Gbit/s !
- 30% data reduction can be achieved by clustering data: 13.6Gbit/s
  - share the bunch id (12bit) between clustered pixels,
  - 'share' address bits (by special encoding).
  - must be done before column readout, i.e. inside pixel array !
  - most efficiently in units of 4x4 pixels = "Super pixel"

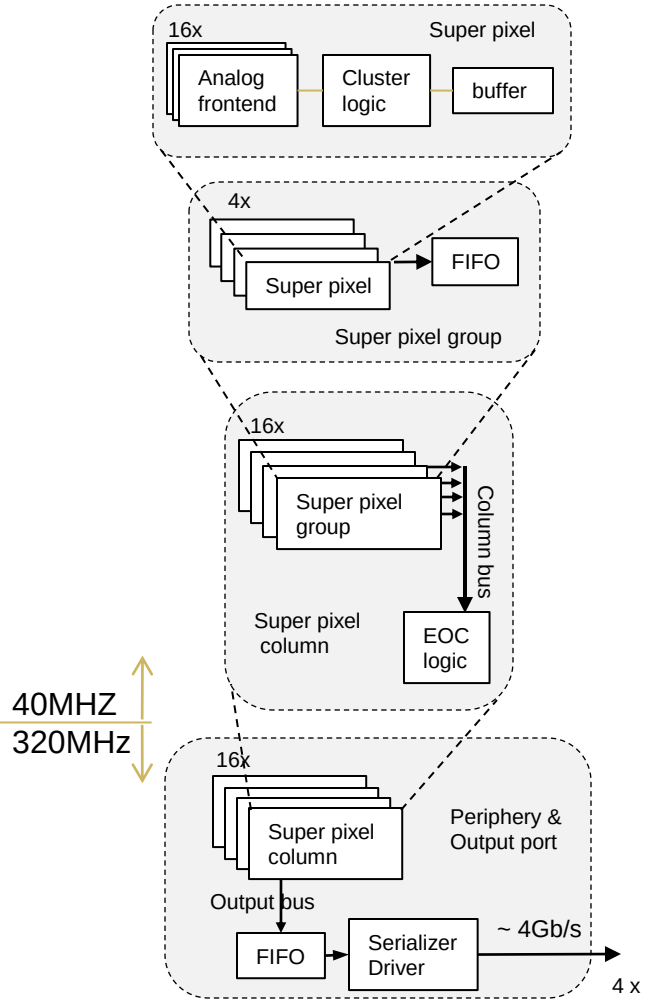
Super pixel

- Super pixel layout:
  - group digital logic in a single area.
    - Advantages:
      - Space saving : some functional blocks can be common (time-multiplexed).
      - More efficient distribution of power and global signals.
      - Better analog/digital isolation.
      - Digital column logic is synthesized with standard library. Ease, reliability, yield …
    - Disadvantages:
      - Bonding pads on top of digital circuit:
        => digital feedback in analog frontend. Shielding ?
      - Non-uniform analog input capacitance:
        => Only small effect
    - Status:
      - The verilog code for digital column exists and has been laid out. Final simulations are done. We will have realistic power estimates soon.
      - It would be extremely useful to have a 'low speed/low power' library for IBM 130nm ! Would result in a big saving in area and power !





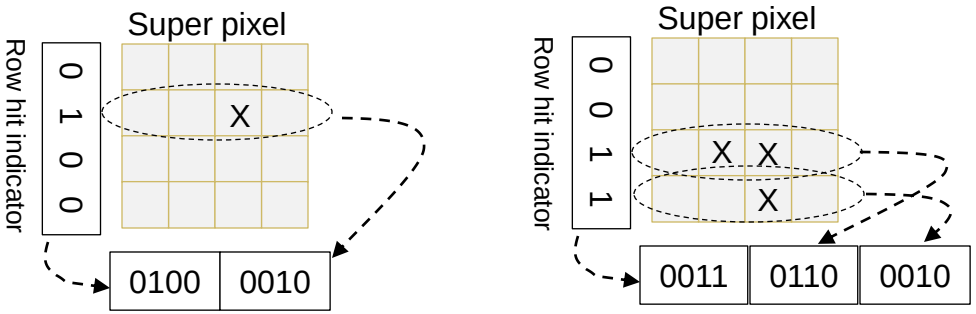
Pixel matrix readout architecture.



- Pixel matrix readout architecture
  - Internal bus speeds:
    - Column bus : 8bit@40MHz
    - Output bus : 16bit@320MHz
  - Total ASIC output : ~16Gb/s.
  - Buffering in :
    - Super pixel : 2 clusters
    - Super pixel group FIFO : ~400 bit
    - Output FIFO: multi kbyte
- Simulation shows losses< 0.5% in highest occupancy conditions.

ASIC design. Data reduction

- Address encoding in 4x4 super pixel :
  - "Row hit indicator" : indicate which rows have hits (4 bit, always present).
  - 0 to 4 "row hit patterns" : indicate which pixels in row are hit (4bit).
  - Super pixel address : 12 bit.
  - Examples:

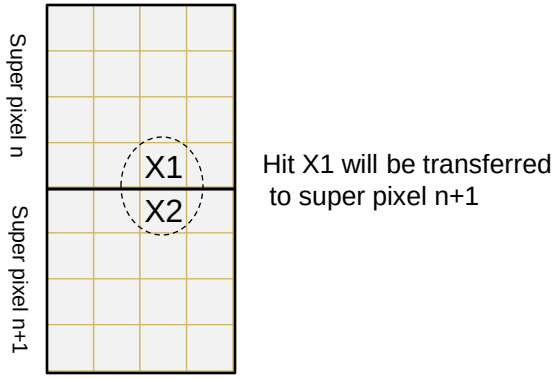


  - Gain compared to individual pixel address :
  - Reject large multiplicity :
    - If hit > N then no readout.
    - N is configurable and rejection can be de-activated.

# hits	Individual address	Row hit encoding
1	16 bit	20 bit
2	32 bit	24 bit
3	48 bit	28 bit
4	64 bit	32 bit

ASIC design. Data reduction

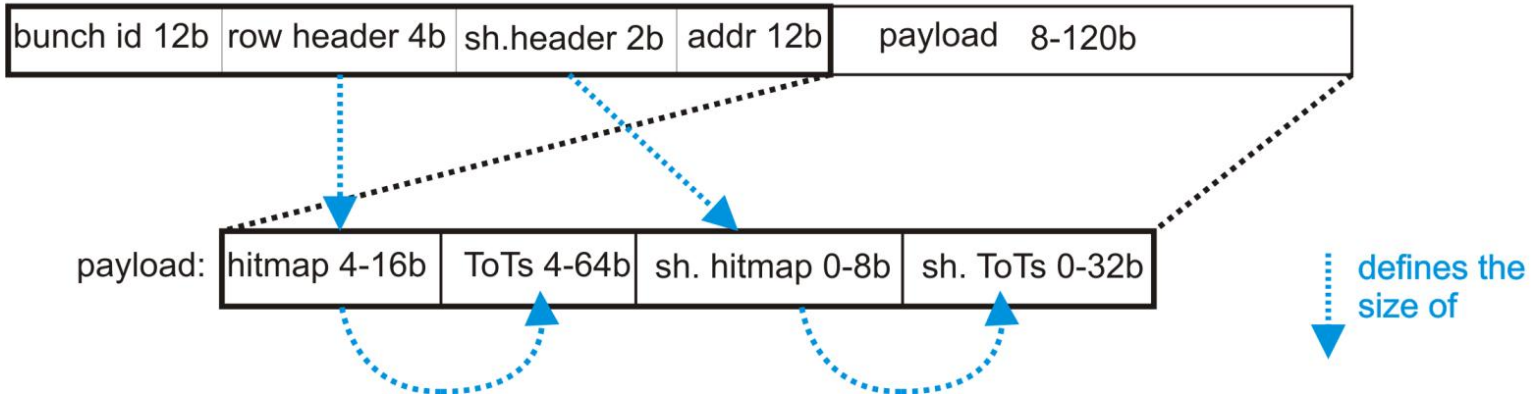
- Sharing across super pixel boundaries :
  - Only in 1 direction (column)
  - some limitations may lead to wrong or no clustering. But never loss of data.
  - Results in ~10% data reduction.



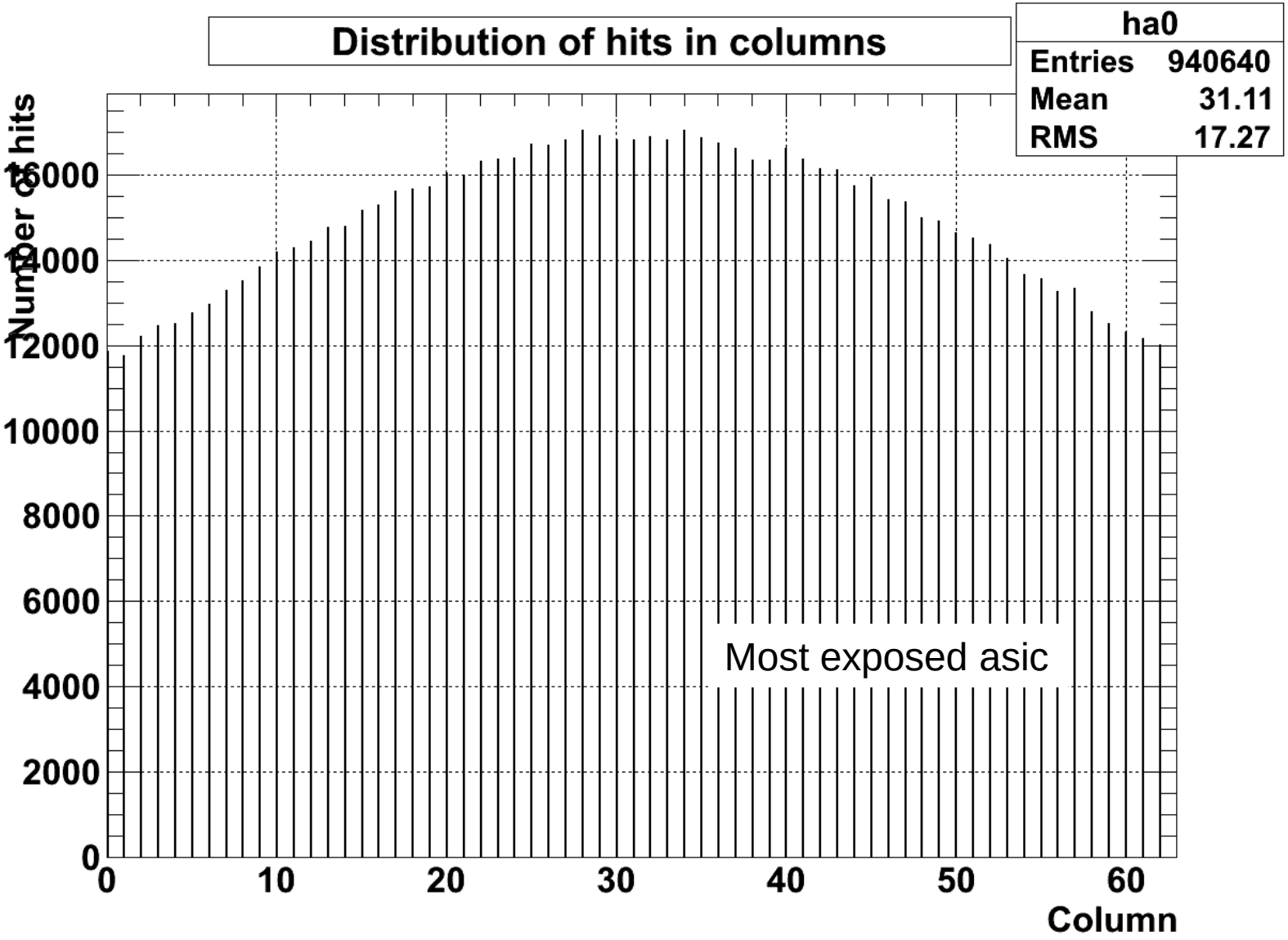
Packet format

Header(fixed size) 30 bits: bunch ID 12 bits, row header 4 bits, sharing header 2 bits, address 12 bits

Payload(varying size but fields in specified order):
- Hitmap: 4-16 bits
- Time-over-threshold (ToT) values: 4-64 bits
- Shared hitmap: 0-8 bits
- Shared ToT values: 0-32 bits



Simulations with Gauss/Boole data



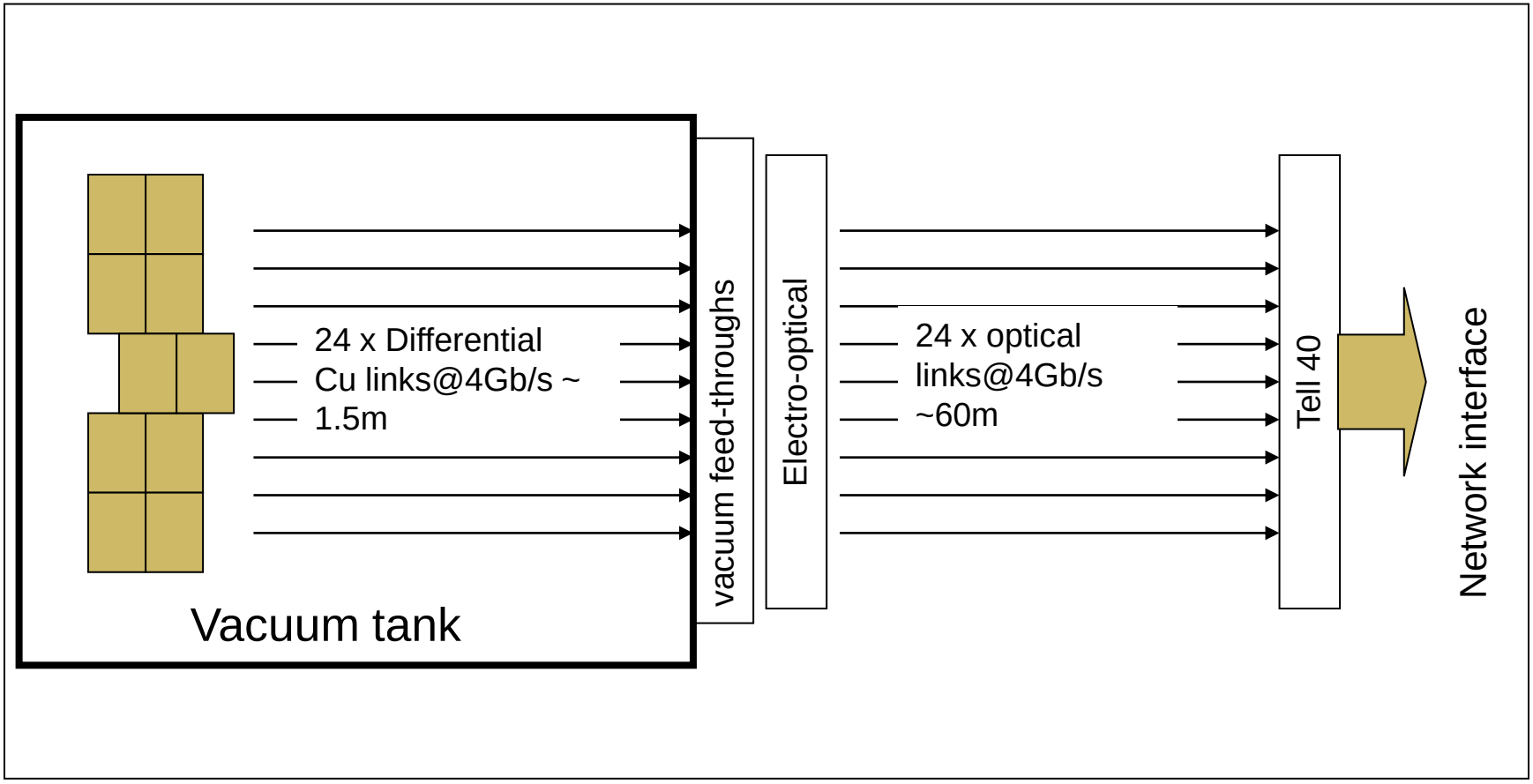
Simulations with Gauss/Boole data

Column	Efficiency (only missing packets)*	Efficiency (correct packets)	FIFO buffer size, # words, header/data	Avg. data rate, Mbps	Proportional and absolute area of FIFO
28	99.150 %	98.916 %	3/9	241.450	
28	89.816 %	88.906 %	4/8	218.606	
28	99.264 %	99.120 %	4/9	241.748	
28	99.341 %	99.192 %	4/10	241.924	14.7 %, 16612 um²
28	99.395 %	99.264 %	4/11	242.050	
28	99.407 %	99.276 %	4/12	242.072	15.7%, 18000 um²
28	99.413 %	99.282 %	4/14	242.089	
28	99.401 %	99.240 %	5/10	242.057	
28	99.497 %	99.383 %	5/12	242.303	
28	99.563 %	99.473 %	6/12	242.458	
28	99.677 %	99.623 %	8/16	242.723	
28	99.731 %	99.695 %	10/20	242.863	
28	99.749 %	99.719 %	12/24	242.908	
28	99.77 %	99.74 %	16/32	242.97	

More simulations still needed. Investigate margins.

Copper/optical cabling.

1 half station readout slice



Tell 40 issues.

- Number of Tell40's required:
  - Assume Tell40 will use 4 input mezzanines with
    - 24 input links/mezzanine. => total 96 input data links.
    - Output links ? 24 ?
  - 1 VELOpix half-station:
    - (2 sensor tiles) x (6 asics/tile) x (4 links/asic) = 48 output data links.
  - We will need 2 (left & right) x 23 (half-stations per side)= 46 x Tell40 units (with 48 input and 48 output links).
- Possible tasks in Tell40:
  - Re-order the VELOpix packets in time ?
    - VELOpix produce non-time-ordered packets.
  - Aggregate the packets from the same event :
    - Group clusters with same time identification.
    - Remove redundant time-id (12bit) ?
    - less packets , reduced network traffic.
  - Perform correct clustering:
    - 'Superpixel cluster' may contain 2 or more clusters : split ?
    - Combine clusters in 'row dimension' ? VELOpix cannot combine across superpixel in row direction.
  - Correct data per pixel for gain and offset non-uniformity ?
  - Compute a cluster center position ?
    - Reduces data a lot !
    - Reformat (total charge, position) ?
    - Eta-weighted interpolation: non trivial ! Also, don't know the track angle !
  - Add alignement ?
    - Save CPU time ?
- The Tell40 will also provide the configuration and fast control signals (GBT-SCA).