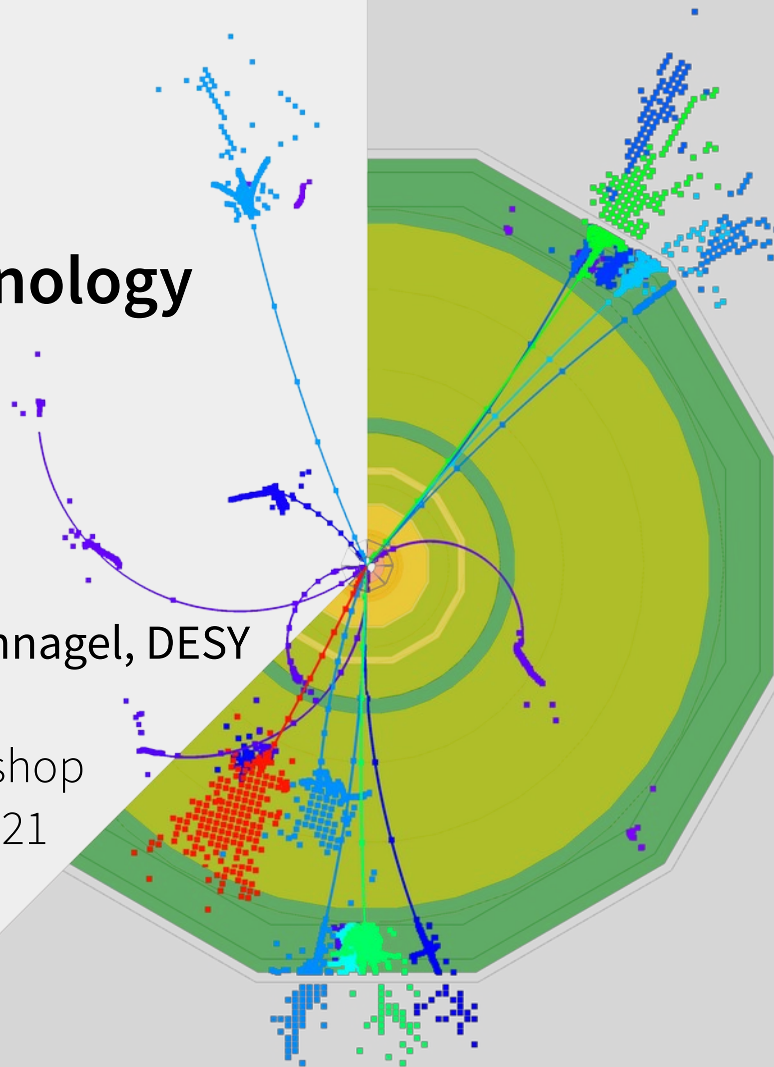
https://www.desy.de/

New Developments in Tracking Detector Technology



Simon Spannagel, DESY

International Workshop
on Future Linear Colliders 2021

17 March 2021

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

Tracking Detector Requirements at a Lepton Collider

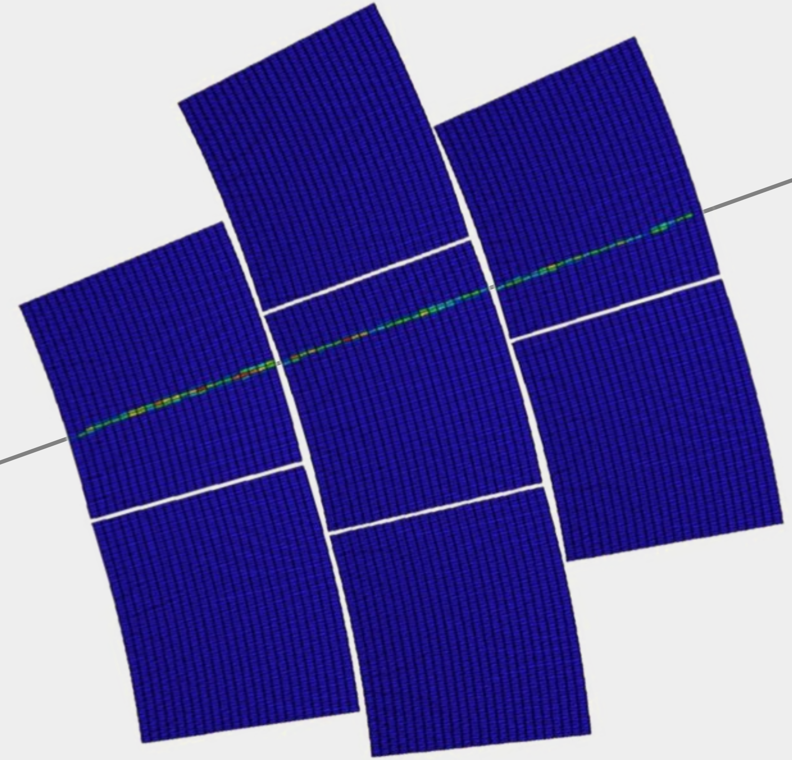
- Precision measurements especially demanding on vertex & tracking detectors
  - Momentum resolution – large lever arm, minimum scattering
  - Impact parameter resolution – high resolution, minimum scattering

- Physics studies for lepton colliders provide guidelines:

	Lepton Collider	(HL-) LHC (ATLAS/CMS)
Material budget	< 1% X_0	10% X_0
Single-point resolution	≤ 3 µm	~ 15 µm
Time resolution	~ ns	25 ns
Granularity	≤ 25 µm x 25 µm	50 µm x 50 µm
Radiation tolerance	< 10^{11} n_{eq} / cm^2	O(10^{16} n_{eq} / cm^2)

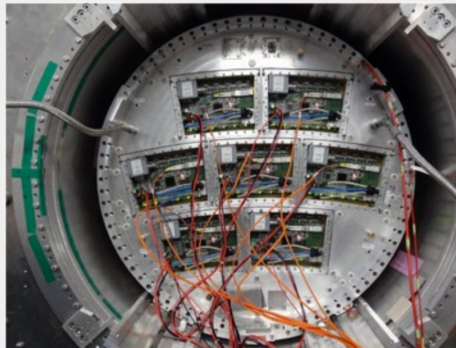
→ New experimental conditions: unique chance to rethink vertex & tracking detectors

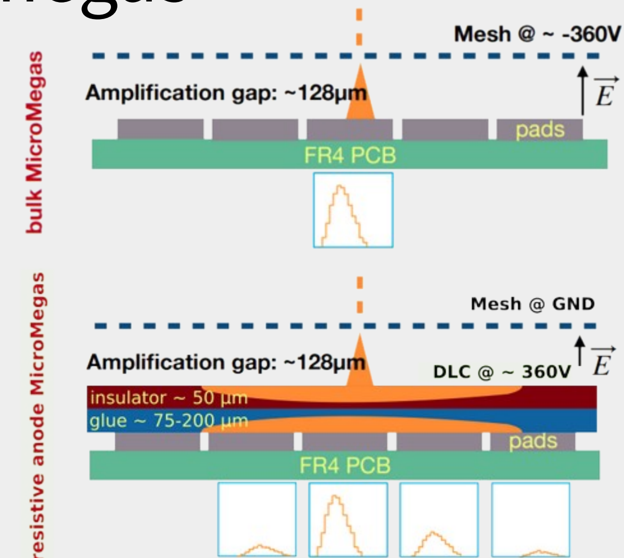
TPC Developments
for Readout & Characterization

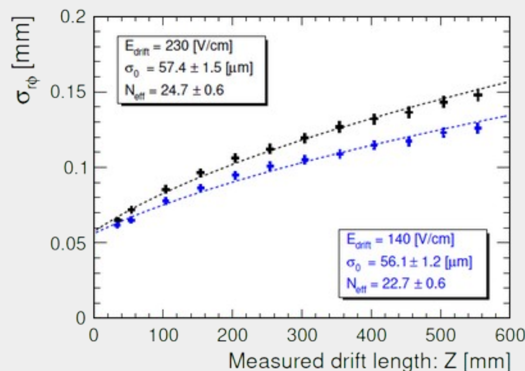


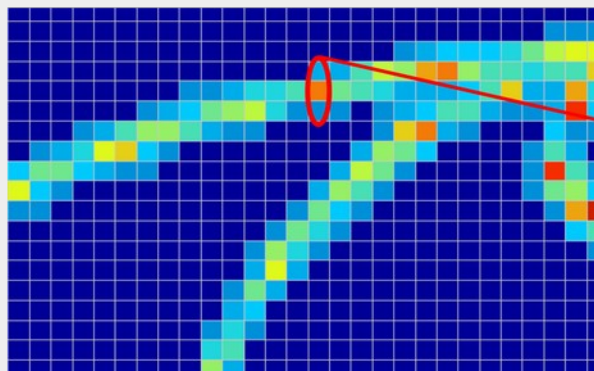
Encapsulated Resistive Anode bulk Micromegas

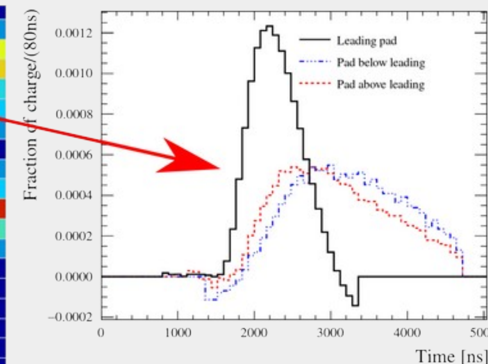
- Addition of resistive & insulating layers
  - Spreading of signal over multiple pads
  - Spatial resolution improvement
- New HV scheme: place grid on ground,
  Significantly reduces distortions @ module boundaries
- Study of charge spreading parameters ongoing
  (resistivity, glue thickness, gain, pad size, …)





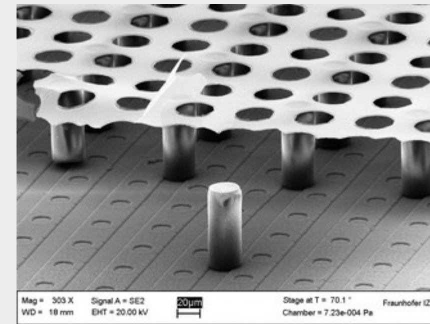
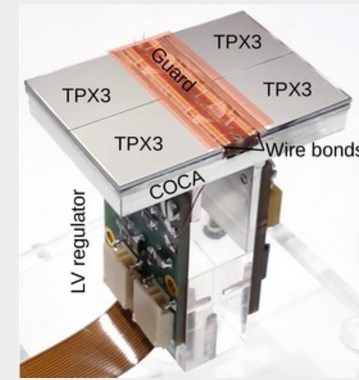




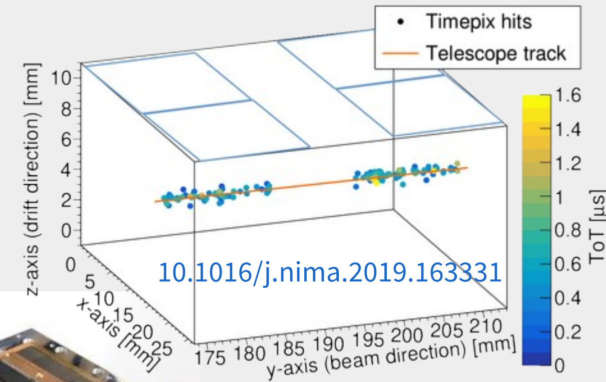


GridPix Developments

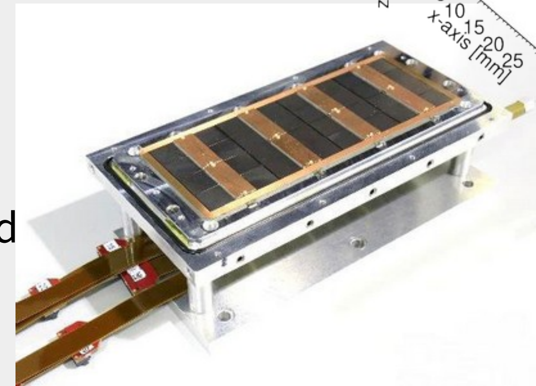
- Use bump bond pads of ASIC as charge collection pads, place micromegas grid directly on chip

- New generation of GridPix with Timepix3 ASIC
  - Faster readout, better timing, possibility for timewalk correction
- Developed “quad” module at Nikhef,
  - Building block for larger TPC modules
  - Tested at ELSA with Mimosa26 telescope
- Work underway for 8-quad module (32 GridPix)
  - To be tested in beam in 2021, with magnetic field
  - Fill LCTPC module ~100 GridPix

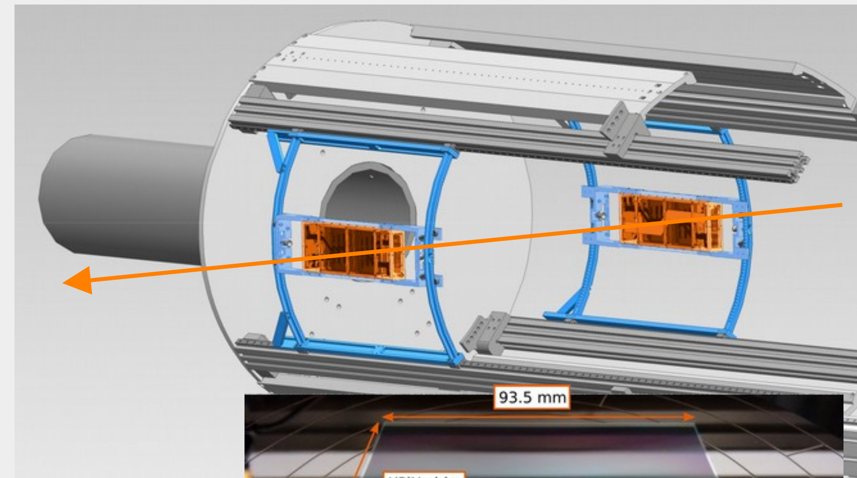


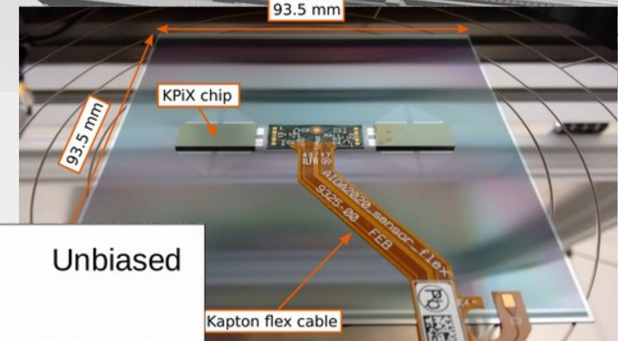
10.1016/j.nima.2019.163331

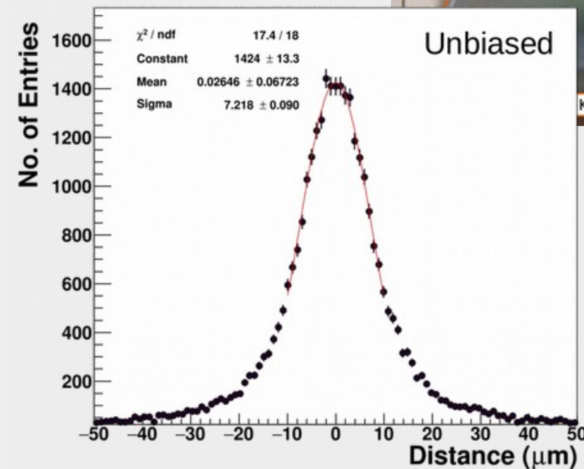


The LYCORIS Large Area Telescope

- Requirement for tracking in PCMAG
  - Momentum measurement for TPC prototypes
  - Study of distortions in Large Prototype
- Building tracking stations from KPix
  - Hybrid-less silicon strip sensor, integrated pitch adapter, digital readout
  - 10 cm x 10 cm sensor, thickness of 320 µm
  - Pitch of 25 µm, every 2nd strip read out
- Achieved ~7 µm resolution < 10 µm required



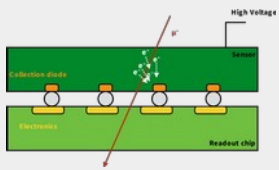




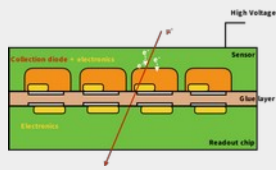
Talk by Uwe Krämer

Silicon Technologies

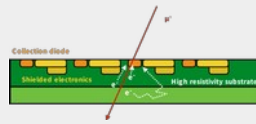
for Vertex & Tracking Detectors at Linear Colliders



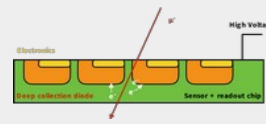
Hybrid



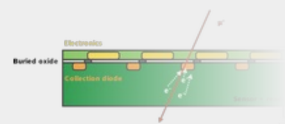
ACF



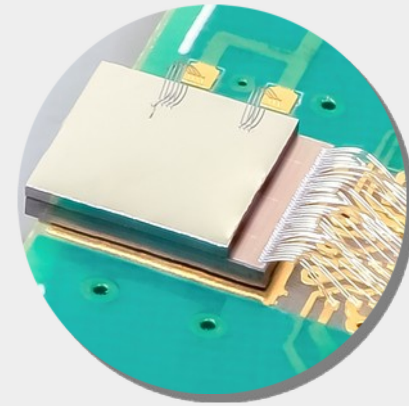
DMAPS



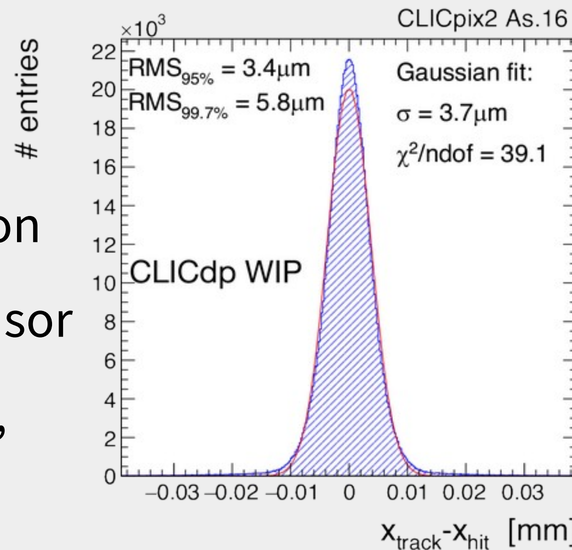
HV-CMOS

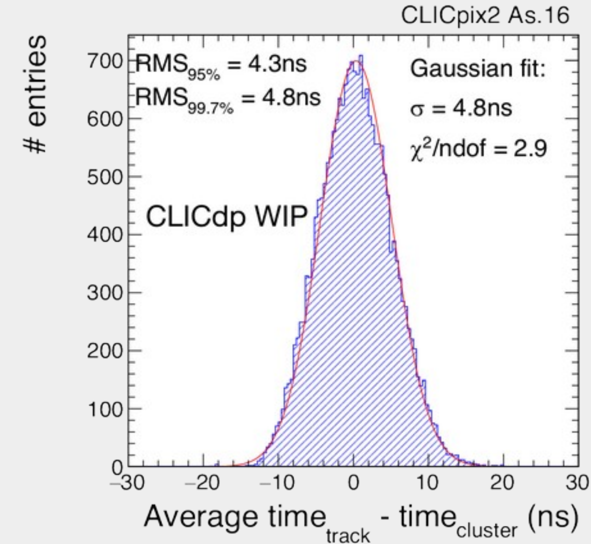


The CLICpix2 Hybrid Prototype



- Readout ASIC designed for CLIC vertex detector
  - Designed in 65nm CMOS process (same as RD53)
  - Matrix of 128 x 128 pixels with pitch of 25 x 25 µm
  - Simultaneous 5-bit ToT and 8-bit ToA
- Part of Timepix/Medipix family
- Very good position / time resolution
- Results achieved with 130 µm sensor
- Chip-level bump bonding difficult, limitation on pixel pitch

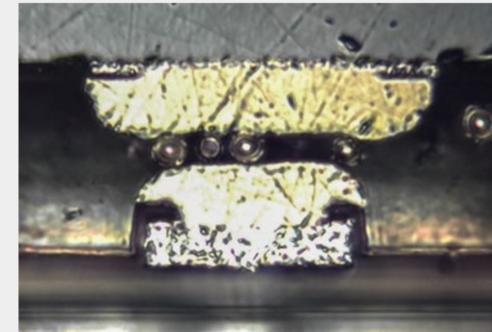




Anisotropic Conductive Film

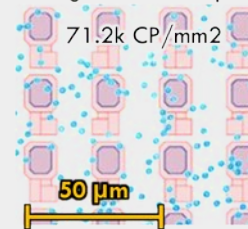
Talk by Mateus Vicente

- Overcome limitations of bump bonding: fine-pitch hybridization
  - Small (< 3 μm) conductive particles in glue film, stochastically distributed
  - Vertically compressed particles electrically connect bonding pads
- Used in industry (1D and larger bond surfaces)
- First successful Timepix3, limited by bonding pressure of machine
- Small pitch: requires aligned particles
- Also interesting for module integration
  - Alternative to wire bonding
  - Closer application to industry usage

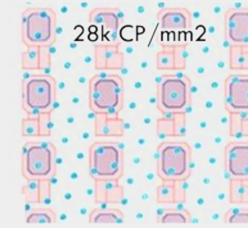


Timepix3-ACF-sensor cross-section

Currently available ACF
Minimum bonding area: 1000 μm²

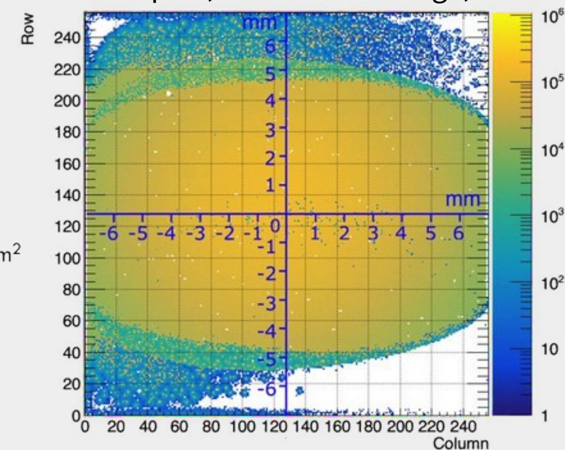


Particle aligned ACF
Minimum bonding area: 300 μm²



Picture of the ACF CPs (light blue) overlaid with the CLICpix2 pads (red) layout

Timepix3, 30% ACF coverage, Sr90

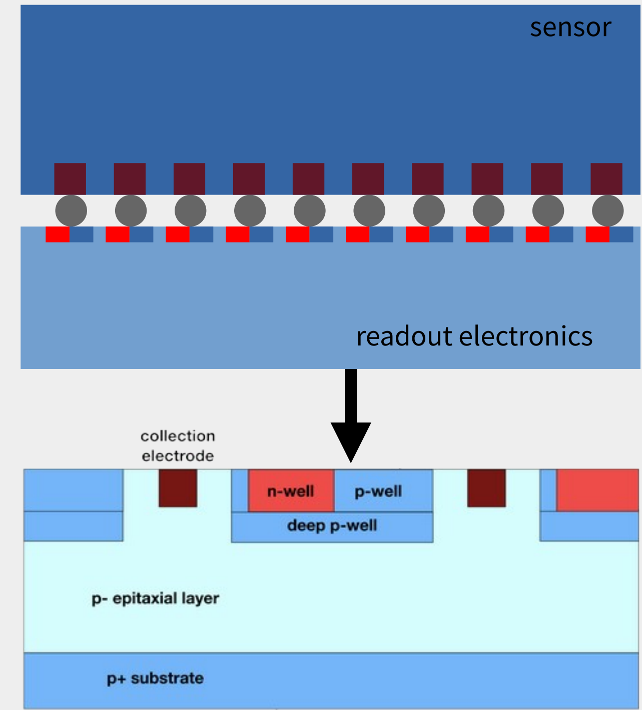


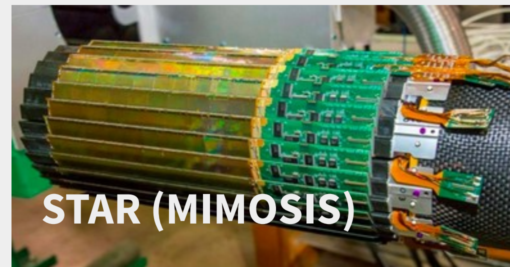
Monolithic Active Pixel Sensors

- **Hybridization** often limiting factor (cost, feature size)

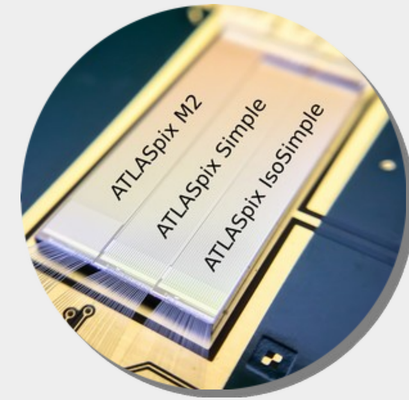
- MAPS **combine sensor & readout** in single wafer
  - Separation of electronics & sensor by deep wells
  - Signal from depleted high-resistivity (epitaxial) silicon
- Offer several **advantages** over hybrids:
  - Low capacitance (few fF) / high SNR designs possible
  - Drastic reduction of material budget
  - No bump-bonding, no limit on bonding pitch
  - Cost reduction for large systems

- First application in large-scale systems

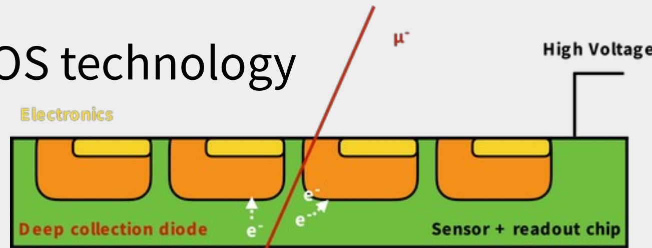




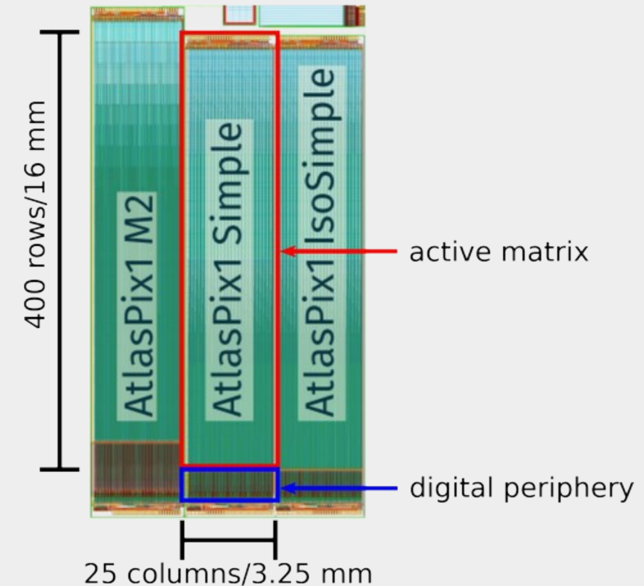
The ATLASpix HV-MAPS Prototype



- Designed for the ATLAS ITk upgrade & the CLIC tracking detector
  - 180 nm HV-CMOS technology



  - Matrix of 25 x 400 pixels with pitch of 130 x 40 μm^2
  - Self-triggered/continuous readout scheme
  - Energy + time measurement per pixel
  - Different substrate resistivities: 20, 80, 200 Ωcm
- Closely related to MuPix HV-MAPS for Mu3e experiment



Talk by Thomas Rudzki

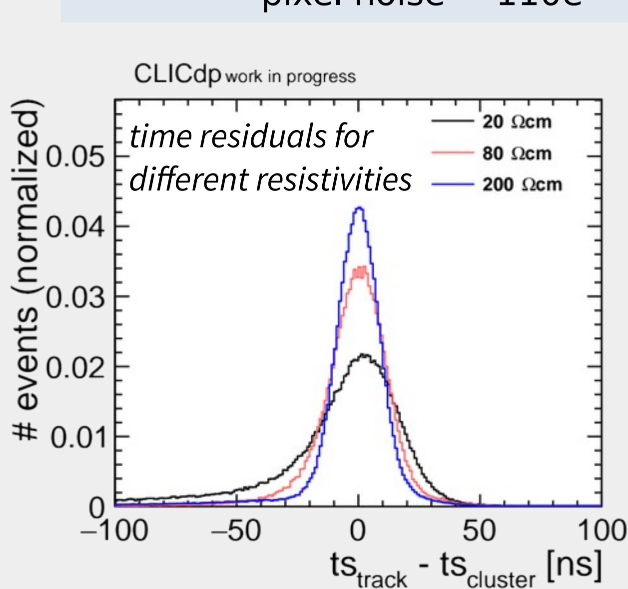
ATLASpix – latest results

lab characterization:

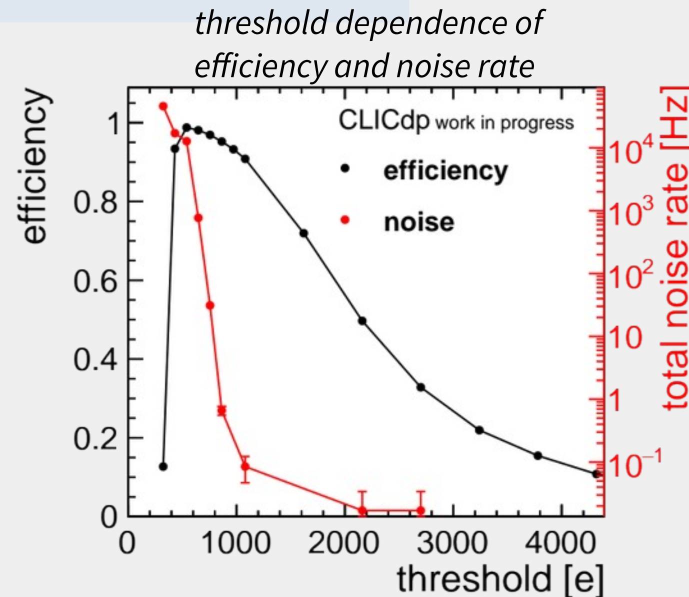
- noise rate < 10 kHz (full chip) = 1Hz (per pixel)
- X-ray calibration:
  (w/o equalization)
  - gain ~ 116 mV/1000e
  - threshold dispersion ~ 120e
  - pixel noise ~ 110e

test-beam characterization:

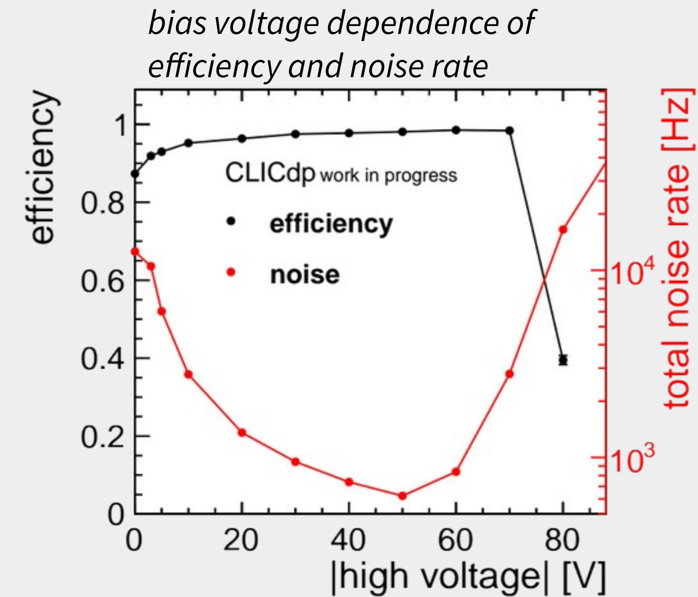
- binary spatial resolution
- timing resolution ~ 6.8ns
- efficiency > 99%
- substrate comparison:
  larger substrate resistivity:
  - faster timing
  - larger efficiency window



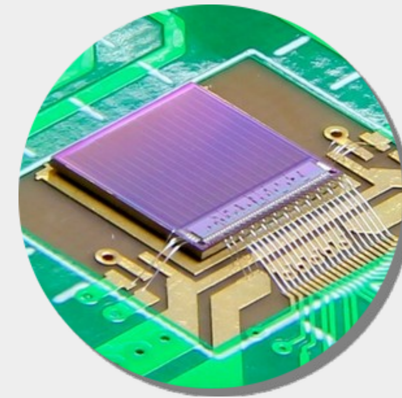
threshold dependence of efficiency and noise rate



bias voltage dependence of efficiency and noise rate



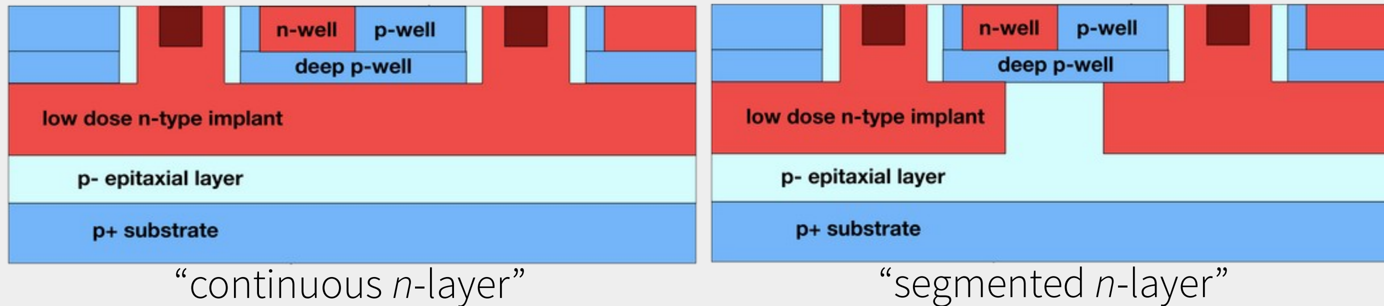
The CLICTD MAPS Prototype



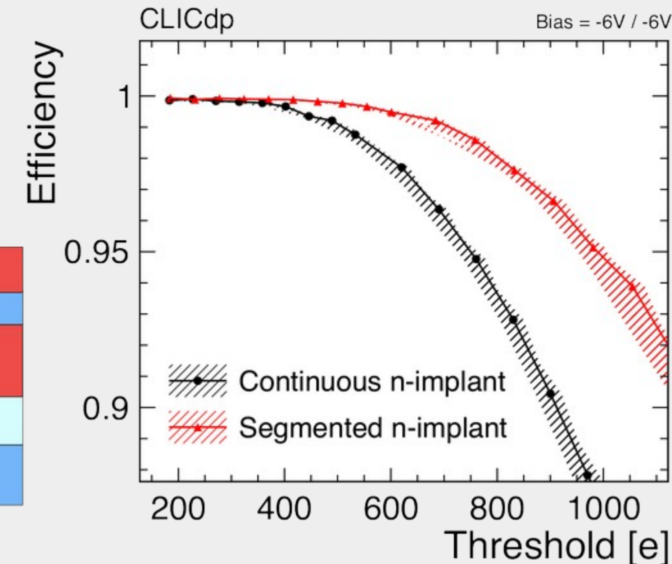
- Pixel detector designed for CLIC tracking detector
  - 180 nm commercial CMOS imaging process, small coll. electrode
  - Pixel pitch: 37.5 µm x 30 µm, 30 µm epitaxial layer
  - Fully-integrated sensors, simultaneous ToA/ToT measurement

Talk by Katharina Dort

- Field engineering important to control signal formation
- Test bench for testing different sensor designs:



"continuous *n*-layer" "segmented *n*-layer"

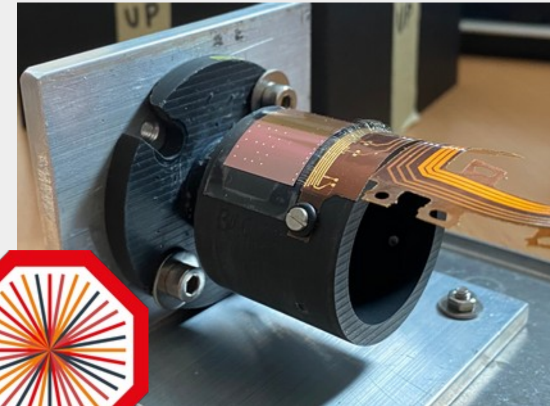


65 nm CMOS Imaging Technology

65nm

180nm

- MAPS design in **65 nm CMOS imaging process** – first application in HEP
  - Higher logic density → **reduced pixel pitch**
  - Lower analog/digital power consumption
  - Large 300 mm wafers
- International collaboration for common submissions to foundry
- Goal: explore new technology in terms of
  - Scalability — wafer-scale sensors through stitching
  - Timing resolution — through sensor engineering
  - Position resolution — through increased granularity



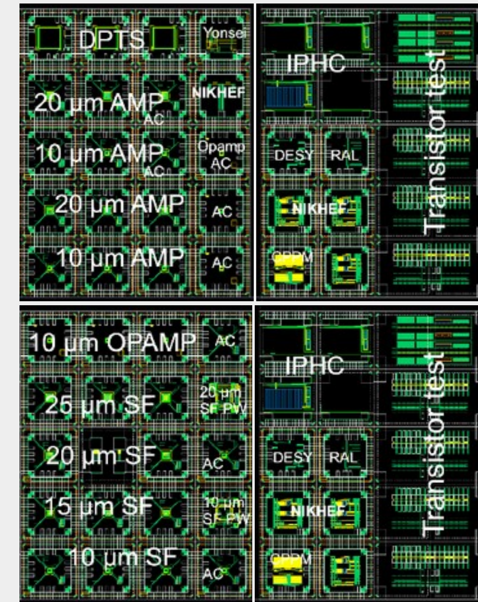
ALICE

Talk by Magnus Mager

Science & Technology Facilities Council
Rutherford Appleton Laboratory

65 nm CMOS Imaging Technology (II)

- Common design effort for first prototypes & test structures
  - Transistor test structures, analog/digital test pixels
  - Pixel test matrices with rolling shutter / analog readout
  - Front-end amplifier w/ Krummenacher feedback
- Designs submitted to foundry as MLR in 12/2020
  - Expected back summer 2021, testing preparation ongoing



Talk by Auguste Besson

- The *Tangerine* Project – Towards Next Generation Silicon Detectors
  - Developing new generation of MAPS, geared towards high position resolution
  - First prototype might be used for beam telescopes

Performance Goals for MAPS Sensor

- Position resolution ≤ 3 µm
- Timing resolution ~ 1 – 10 ns
- Material budget ~50 µm
- Charge measurement for interpolation

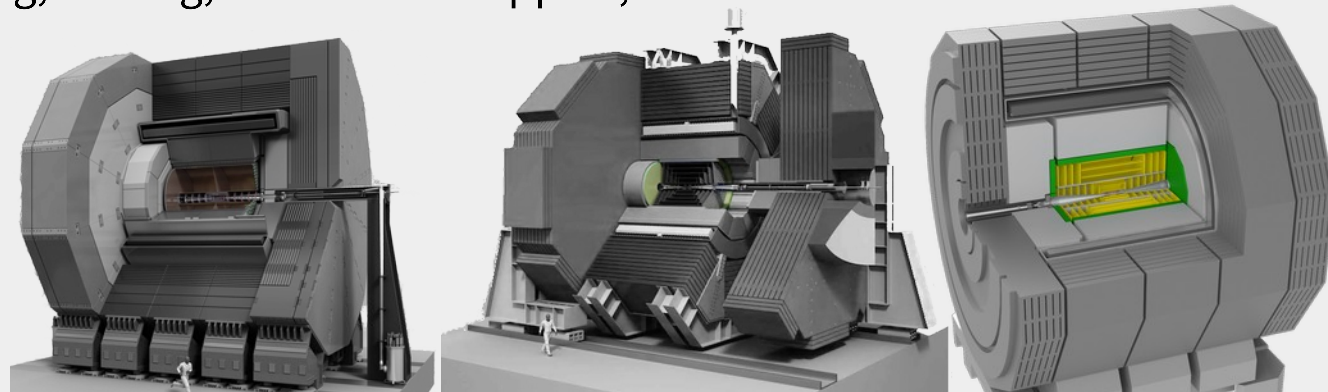
Summary

Summary

- Significant advances in tracking detector technologies
  - **TPC developments**: Resistive Micromegas, Timepix3 GridPix, LYCORIS telescope
  - **Silicon detectors:** Hybrids (CLICpix2, ACF), MAPS (CLICTD, ATLASpix, 65 nm)

- *“Snapshot of a selection”* – Many developments not covered here
  - Many sensor technologies under investigation   Gating GEMs, LGADs, RSDs, SOI, DEPFET, …
  - Technologies beyond sensors as important:
    data transmission, powering, cooling, mechanical support, …

- LC detector R&D continues to drive exploration of new detector technologies



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