Technology Developments on Thin iLGAD Sensors for Future Linear Colliders

International Workshop on Future Linear Colliders (LCWS 2021)

PD5: Tracking Detectors

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The RD50 iLGAD Project

Proof-of-concept and radiation tolerance assessment of thin pixelated Inverse Low Gain Avalanche Detectors (ILGAD)

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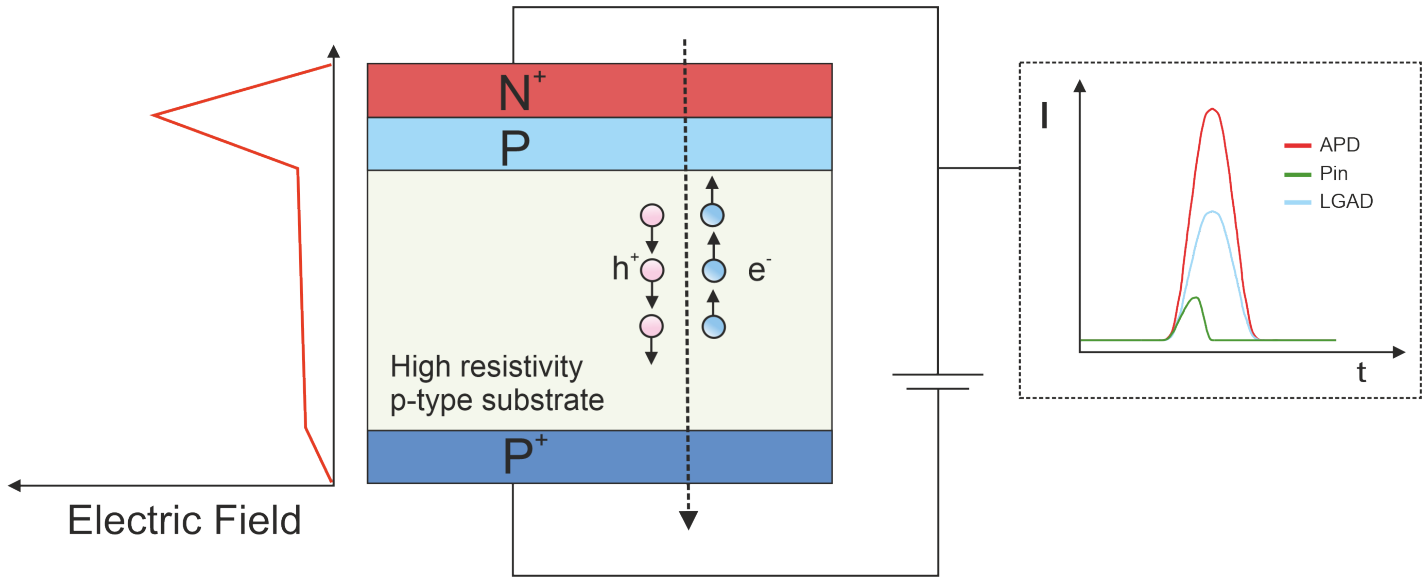
Outline of the Presentation

- Introduction: LGAD Technology
- Inverse LGAD as 4D Tracking Sensor
- First iLGAD Generation
- Inverse LGAD for Timing Applications
- Third iLGAD Generation (iLG3)
  - Trench iLGAD Concept
  - Fabrication Process
  - Mask Set Design
  - Work Plan
- Conclusion and future steps

Introduction: Low Gain Avalanche Detector (LGAD) Technology

- **LGAD** technology is based on the APD concept.
- Multiplication layer less doped to reach a **linear** and **moderate gain** (10-30) in a high operating voltage regime.
- **Low** signal to noise ratio **(S/N)**.
- **LGAD** is the baseline technology of the endcap MIP timing detector for the high-luminosity upgrade of the **ATLAS** and **CMS** experiments.



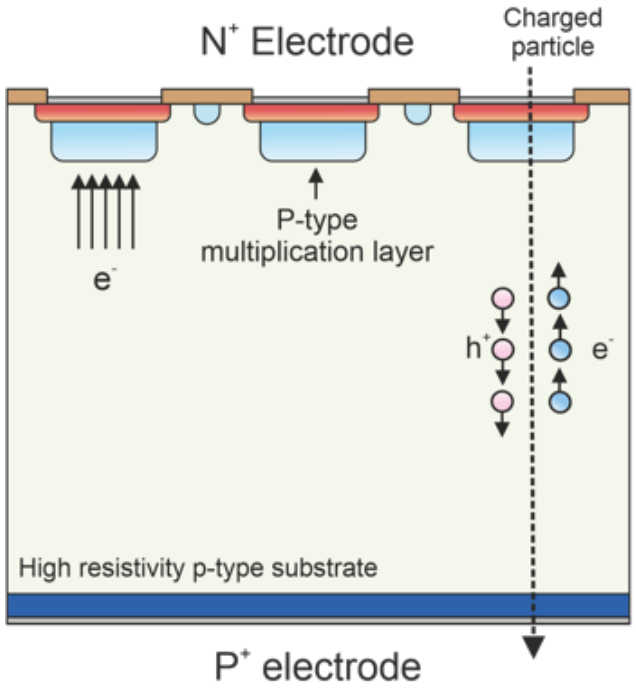
- **Main challenges:**
  - Radiation **tolerance to neutrons and protons.**
  - Technology **long-term reliability (Safe operating voltage).**
  - Large scale **manufacturing yield.**
  - Improve **fill-factor.** → **Motivation for the iLGAD**

Inverse LGAD as 4D Tracking Sensor

- Inverse Low Gain Avalanche Detector (iLGAD) is based on the LGAD technology.
- The main motivation for the iLGAD technology is **increase the fill factor** to a 100%.

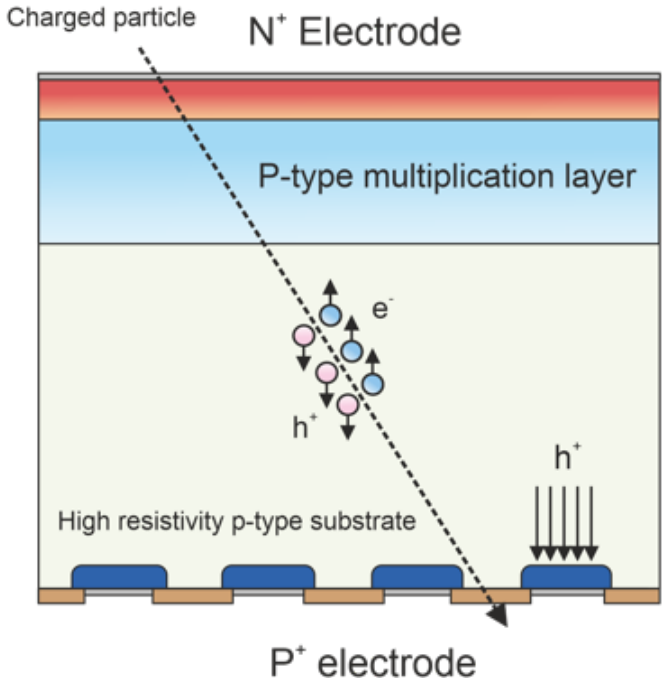
LGAD TECHNOLOGY

- Segmentation of the multiplication.
- Electron collection
- Single side process



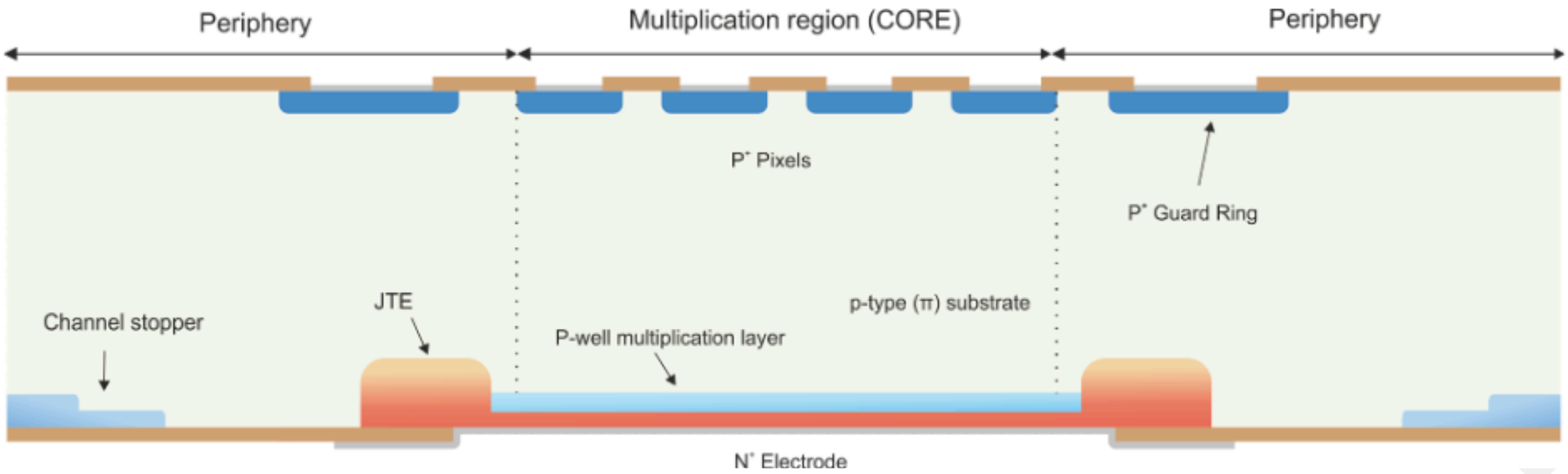
iLGAD TECHNOLOGY (iLG1)

- Multiplication extended over the electrode.
- Hole collection
- Complex double side process



iLGAD First Generation (iLG1)

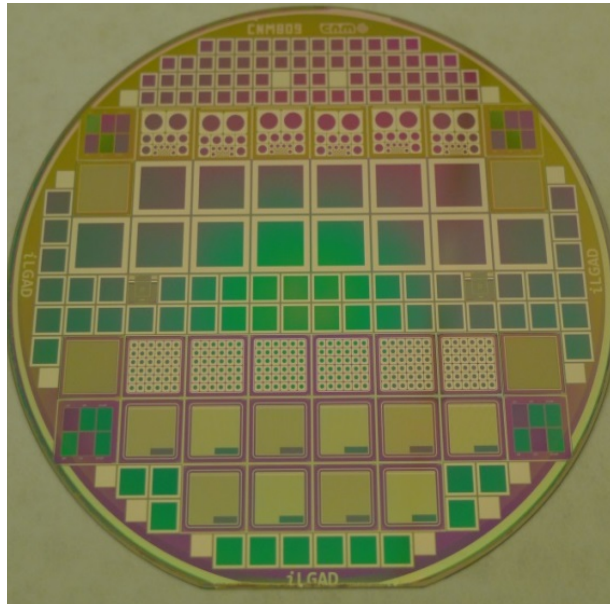
- Segmentation at the **ohmic contact**: strip and pixels.
- **Multiplication** extended over all the **CORE**.
- **P-type collector ring** at the ohmic side to extract leakage current.
- **JTE** to protect the n+/p curvature and **channel stopper** to avoid the depletion reaches the end of the detector.
- Readout is made by the strips/pixels: **holes collection**.



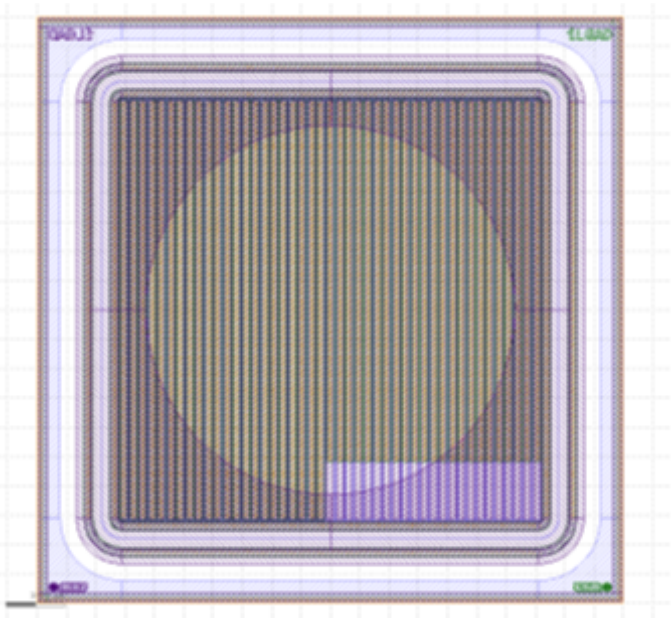
iLGAD First Generation (iLG1)

- 4-inch 285 µm p-type high resistivity wafers.
- More than 100 fabrication steps.
- 11 photolithographic steps: double side fabrication process.
- Pad-like, strip and pixelated detectors.

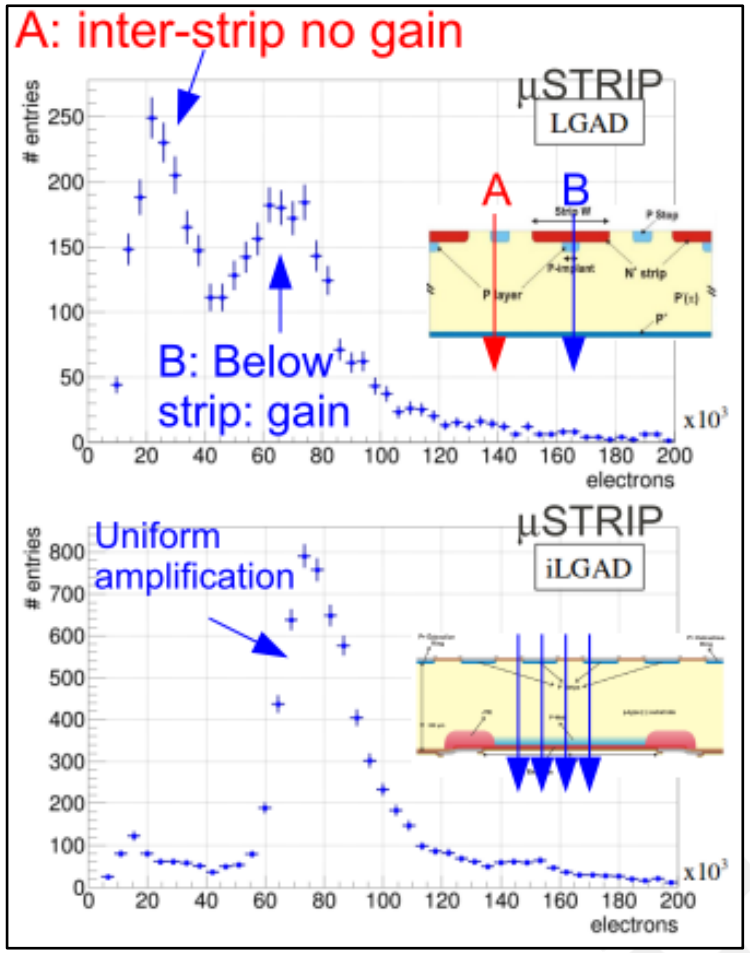
Mask design



µStrip iLGAD



Test Beam Irradiation



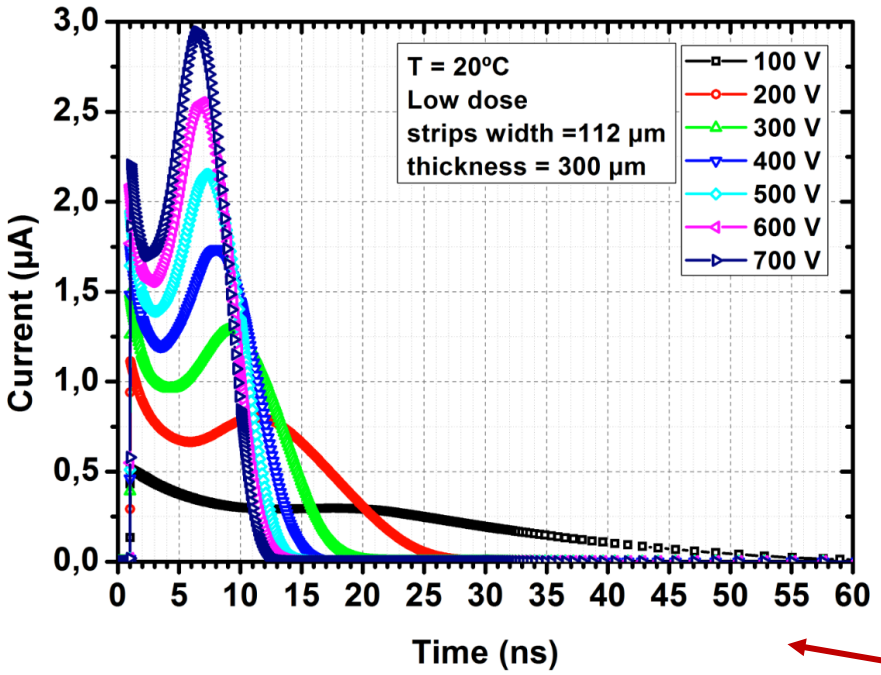
Currás, Esteban, et al. "Inverse Low Gain Avalanche Detectors (iLGADs) for precise tracking and timing applications." *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 958 (2020): 162545.

iLGAD for Timing Applications

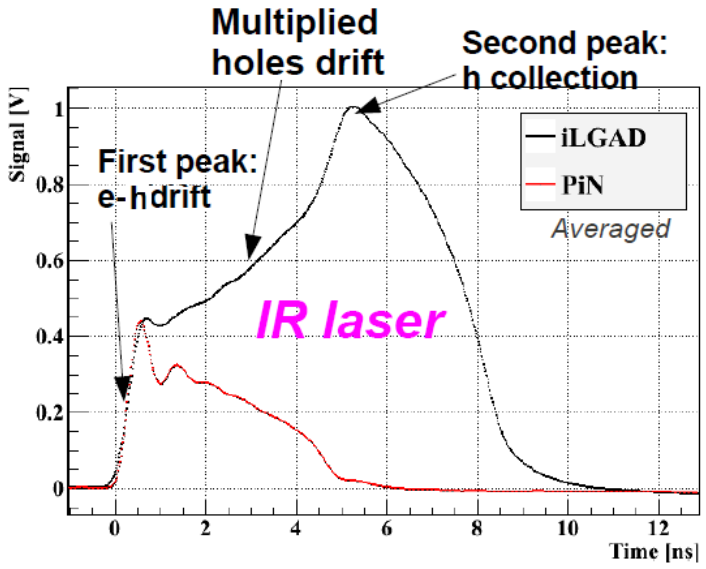
In order to use iLGADs for timing applications:

- Reduce the thickness of the detector to increase the electric field (at same voltage) in order that hole drift velocity reaches saturation.

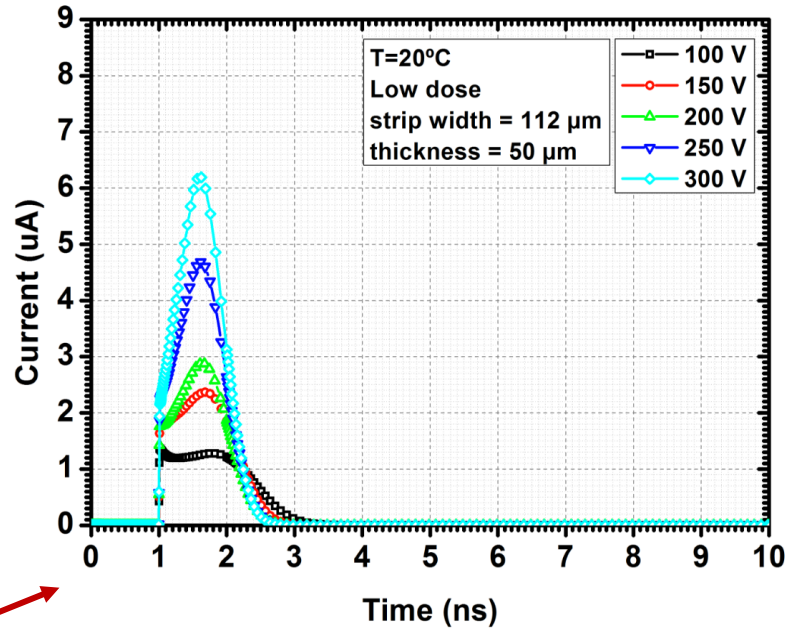
TCAD Simulation 300 µm thick iLGAD



Experimental 300 µm thick iLGAD



TCAD Simulation 50 µm thick iLGAD

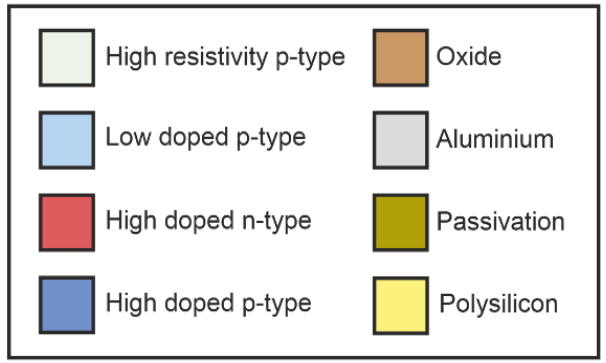


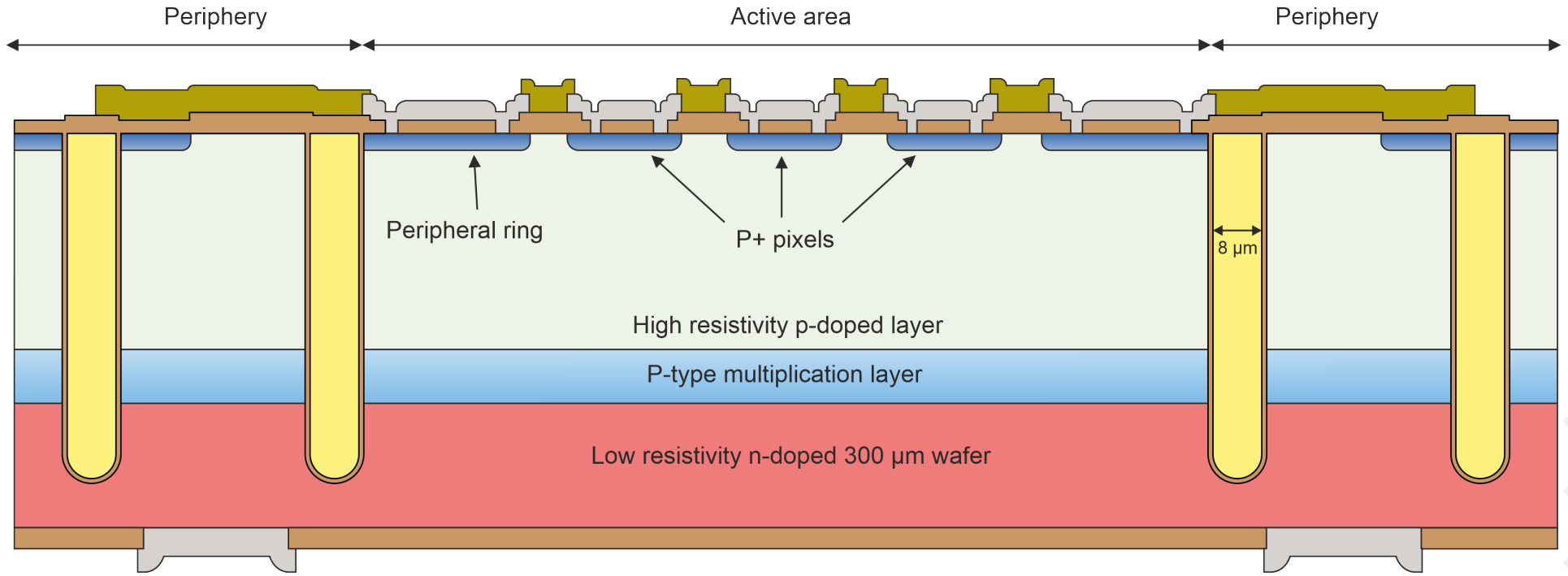
Different scale!

iLGAD Third Generation (iLG3): Trench iLGAD Concept

In the iLG3 we are going to use trenches to isolate the active area.

- ✓ **Multiplication region** is fully **isolated**.
- ✓ **Simpler single-side** and **50% less** fabrication steps.
- ✓ Devices are able to sustain **higher voltages.**
- ✓ **Slim-edge technology.**
- ✓ **Thin detectors.**
- ✓ Optimization of the **multiplication layer is independent of charge collection and cross-talk at the electrodes.**

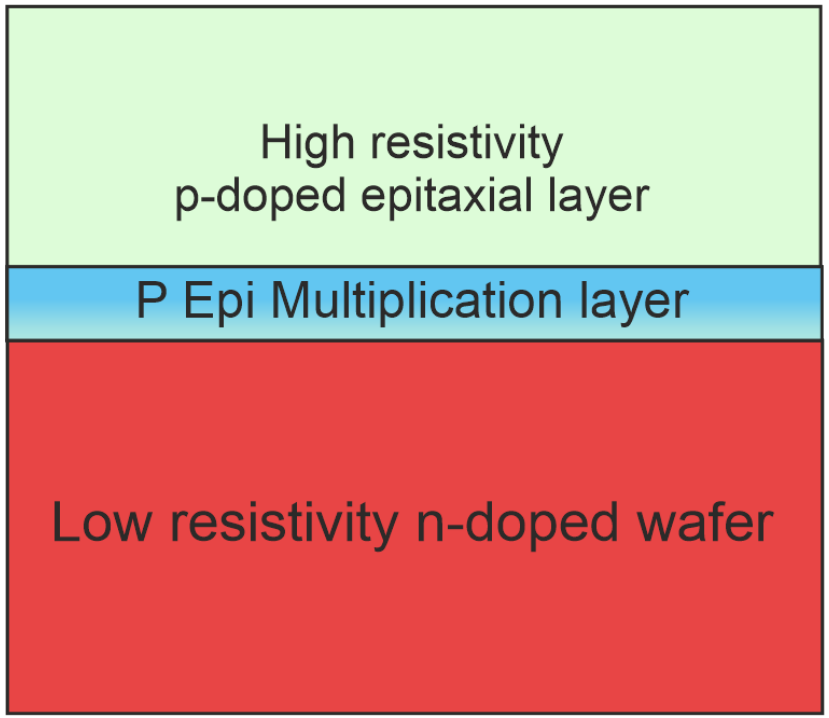




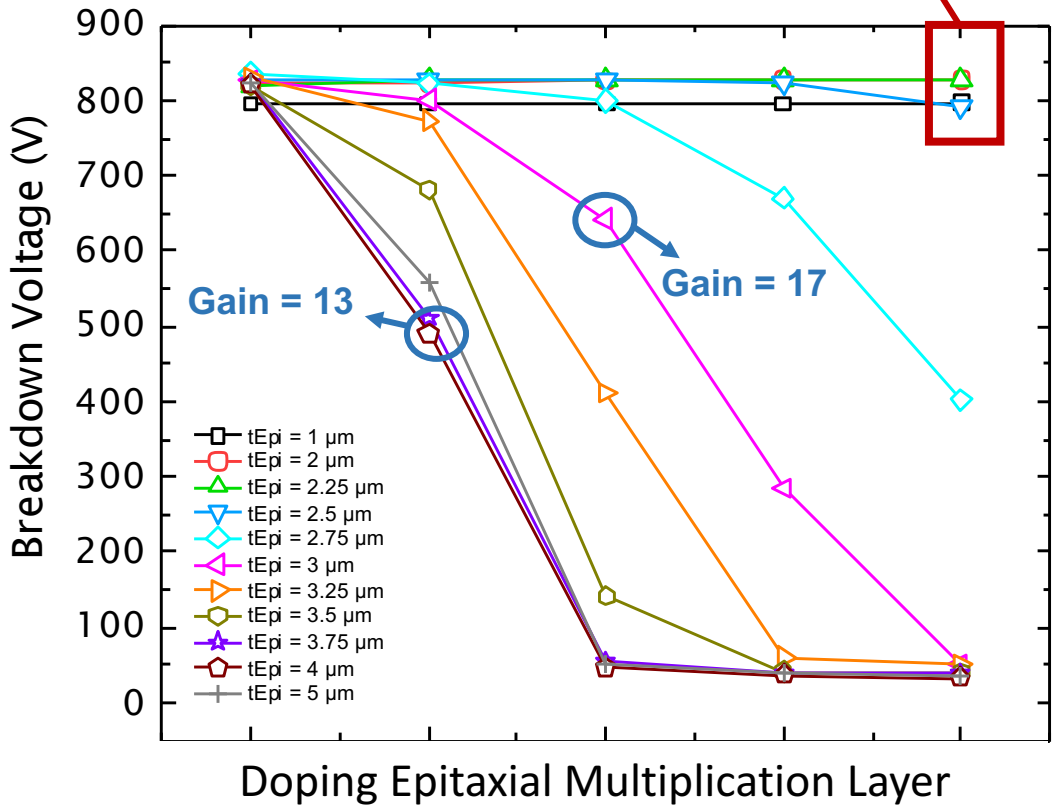
iLGAD Third Generation (iLG3): Fabrication Process

We are planning to carry out this fabrication with two different approaches:

1. **Epitaxial wafer + epitaxial multiplication**
2. Si-Si wafers + implanted multiplication



No gain layer due to diffusion of n-doped wafer to the epitaxial p-doped



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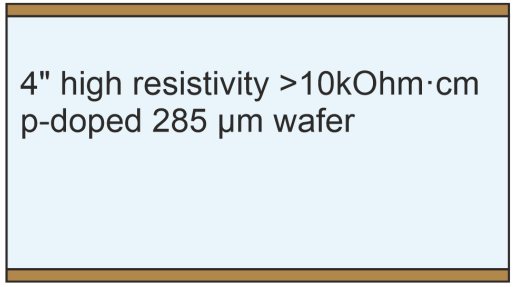
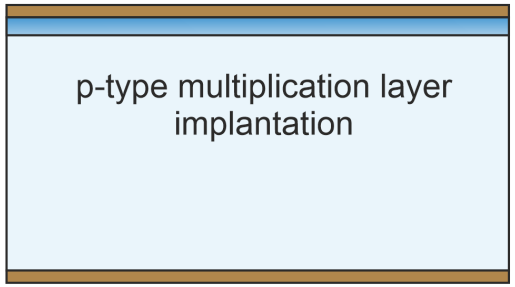
CNM

(1)



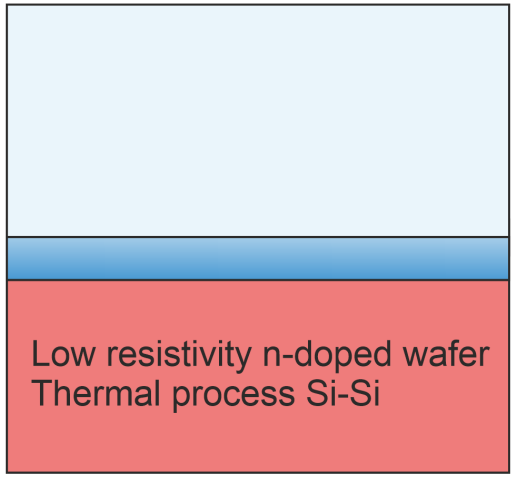
(2)



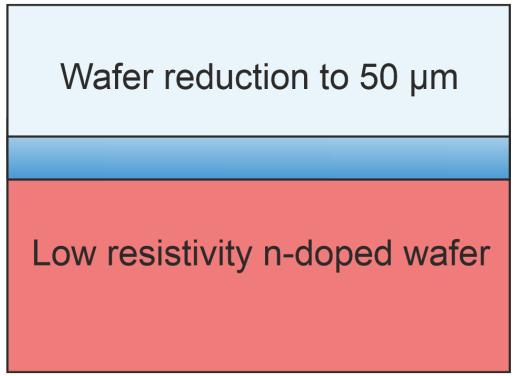
Dose/energy multiplication layer is adapted to the Si-Si thermal process

Foundry

(3)



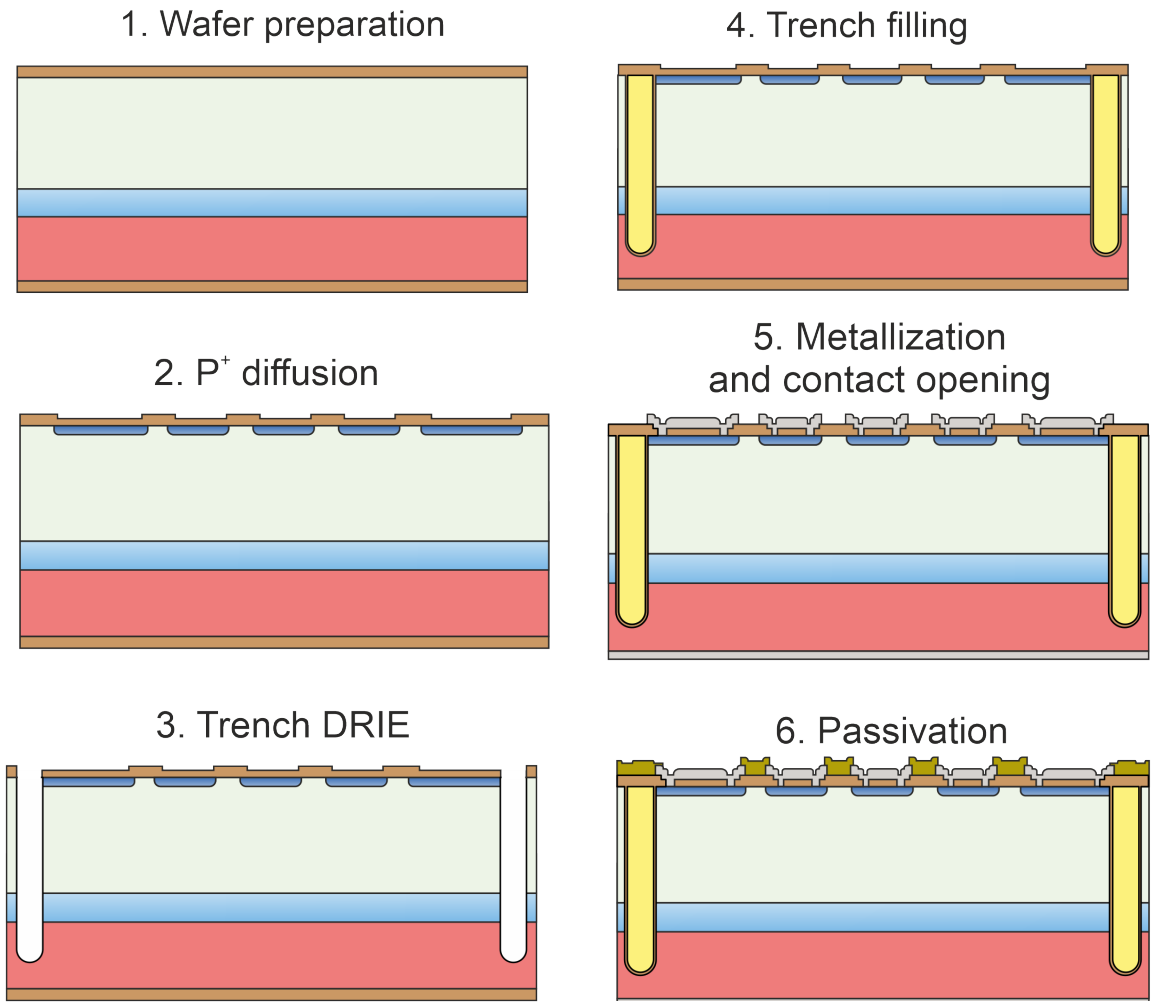
(4)



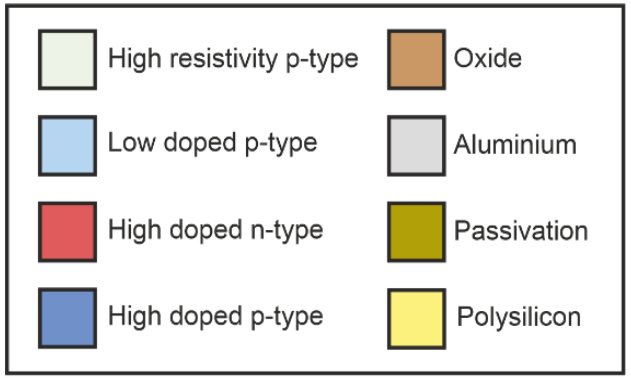
After (4), the profile is the same as standard LGAD runs. This is the starting point for the fabrication.

iLGAD Third Generation (iLG3): Fabrication Process

Trench iLGAD Fabrication Process



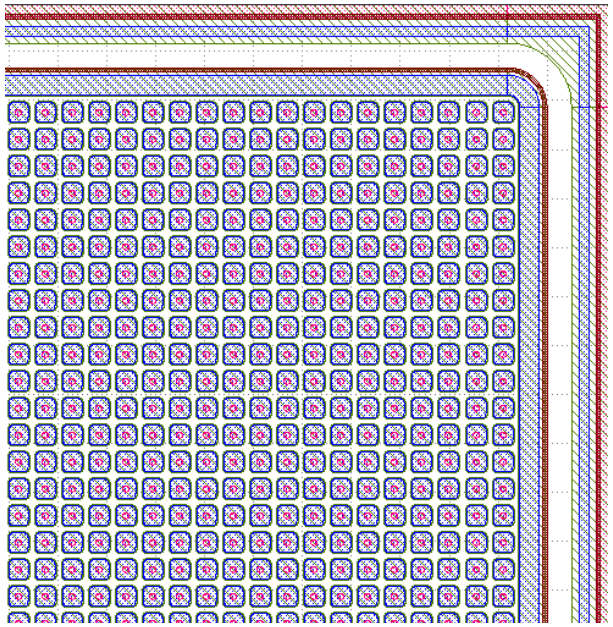
7 Photolithographic steps
~50 fabrication steps
Single-side process



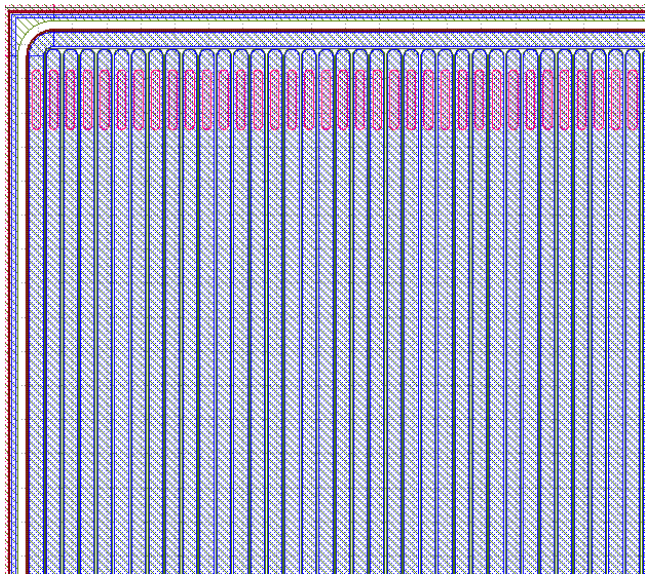
iLGAD Third Generation (iLG3): Mask Design

- **Timepix3**: 55x55 pitch, 256x256 pixels
- **TDCPix**: 300x300 pitch, 44x45 pixels
- **UZH-PSI**: 100x100 pitch, 30x30 pixels
- **iStrip**: 100x100 pitch, 75 strips

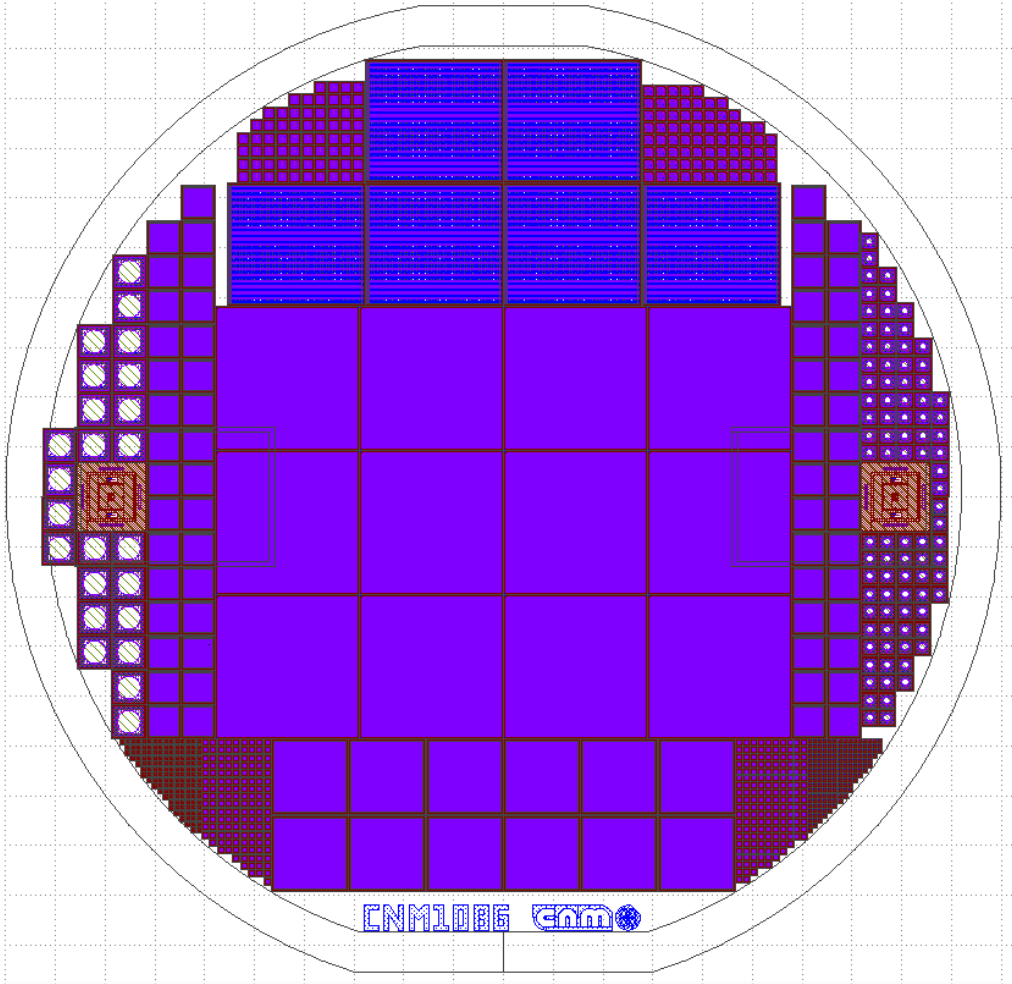
Timepix3



iStrip



Wafer layout



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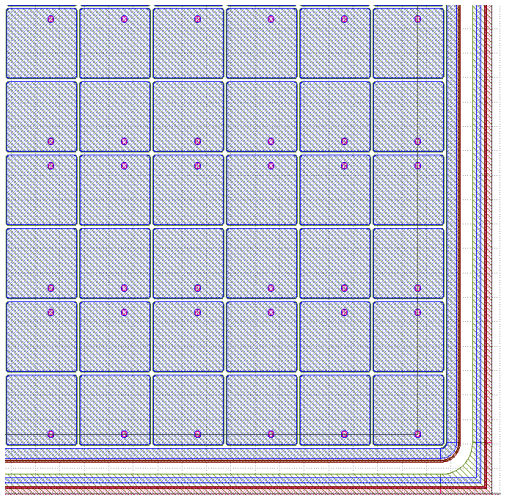
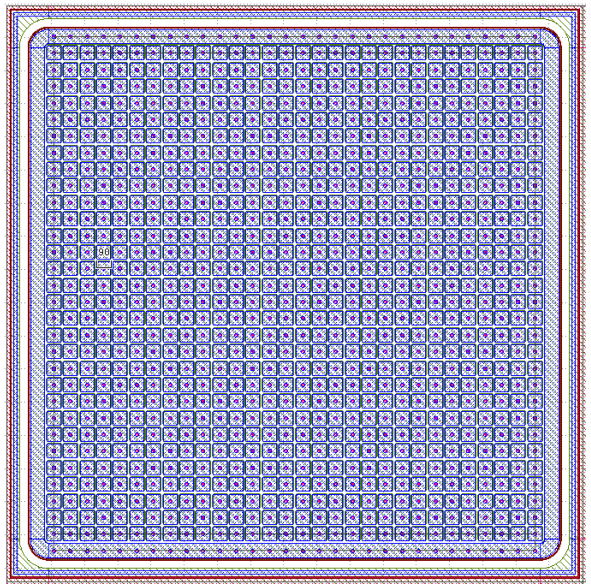
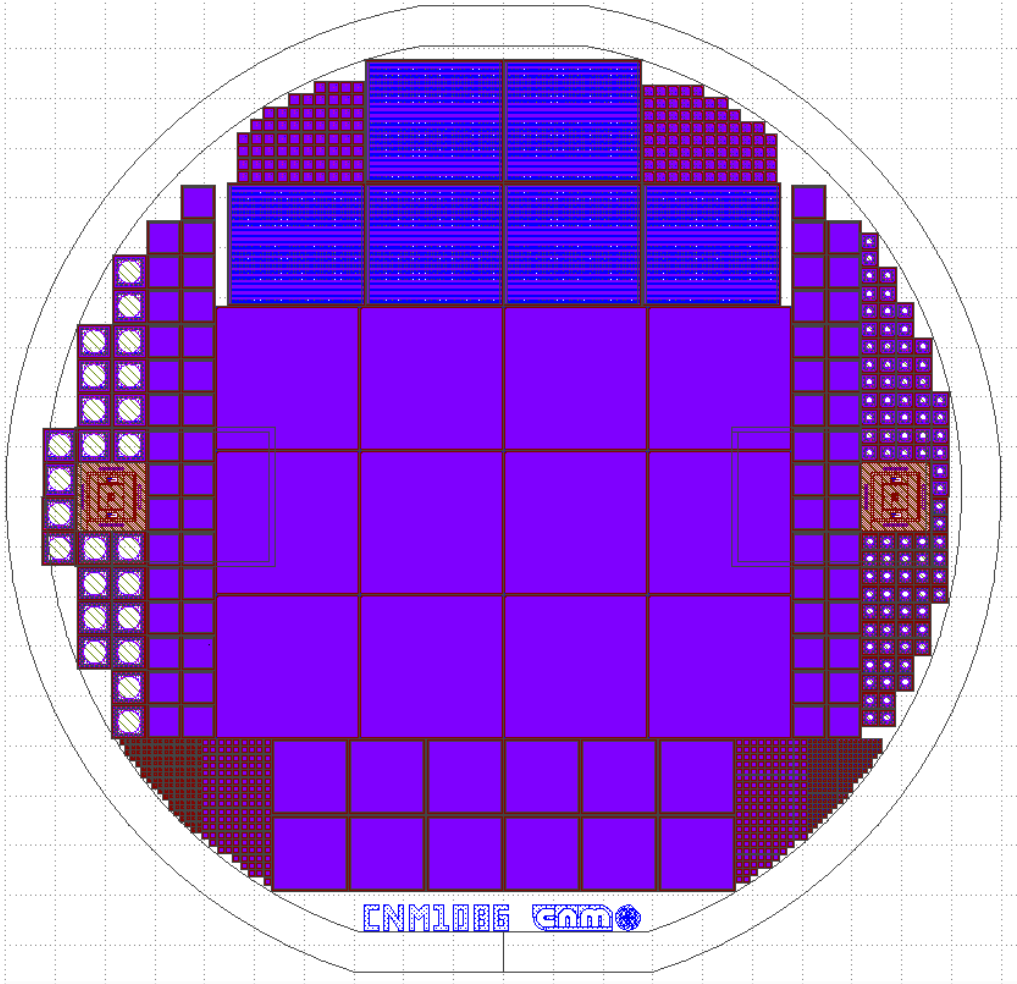
TDCPix



UZH-PSI



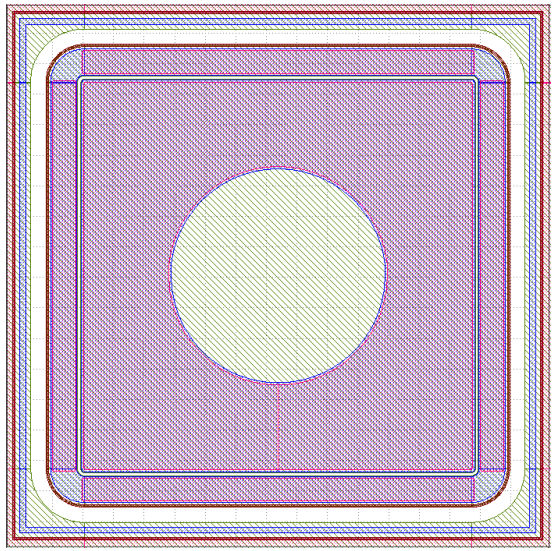
Wafer layout



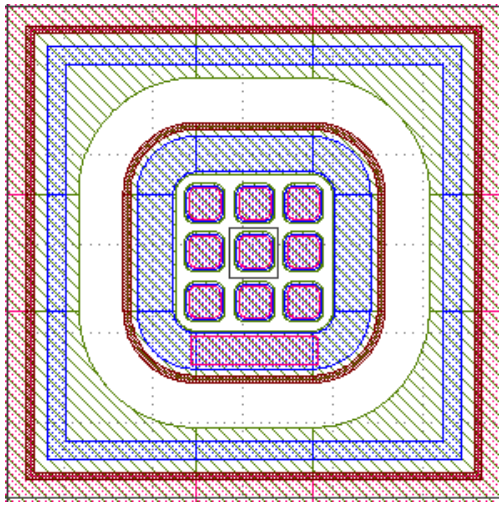
iLGAD Third Generation (iLG3): Mask Design

- Pad detectors
- MOS structures
- 3x3 Test structures

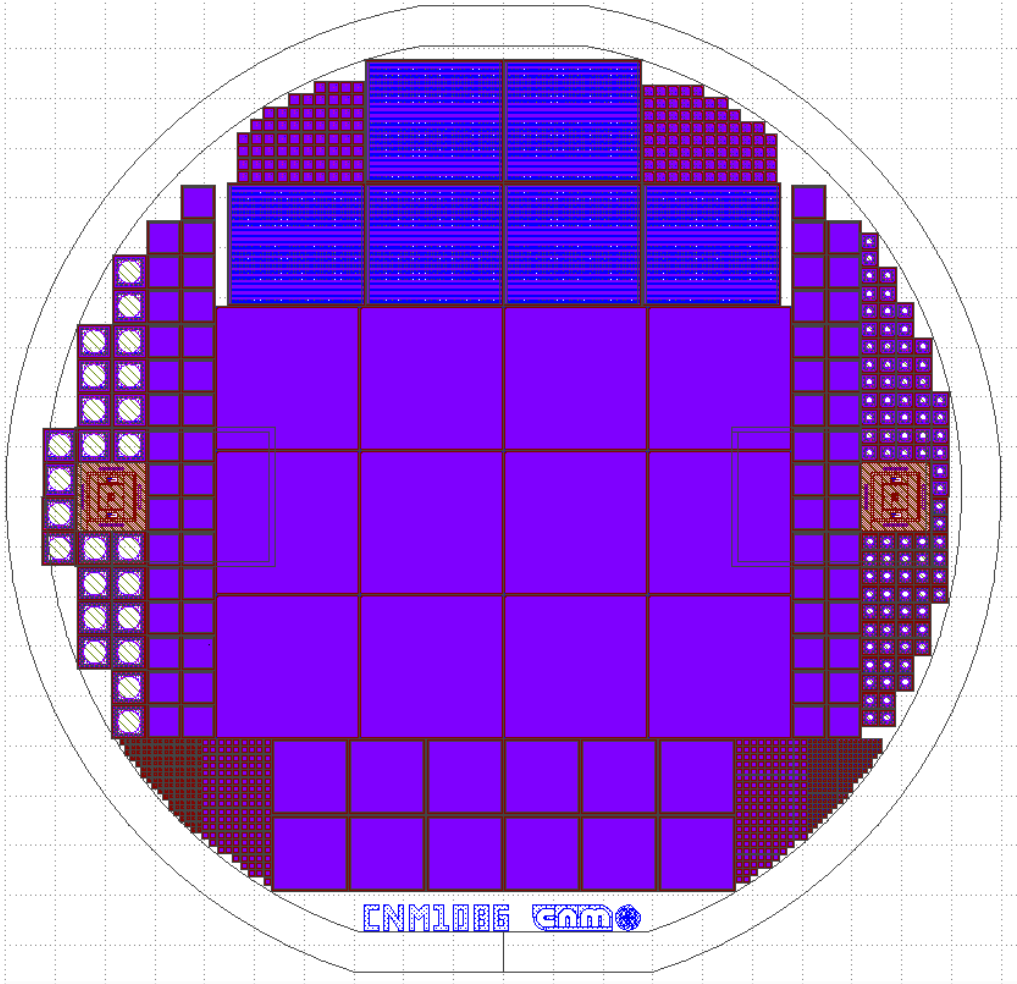
Pad Trench LGAD



3x3 T-iLGAD



Wafer layout



iLGAD Third Generation (iLG3): Work Plan

- Epitaxial and Si-Si Wafers are purchased and delivered
- Technological simulations are ready
- The process technology steps are ready
- We are designing the mask set
- Work Planning:
  - Mask Design
    - End of February 2021
  - Mask Fabrication
    - Mid-March 2021
  - Fabrication
    - Some clean room processes will not available until mid-April 2021
    - Fabrication will start at the end of April 2021
    - Fabrication will be completed by the end of September 2021

Conclusions and Future Work

- Inverse LGAD concept has been considered as 4D tracking sensor.
- First iLGAD generation (iLG1) has been successfully fabricated and show promising results.
- Third iLGAD generation (iLG3) has been described. We expect to use these sensors for timing applications.
- TCAD simulations has been performed to obtain a suitable periphery to sustain high voltages and reducing the fabrication time.
- Fabrication is going to be done with two different types of wafers: epitaxial and Si-Si wafers.
- Currently, we are drawing the mask set.
- The run will start by April 2021.
- By end of 2021, we will have the run fully characterized and samples will be distributed.

Thank you for your attention!