

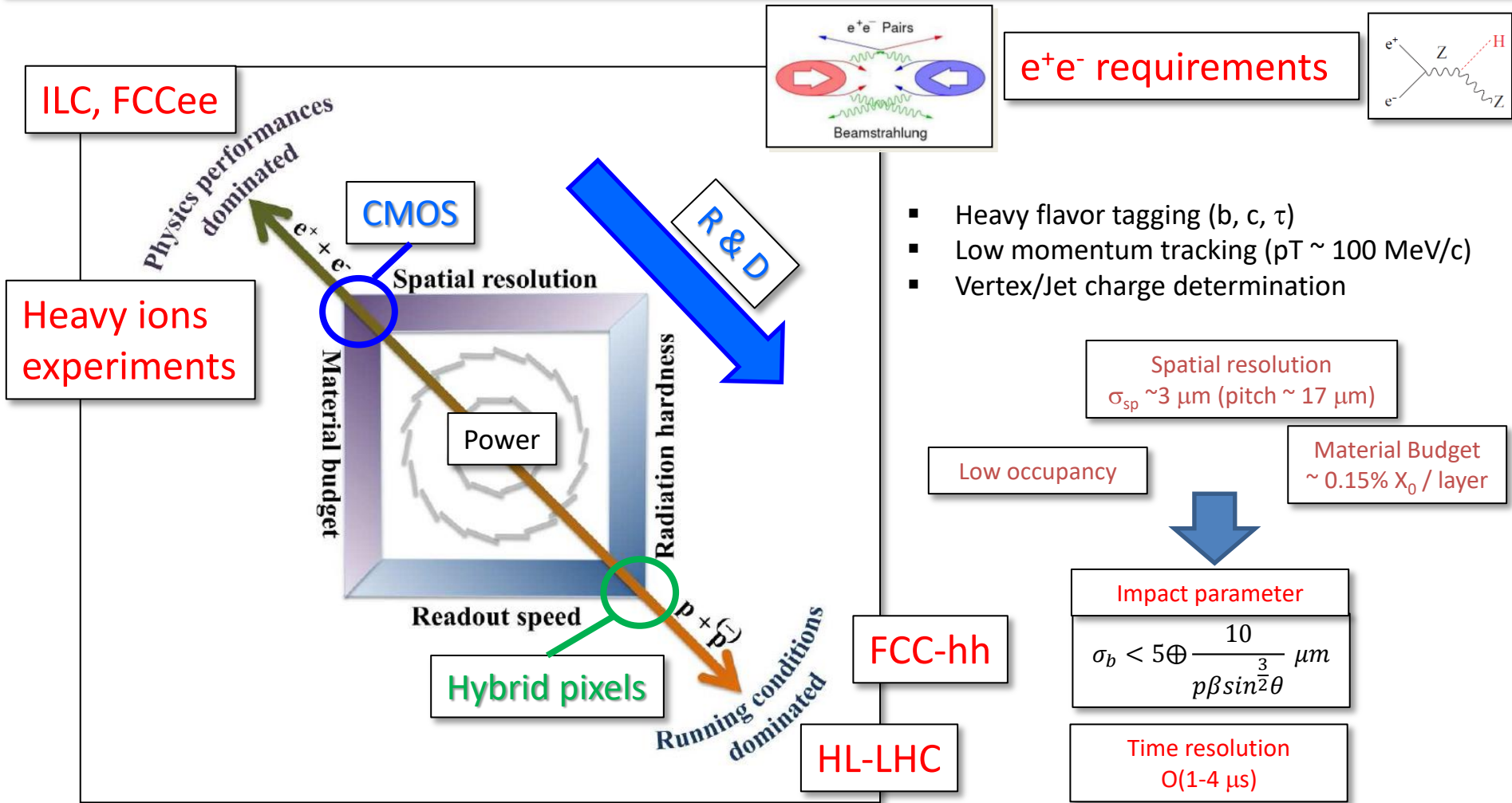
CMOS pixels sensors for the ILC vertex detector

Auguste Besson

On behalf of the PICSEL group & C4PI Platform
@IPHC - Strasbourg University

- MIMOSIS chip development
- 3D/SOI
- Stitching & bending
- 65 nm R&D

Vertex detector technology figure of merit



Challenge:

⇒ Keep excellent spatial resolution, low material budget, moderate Power consumption and push towards better time resolution (BX)

CPS @ IPHC (PICSEL & C4PI): on the road to Higgs factories



EUDET beam telescope
(Mimosa 26 by IPHC)
~ 15 copies since 2009

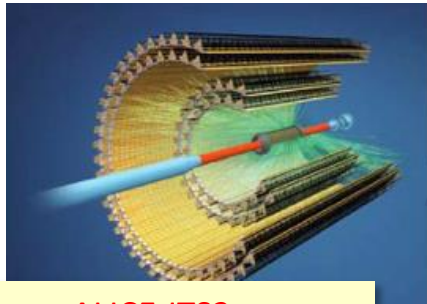
$O(100 \mu s)$

Process: 0.35 μm



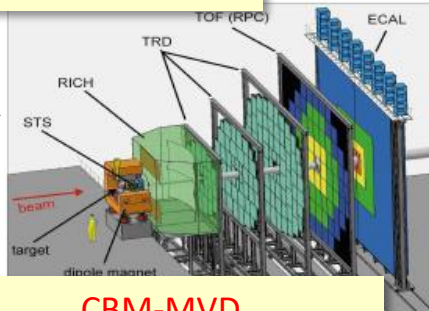
STAR-PXL detector
(ULTIMATE by IPHC)
2014-16

Process: 0.18 μm



ALICE-ITS2
(ALPIDE by CERN & IPHC)
In installation

$O(10 \mu s)$



CBM-MVD
(MIMOSIS by IPHC & IKF)
Under development



ILC VXD & inner tracker
R & D

$O(1 \mu s)$

Process: 65 nm ?

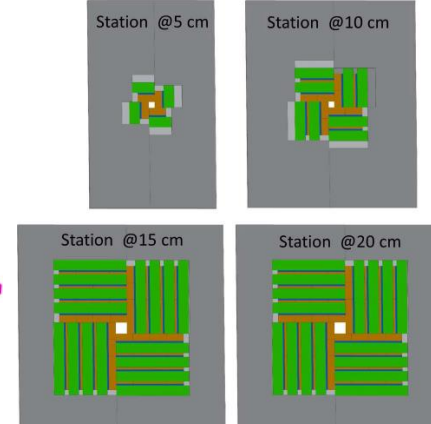
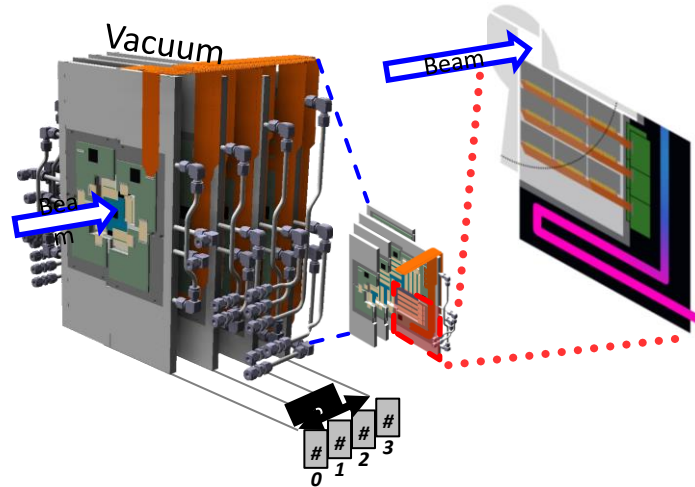
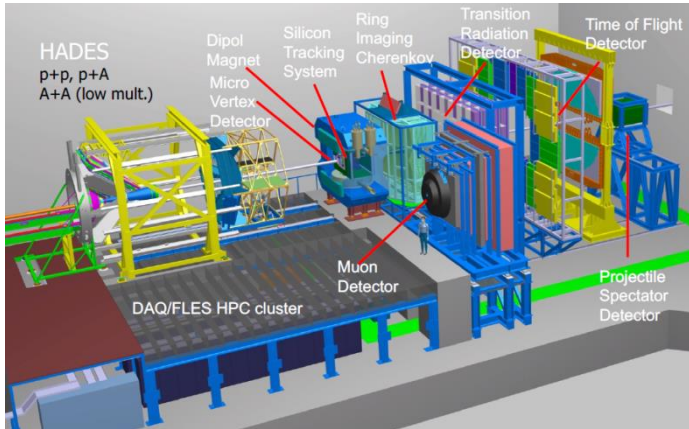
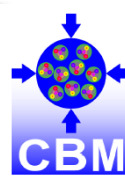
- IPHC: R&D started in ~1999
 - ✓ Take advantage of mid-term projects to get closer to ILC vertex detector requirements
- Today (\Rightarrow ~2023)
 - ✓ CBM-MVD: MIMOSIS chips



- ✓ 65 nm technology exploration

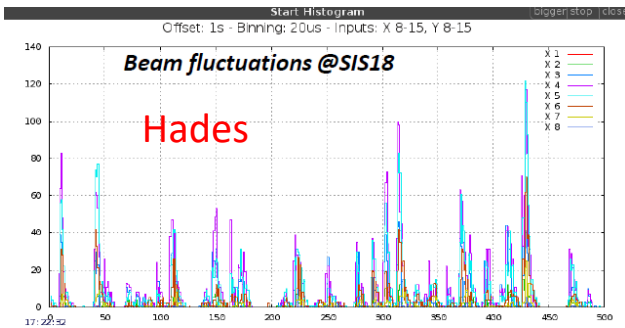
- Other activities:
 - ✓ Integration
 - ✓ SOI
 - ✓ Double-tier
 - ✓ Faster charge collection time

CBM-MVD @ FAIR



Joachim Stroth | 56th Winter Meeting on Nuclear Physics | Bormio (Italy)

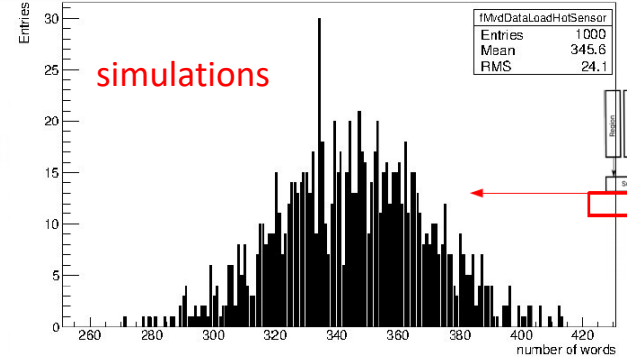
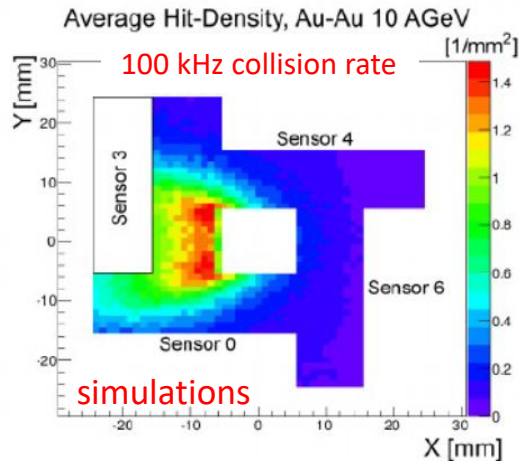
- Non uniform hit density in time and space
- High radiation environment



Michal Koziel | deutsche physikalische gesellschaft 2017 | Münster (Germany)

Au/Au 10 AGeV 100kHz

LCWS 2021

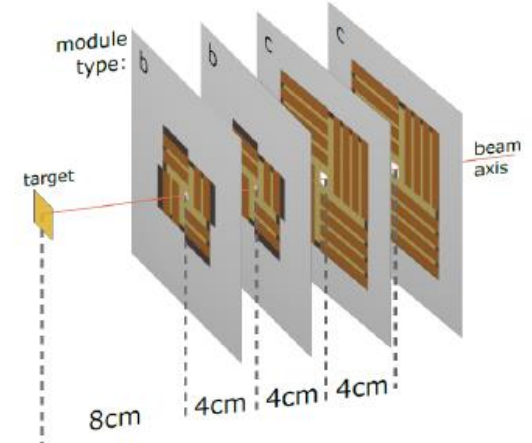


simulations
Data load distribution in most occupied sensor
(number of 16 bits words during 5 μs)

MIMOSIS requirements

- Requirements

Physics parameter	Requirements
Spatial resolution	$\sim 5 \mu\text{m}$
Time resolution	$\sim 5 \mu\text{s}$
Material budget	$0.05\% X_0$
Power consumption	$< 100 - 200 \text{ mW/cm}^2$
Operation temperature	-40°C to 30°C
Temp gradient on sensor	5 K
Radiation* (non-ion)	$\sim 7 \times 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2$
Radiation* (ionizing)	$\sim 5 \text{ Mrad}$
Data flow (peak hit rate)	$@ 7 \times 10^5 /(\text{mm}^2\text{s})$ $> 2 \text{ Gbit/s}$



- MIMOSIS chip

- ✓ Based on ALPIDE architecture
 - Higher data flow
 - (elastic buffer)
 - Higher radiation requirements

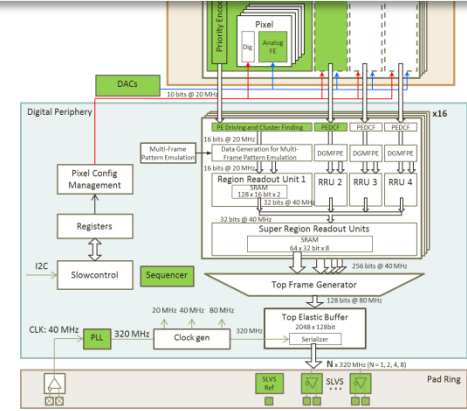
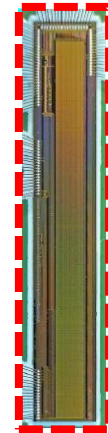
Parameter	Value
Technology	TowerJazz 180 nm
Epi layer	$\sim 25 \mu\text{m}$
Epi layer resistivity	$> 1 \text{ k}\Omega\text{cm}$
Sensor thickness	$60 \mu\text{m}$
Pixel size	$26.88 \mu\text{m} \times 30.24 \mu\text{m}$
Matrix size	1024×504 (516096 pix)
Matrix area	$\approx 4.2 \text{ cm}^2$
Matrix readout time	$5 \mu\text{s}$ (event driven)
Power consumption	$40-70 \text{ mW/cm}^2$

MIMOSIS = a milestone for Higgs factories ($5 \mu\text{m}$ / $\leq 5 \mu\text{s}$)

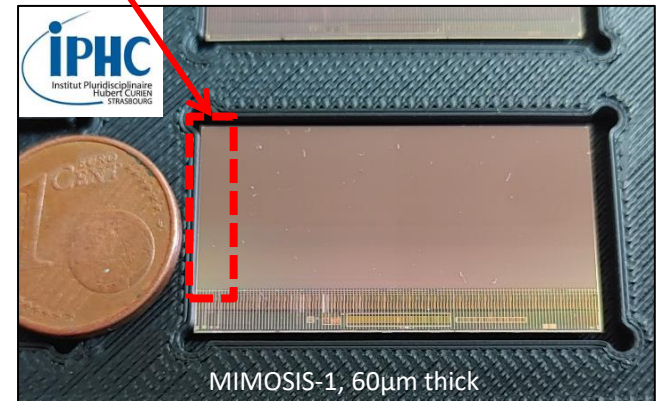
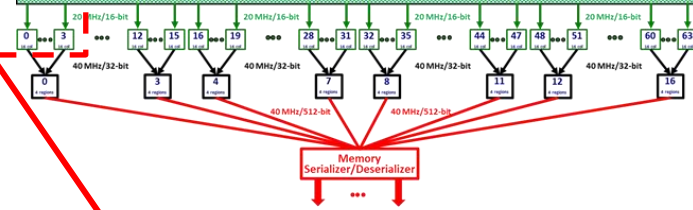
MIMOSIS roadmap

- 4 prototypes:
- MIMOSIS-0: = 2 regions
 - ✓ Tests (2018-2019)
 - Testability
 - Priority encoder frequency
 - Radiation hardness design (SEU)
- **MIMOSIS-1: 1st full size prototype**
 - ✓ Elastic buffer, SEE hardened
 - ✓ Fabricated in 2020
 - ✓ Tests ongoing
- MIMOSIS-2:
 - ✓ On-chip clustering
 - ✓ Submission in 2021
- MIMOSIS-3: final pre-production sensor
 - ✓ >2022

MIMOSIS-0



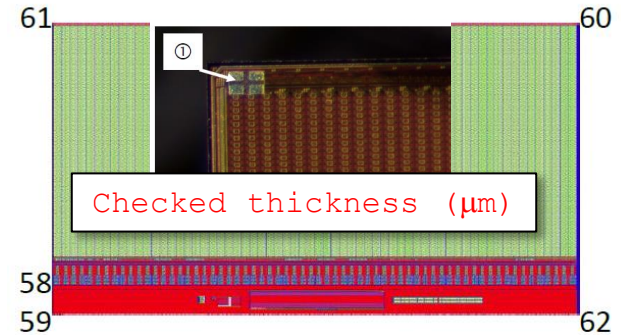
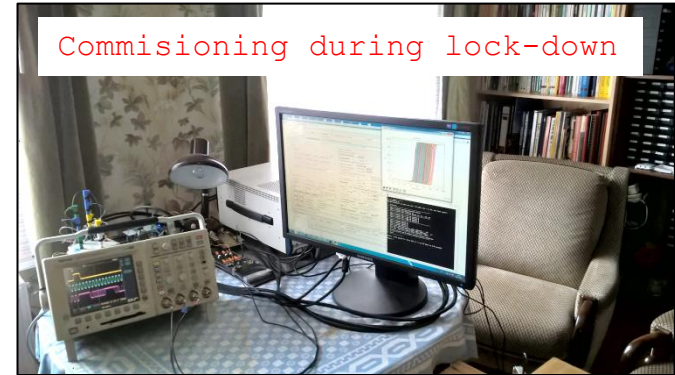
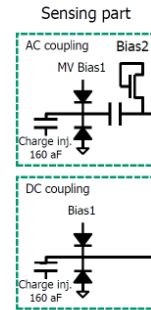
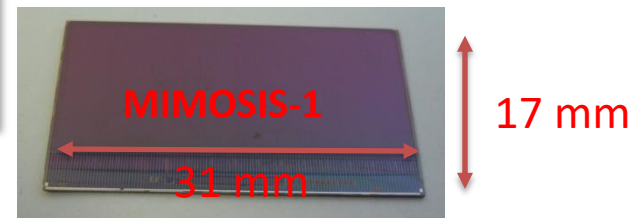
504 x 1024 pixels = 16 super regions
 1 super-region = 4 read-out regions of 16 columns
 2 columns = 1 data driven read-out



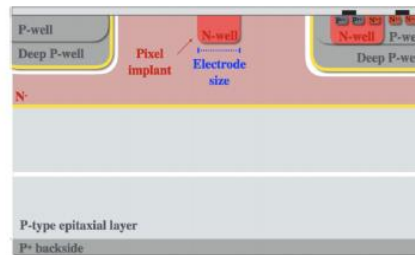
MIMOSIS-1, 60µm thick

⇒ architecture adaptable to a fast sensor for an ILC vertex detector

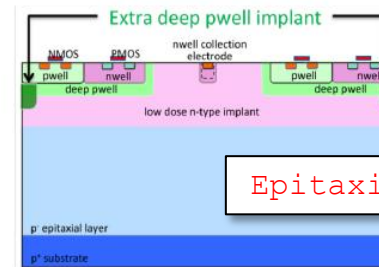
MIMOSIS-1 tests



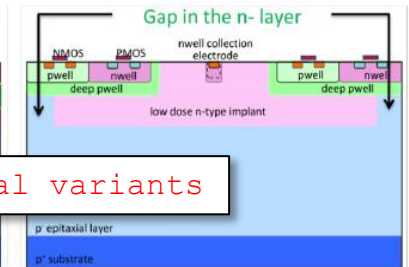
continuous n-layer



additional p-implant



gap in n-layer

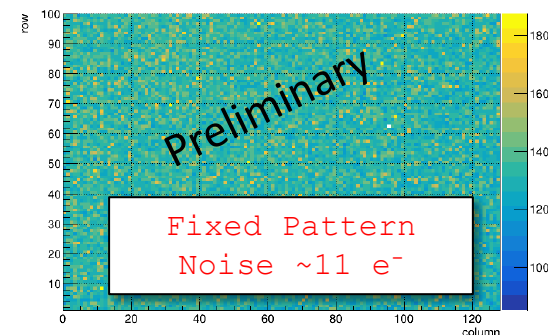
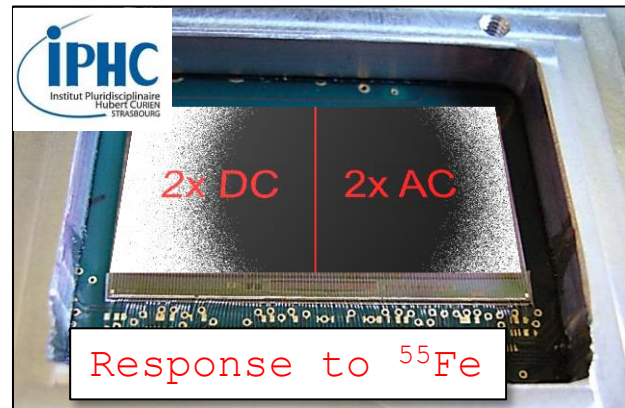


Epitaxial variants

- standard process (3 available wafers)
- continuous n-layer (blanket) (3 wafers)
- additional p-implant (3 wafers)
- gap in n-layer (3 wafers)

- MIMOSIS tests
 - ✓ Submatrices: DC/AC pixels
 - ✓ 6 epitaxial variants (18 wafers)
 - Thinned down to 60 μm
 - Study **Yield**
 - Study **charge collection / spatial res.**
 - Explore performances after **irradiation**
- Intense test program in 2021:
 - ✓ Laboratory tests ongoing
 - ✓ Irradiation tests
 - ✓ Beam tests @ DESY/CERN (Scheduled June/July)
 - ✓ Latchup / SEE tests at GSI ongoing

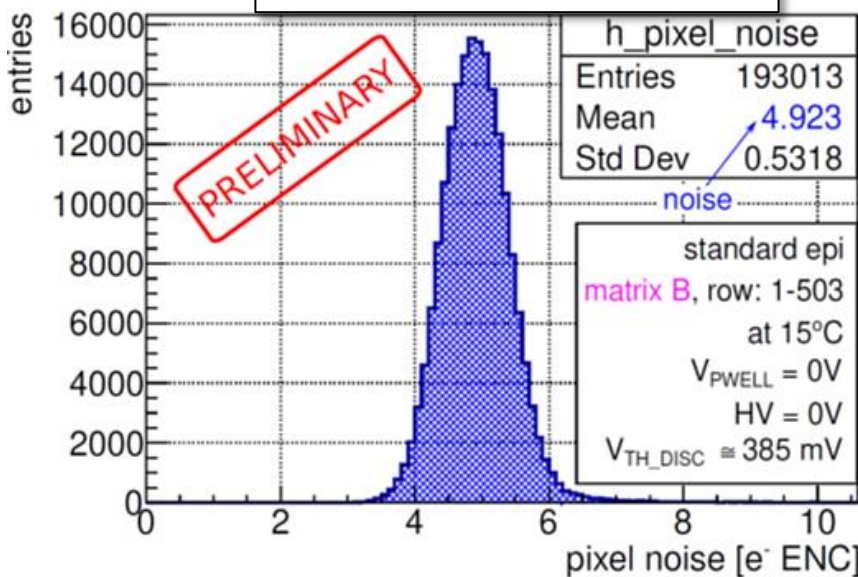
MIMOSIS Preliminary results



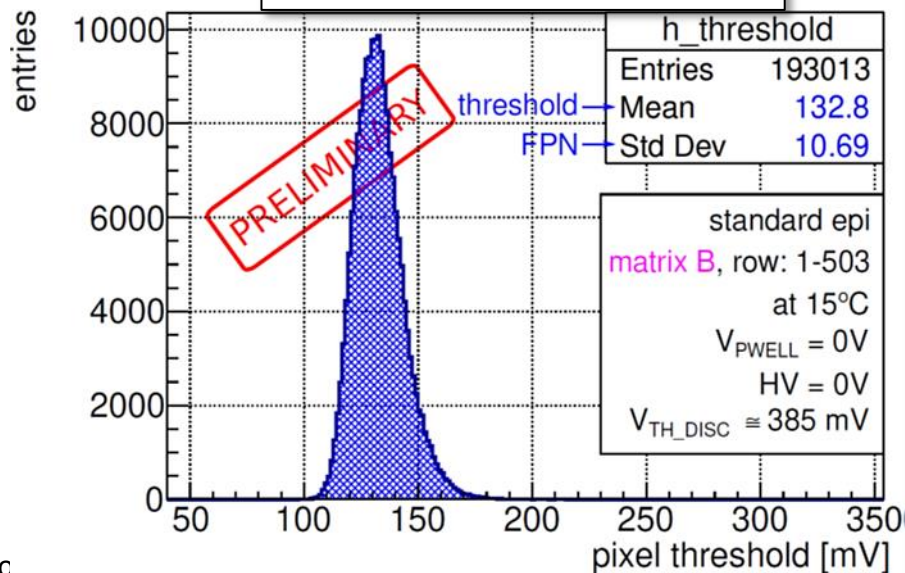
First results match expectations

- DC pixels (no back bias applied)
 - ✓ Threshold $\sim 100\text{-}150 e^- \text{ ENC}$
 - ✓ Pixel Noise $\sim 3\text{-}5 e^- \text{ ENC}$
 - ✓ FPN $\sim 5\text{-}17 e^- \text{ ENC}$
 - ✓ Preliminary:
 - Only few chips tested
 - calibration $\text{mV-}e^- \sim 25\%$ precision

Pixel (Thermal) Noise



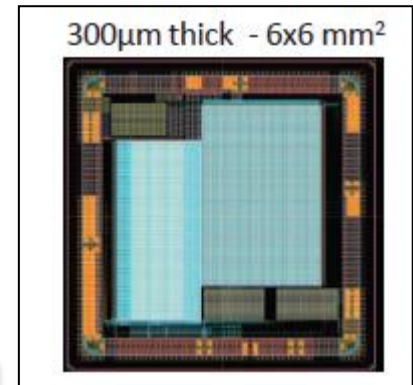
Fixed Pattern Noise



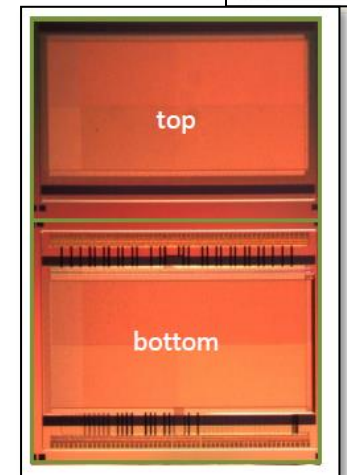
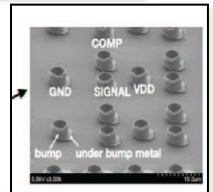
SOI & 3D development @ IPHC



- 2 chips expected back ~ April 2021 (200 nm process)
 - ✓ 1st: HEP applications ⇒ **test Alpide/Mimosis-like pixels (FE), charge collection**
 - ✓ 2nd: **imaging** ⇒ 192x128 pixels with rolling shutter or global shutter readout. Spectroscopic capabilities
 - ✓ **Complementarity with SOFIST family (KEK)**
- Digital libraries developed in cooperation with KEK.



Double-tier activities @ IPHC



- Double-tier « 3D » in CMOS TJ 180nm technology
 - ✓ Bonding performed by T-micro (same company used for SOFIST)
 - ✓ Bonding pitch = 10 µm.
 - ✓ Pitch = 20 µm
 - ✓ 2nd submission expected back from foundry ~ July 2021
- Both chips are sensitive + output logic in bottom chip
- Goal: compare
 - ✓ Direct read-out from bottom chip
 - ✓ **Read-out after transmission through bonding from top chip**
- Allows to
 - Test capacitive noise between the 2 layers
 - Test pixel dispersion

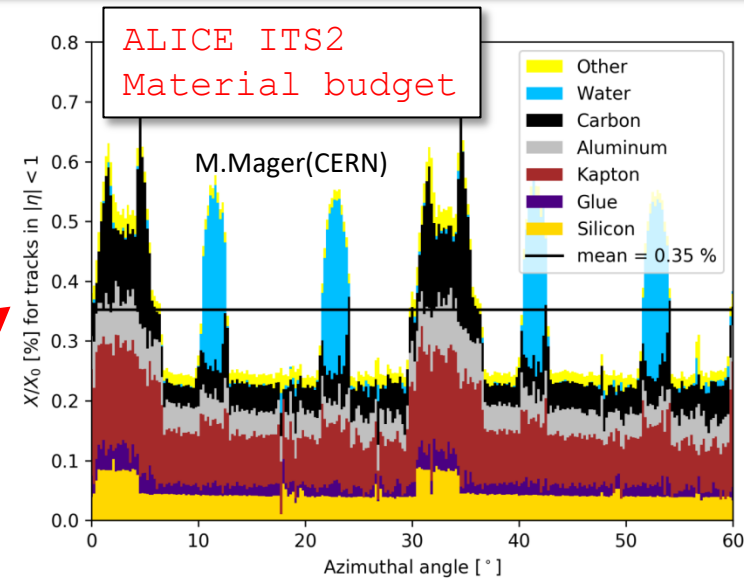
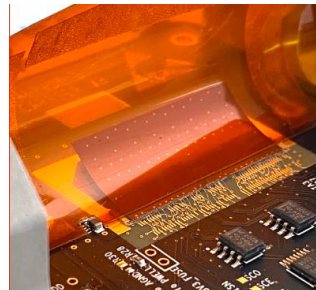
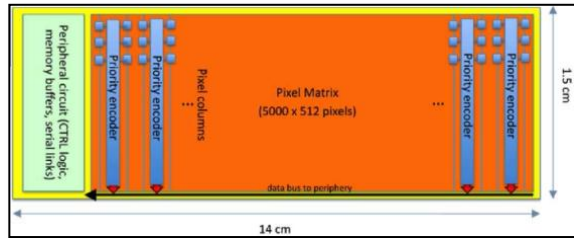
Example of fruitful collaboration between different labs and different technologies



Bent sensors tests @ IPHC

Stitching:

- ✓ The way to go to minimize material budget



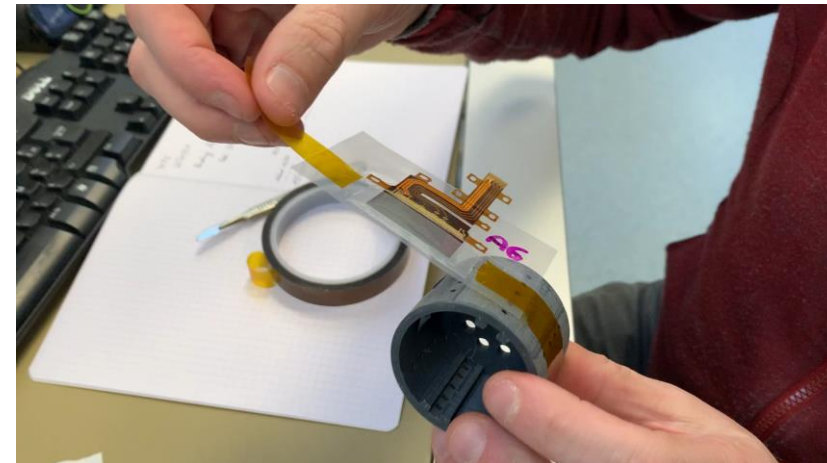
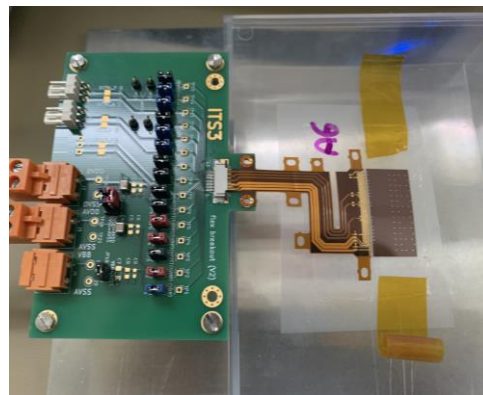
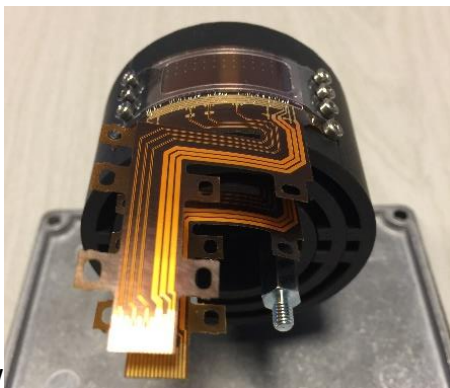
ALICE-ITS3/CERN drives the R&D

- ✓ Cf. M. Mager talk on Thursday

- And e.g. M.Mager 4th FCC Physics and experiment workshop (Nov. 2020): *MAPS in ALICE and perspectives*

Micro-technics tests @IPHC

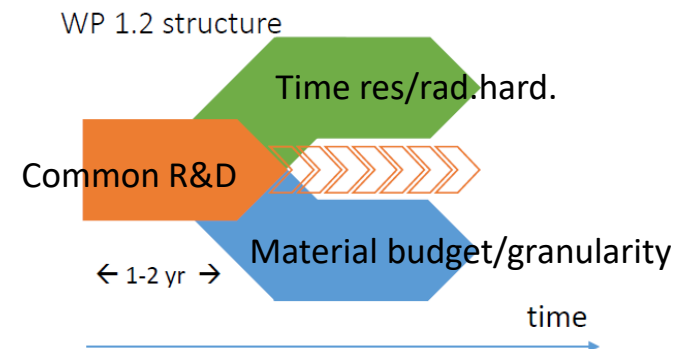
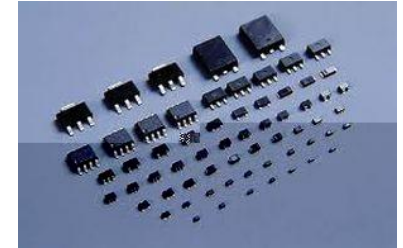
- ✓ collaboration with ALICE-ITS3
- ✓ Know-how acquired for bent bonding.



Bending / bonding
Or Bonding / bending
⇒ Functional tests

TJ-65 nm process: smaller feature size

- 65 nm feature size technology
 - ✓ (ALPIDE & MIMOSIS fabricated in 180 nm)
 - ✓ Larger wafers (\Rightarrow 30 cm)
 - ✓ More functionalities inside the pixel
 - ✓ Keeps pixel dimensions small \Rightarrow spatial res.
 - ✓ Potentially faster read-out
 - ✓ Lower Power consumption
 - **TJ-65 nm now available** (since June 2020)
 - ✓ Main driver: CERN EP R&D WP 1.2 & ALICE ITS-3 upgrades (involves other labs) \Rightarrow LS3 ~ 2024-26
 - ✓ Different requirements
 - EP: time resolution and radiation tol.
 - ALICE: granularity and material budget
 - Common R&D during the 1st years.
- \Rightarrow Synergy with Higgs factories requirements
- \Rightarrow See talk by Magnus Mager (thu.18th)



\Rightarrow Relation with foundries and access to options is a key factor

65 nm process status @IPHC

- IPHC-Strasbourg:

- ✓ Goal: **validate the process for charged particle detection**

- **Caveat:** sensitive volume not yet Optimised

- ✓ + Test structures (DACs, amplifiers, etc.)

- ✓ **4 matrices submitted: CE-65**

- Technology exploration with single rolling shutter / **analog output**

- Pitch: 15/25 μm

- N-well variants,

- Amps (AC/DC), SF

- **Testable in beam**

- ✓ Part of Cremlin+ program (1 post-doc)

- ✓ First submission December 1st 2020 (CERN-MLR1)

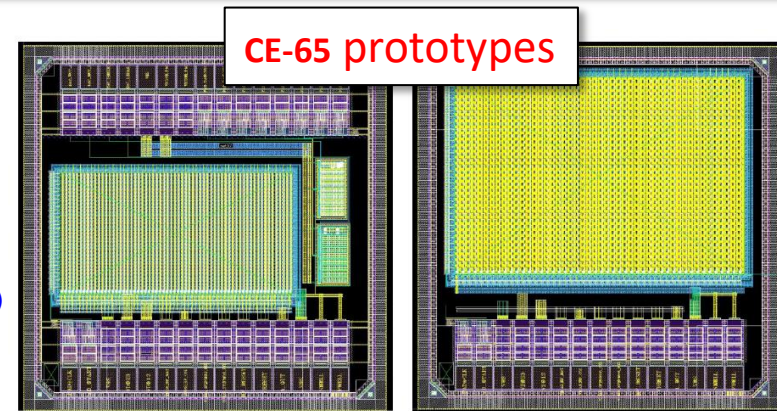
- Expects back from foundry ~ **mid-2021**

- DAQ/Beam tests with ALICE groups (ITS3 WP3 & Cagliari): **Q4 2021-2022**

- Next steps / next submission

- ✓ Under discussion with CERN

- Stitching ?



Variants A/B/C

64 × 32

15 μm pitch

Variant D

48 × 32

25 μm pitch

CREMLIN PLUS
Connecting Russian and European Measures
for Large-scale Research Infrastructures

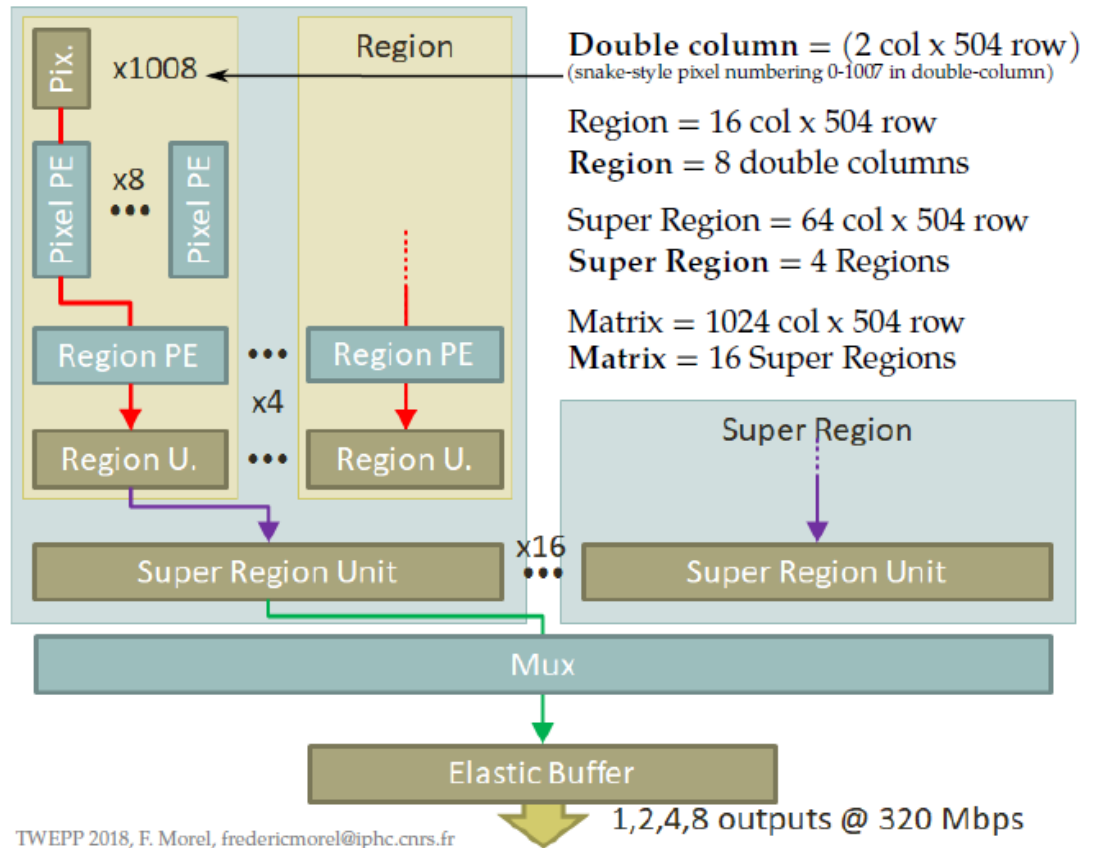
Summary: Synergies in CMOS R&D

- Integration ⇨ many open issues here !
- CMOS Pixel Sensors are the baseline for Higgs factories
 - ✓ Requirements are within reach
- The technology keeps evolving
- Strong dynamic of CMOS pixel Sensors R&D:
 - ✓ 180 nm : MIMOSIS series (5 μ m spatial res./ \leq 5 μ s time res./ 60 μ m thickness)
 - ⇨ full size prototype being tested
 - ✓ 65 nm technology exploration
 - First submission dec.2020
 - Time resolution & granularity
 - ✓ **Stitching** & large surfaces for very low mass detectors ⇨ Priority for Higgs factories in the future
 - Material budget & Large pixelated surfaces
 - ✓ **Synergies** with
 - CERN R&D (ALICE ITS upgrades and EP R&D WP1.2)
 - R&D programs (e.g. AIDA-Innova, CREMLIN+, etc.)
 - Heavy ion experiments (e.g. ALICE beyond LS3/4 proposal, CBM, EIC)
 - Other experiments: Belle-II, etc.

Back up

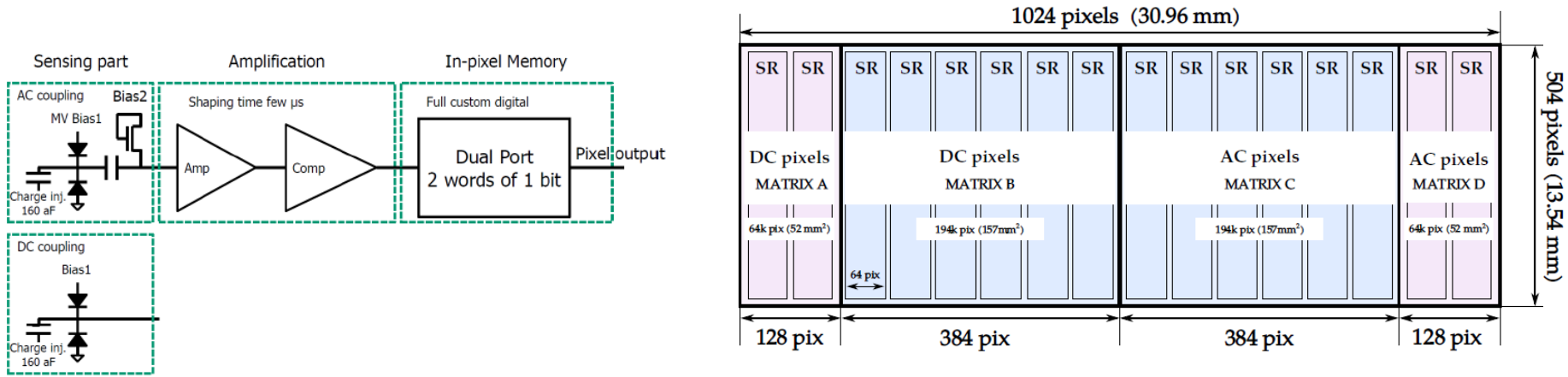
Mimosis data path

- 3-stage buffering allows to handle with data rate fluctuations
- 8 double-columns forms 1 Region (8064 pixels) → read out by priority encoder @ 20 MHz.
- each region has a region buffer (capacity up to 100 words).
- 4 Regions (1 Super Region) → data sent @ 40 MHz to Super Region Buffer
- 16 SR (whole matrix) → data goes through frame generator to elastic buffer @ 80 MHz
- elastic buffer – can store up to 16384 words and outputs the data on 8 differential data links



- MIMOSIS-1 has 8 outputs each 320 Mb/s providing a required data throughput for MVD

AC / DC pixels



- DC Pixels (~ALPIDE) & AC pixels (top bias up to $> 20\text{V}$)
 - ✓ Amplifier / shaper / discriminator chain similar to ALPIDE in both scheme
 - ✓ Data driven readout
 - ✓ Pulse injection for calibration
 - ✓ Pixel masking options

CMOS pixel sensor (CPS) for charged particle detection

Main features

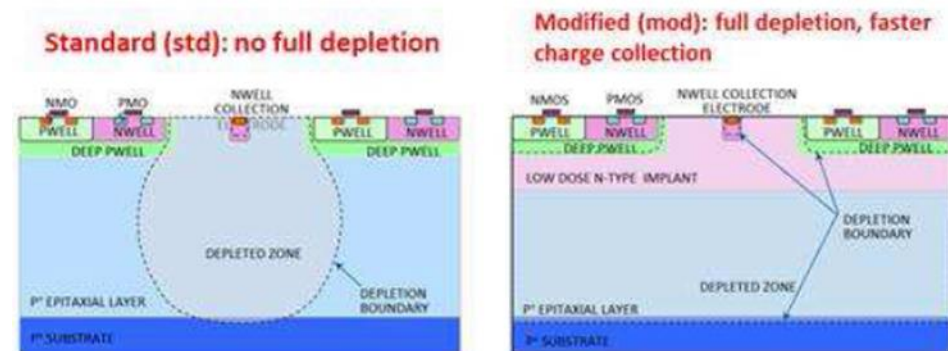
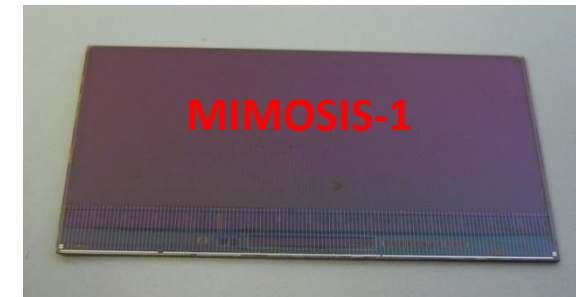
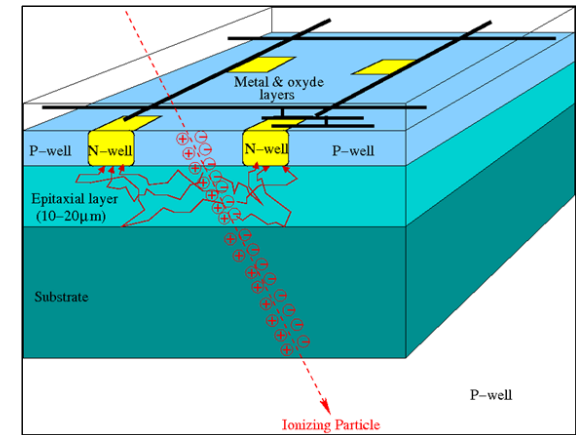
- ✓ **Monolithic** (Signal created in low doped thin epitaxial layer $\sim 10\text{-}30\ \mu\text{m}$)
- ✓ Thermal diffusion of e^- (Limited depleted region) + drift
- ✓ Charge collection: N-Well diodes (Charge sharing)
- ✓ Continuous charge collection (No dead time)

Main advantages

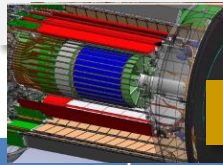
- ✓ **Granularity**
- ✓ **Material budget**
- ✓ Signal processing integrated in the sensor
 - Low signal & **Low Noise**
- ✓ Flexible running conditions (Temperature, Power, Rad. Tol.)
- ✓ **Industrial** mass production
 - Advantages on costs, yields, fast evolution of the technology,
 - Possible frequent submissions

Main limitations

- ✓ Industry addresses applications far from HEP experiments concerns
- ✓ **Needs adapted processes**

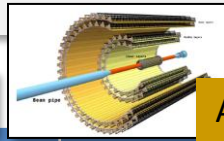


Evolving CPS



ULTIMATE

STAR-PXL



ALPIDE

ALICE-ITS



MIMOSIS

CBM-MVD

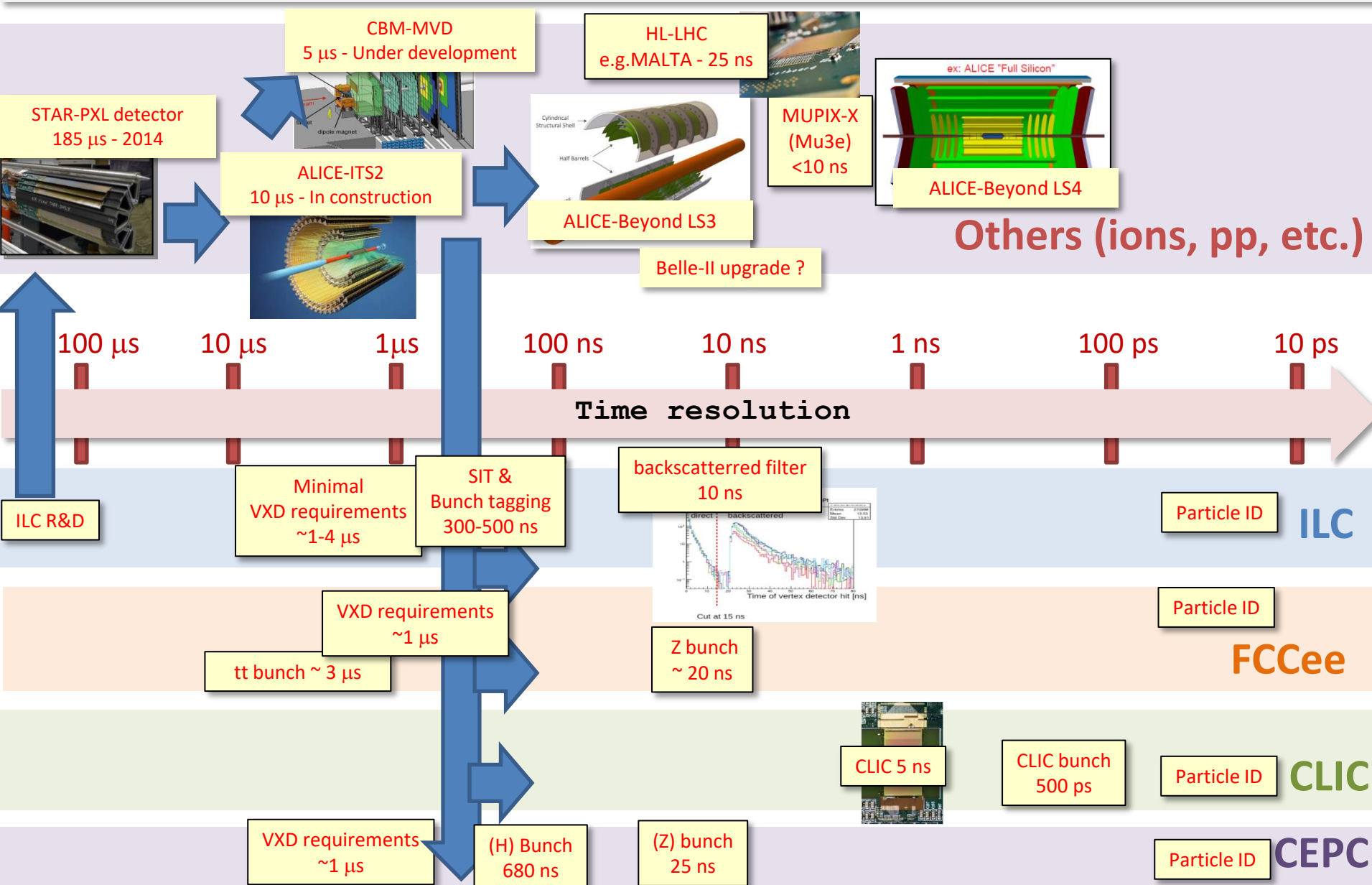
PSIRA proposal



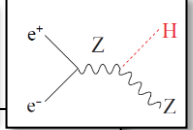
ILD-VXD

	STAR-PXL	ALICE-ITS	CBM-MVD	ILD-VXD
Data taking	2014-2016	>2021-2022	>2022	>2030
Technology	AMS-opto 0.35 μm	0.18 μm	0.18 μm	0.18 μm (conservative) < 0.18 μm ?
	4M	HR, $V_{\text{bias}} \sim -6\text{V}$ Deep P-well	HR, Deep P-well	?
Architecture	Rolling shutter + sparsification + binary output	Data driven r.o. In pixel discri.	Data driven r.o. In pixel discri.	Data driven r.o. (conservative)
Pitch (μm^2) / Sp. Res.	20.7 x 20.7 / 3.7	27 x 29 / 5	27 x 30 / <5	$\sim 22 / \sim 4$ OR $\sim 17/3$
Time resolution (μs)	~ 185	5-10	5	1 – 4
Data Flow		$\sim 10^6$ part/cm ² /s Peak data rate ~ 0.9 Gbits/s	peak hit rate @ 7×10^5 /mm ² /s >2 Gbits/s output (20 inside chip)	~ 375 Gbits/s (instantaneous) ~ 1166 Mbits / s (average)
Radiation	O(50 kRad)/year	2×10^{12} n _{eq} /cm ² 300 kRad	3×10^{13} n _{eq} /cm ² /yr & 3 MRad/yr	O(100 kRad)/year & O(1×10^{11} n _{eq} (1MeV)) /yr
Power (mW/cm ²)	< 150 mW/cm ²	< 40 mW/cm ²	< 100 mW/cm ²	~ 50 -100 mW/cm ² + Power Pulsing
Surface	2 layers, 400 sensors, 360x10 ⁶ pixels 0.15 m ²	7 layers, 25x10 ³ sensors > 10 m ²	4 stations Fixed target	3 double layers 10 ³ sensors (4cm ²) 10 ⁹ pixels ~ 0.33 m ²
Mat. Budget	$\sim 0.39\%$ X ₀ (1st layer)	$\sim 0.3\%$ X ₀ / layer		~ 0.15 -0.2 % X ₀ / layer
Remarks	1 st CPS in colliding exp.	(with CERN)	Vacuum operation Elastic buffer	Evolving requirements

Time resolution in the context of e^+e^- colliders



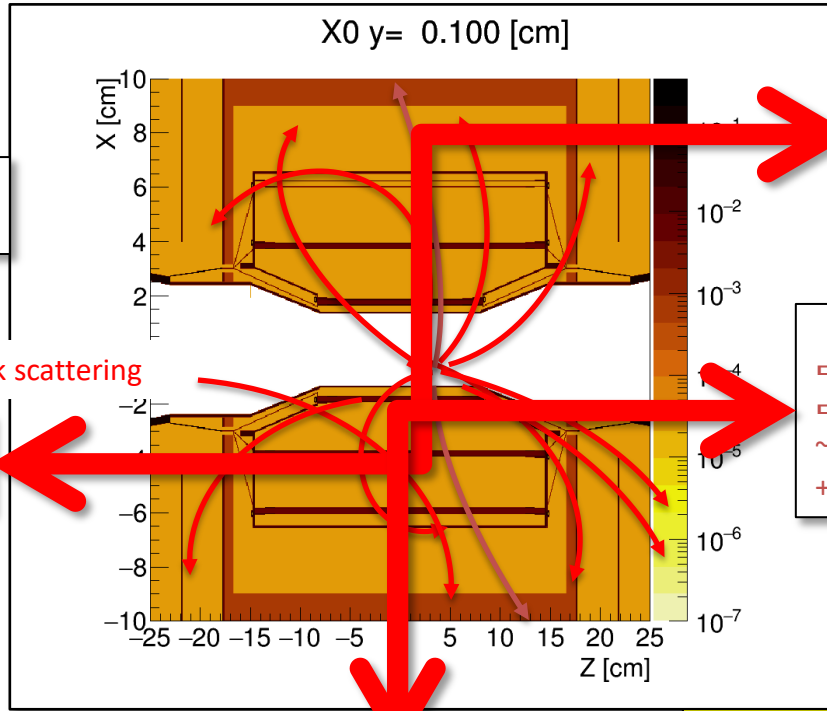
ILC VXD requirements

$$\sigma_b < 5\Theta \frac{10}{p\beta \sin^2\theta} \mu\text{m}$$


Physics
 ⇒ Flavour tagging
 ⇒ Low pT tracks

Physics (<Hz/cm²)

Beam background (~ 5 hits/BX/cm² on layer 0)



Vertex reconstruction
 ⇒ granularity
 ⇒ Pitch ~17 μm
 ⇒ (σ_{sp} ~3 μm)

Material Budget
 ⇒ ~ 0.15% X₀ / layer
 ⇒ < 1% X₀ for the whole VTX
 ~ 900 μm Si
 + ~0.14% X₀ for the beam pipe

Low material detectors & supports structures

Cooling
 Stiffness / Alignment

Beam background
 Radiation hardness
 O(100kRad/yr) & O(10¹¹)n_{eq}/yr
Rad.Tol. devices

Read-out speed
 O(1-10 μs)
 Power consumption
 ~< 50mW/cm²

Fast read-out & low Power architectures

Challenge : meet the requirements all together