The Open University

Silicon Pixel Tracker for the ILC

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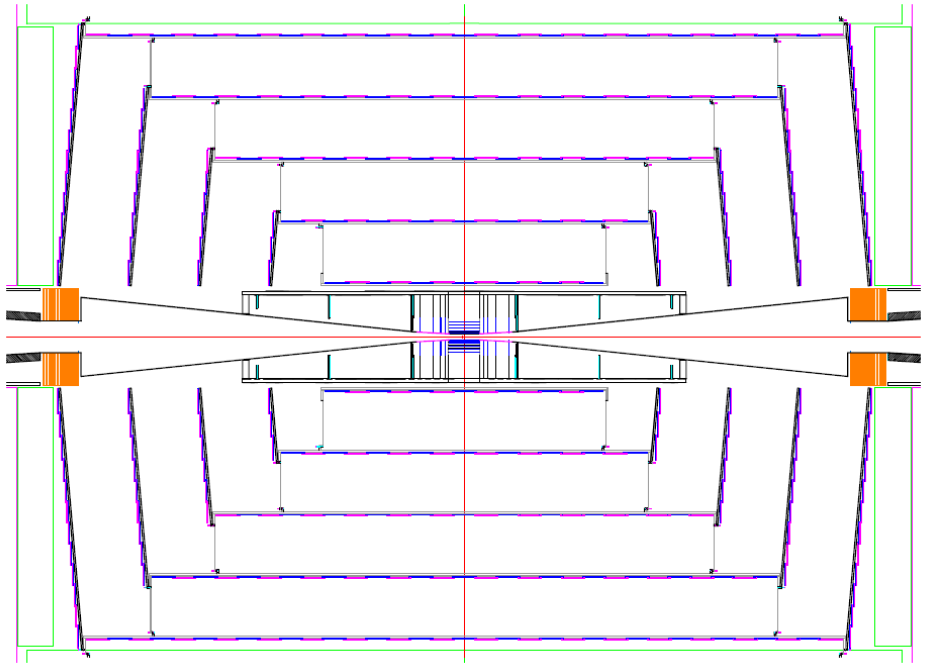
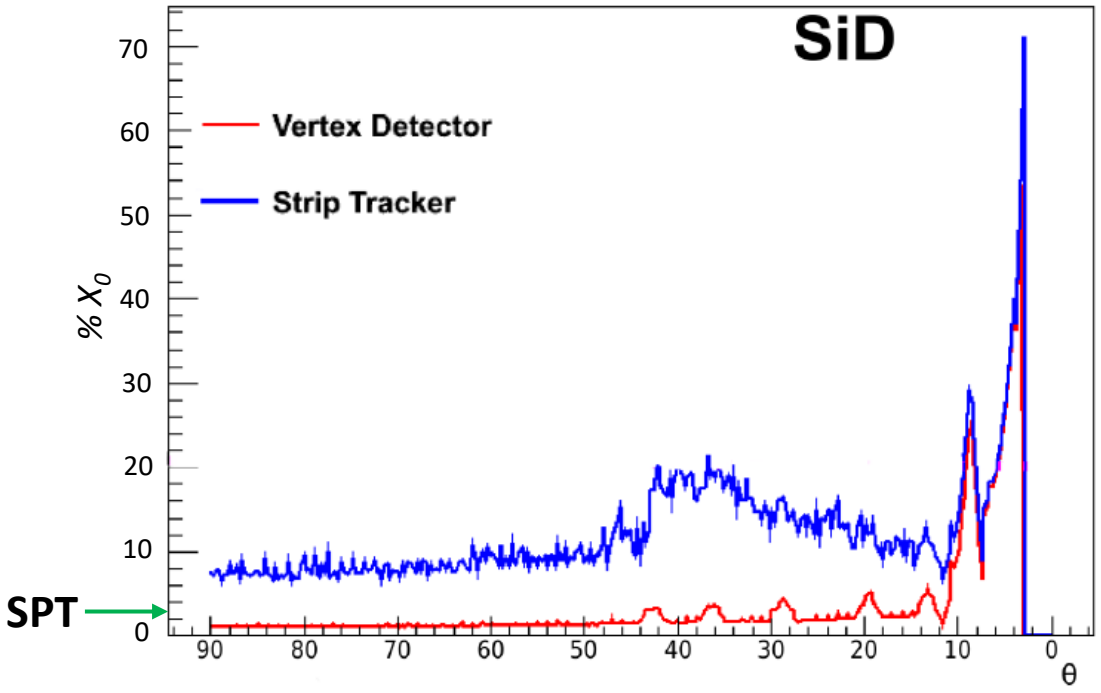
Introduction



SiD microstrip tracker: 5 barrels with 4 disks on each side (ILC TDR 2013)

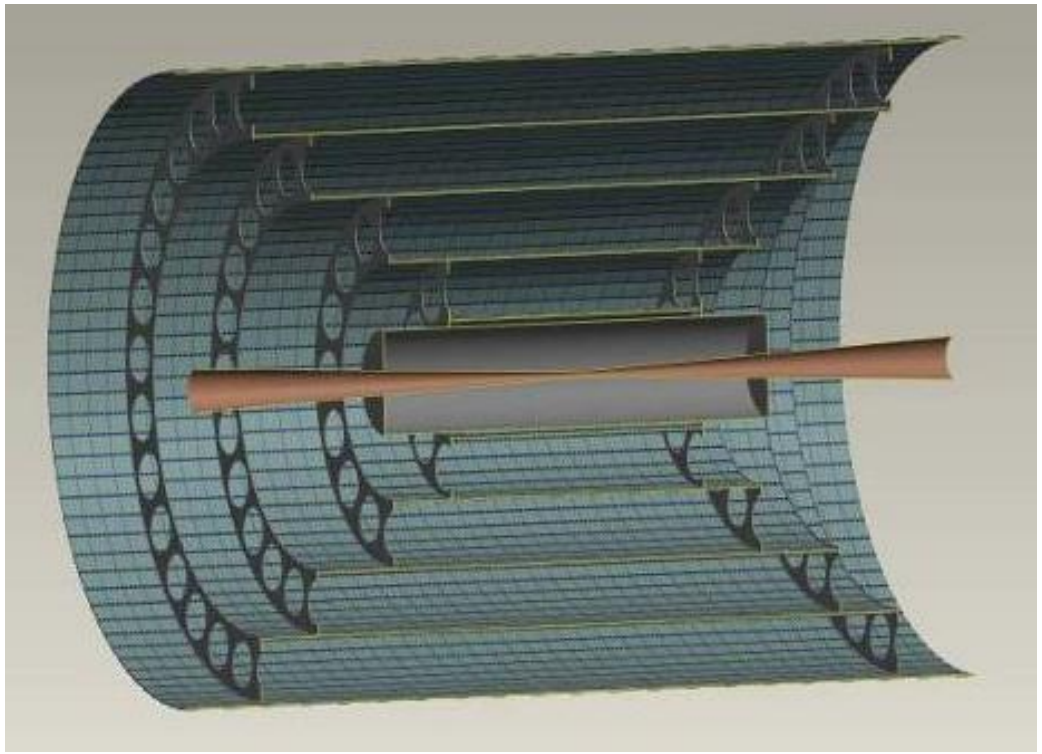
- Baseline: SiD's microstrip tracker
- Silicon Pixel Tracker (SPT) suggested as a next generation detector with several performance advantages
  - First proposed at LCWS2008
- Major technological advances since 2008
  - A large MAPS-based detector has been built – ITS2 (ALICE)
  - Low power, fully depleted, radiation-hard MAPS developed
- The physics case remains very strong

Performance and requirements



- SiD:
  - 5 layers of Si microstrip sensors, 25 µm pitch / 50 µm readout
  - Resolution in $r\varphi \approx 5$ µm, resolution in $rz \approx 5$ mm
- Very clean conditions, strip occupancies are comfortable over the full angular range
- SPT
  - Reduced material over the whole range, total 3% X_0 target
  - Combining time-integrating tracking layers and timing information from the vertex detector and dedicated timing layers (pre-ECAL) for robust pattern recognition

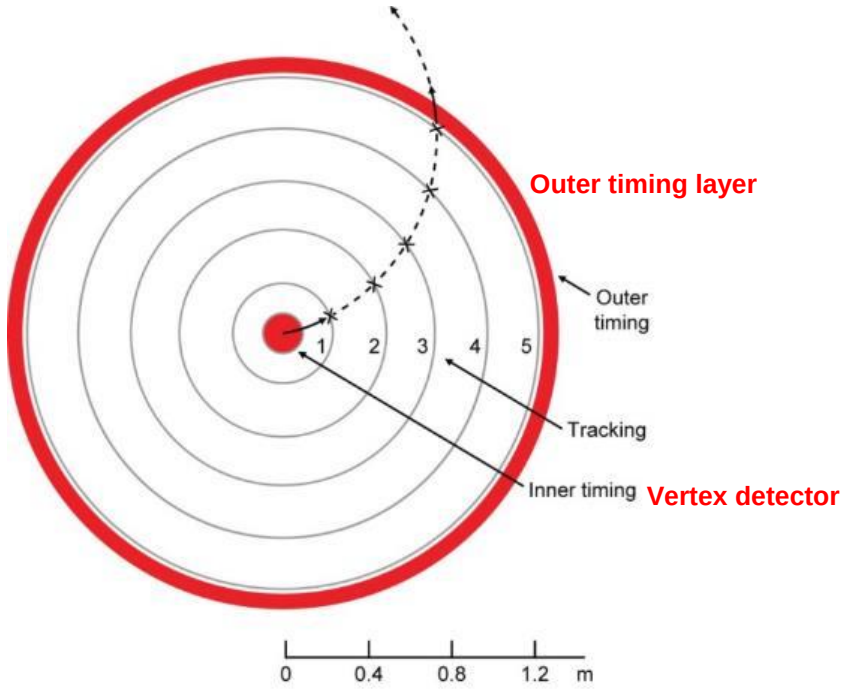
SPT – tracking layers



5 barrels, 4 endcaps (not shown)

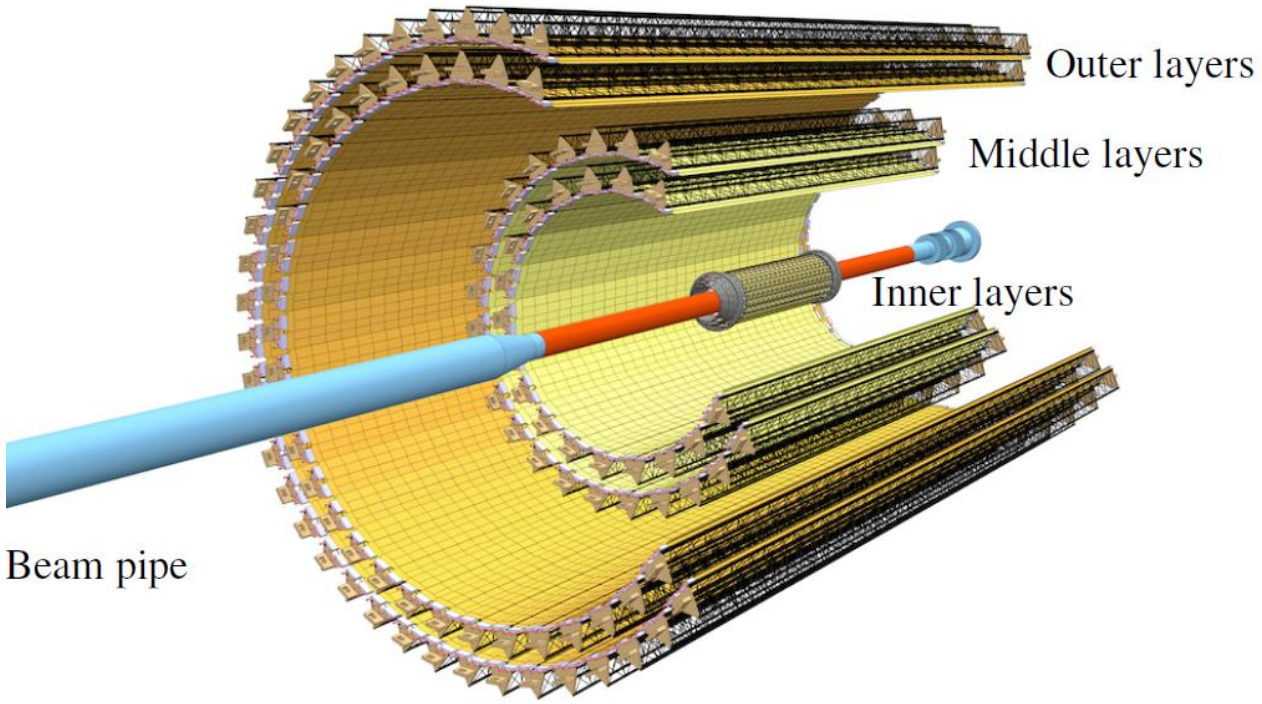
- The main challenge is to reduce power and therefore material
- Power dissipation ~O(100 W), can be air-cooled
- Sensors ≈100 µm thick, low mass support (≈0.6% X_0 per layer)
- Pixel size around 50 µm × 50 µm
- 28 Gpix system, 70 m^2 of silicon
- Main occupancy is due to time-integrated physics events during the train, but is even cleaner than the baseline in terms of pixel occupancy
- Worst case (barrel 1): occupancy is below 10^{-6} due to the fine granularity

SPT – timing layers



- Single bunch timing information from the vertex detector and from dedicated timing layers just before the ECAL
- Outer timing layers
  - 3 closely spaced layers for redundancy
  - Adjacent to ECAL barrel and endcaps
  - Timing resolution of 554 ns (single bunch spacing)
  - Material budget not critical, hence evaporative cooling is acceptable
  - 150 µm square pixels
- Inner timing layers
  - The vertex detector also serves this purpose
- Track reconstruction:
  - Start with 3-hit track stubs in the outer timing layers and work inwards refining the momentum measurement as this proceeds
  - Link to stand-alone tracks in the vertex detector
  - Square pixels deliver equal precision in impact parameter resolution in $r\varphi$ and rz

ITS2 (ALICE) as an excellent example



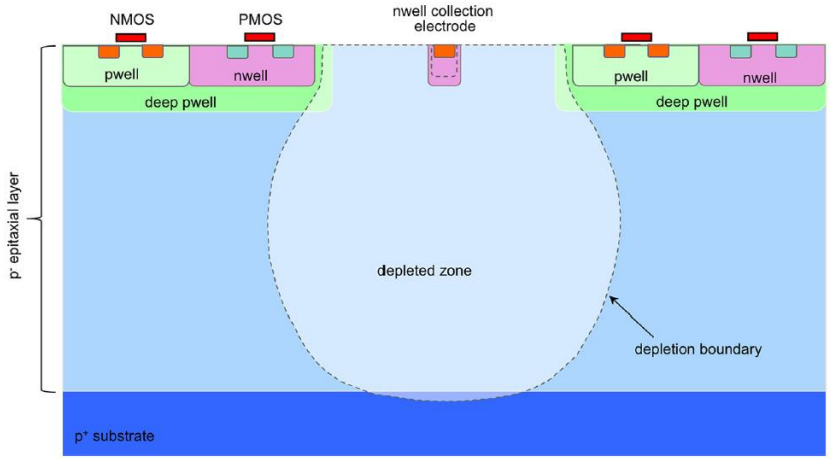
ALICE ITS2 TDR, CERN-LHCC-2013-024

- 12.5 Gpixels
- ≈30×30 µm pixels
- Outer barrel 1.48 m long
- Total 10 m^2 silicon
- 180 nm CMOS process

MAPS Technology

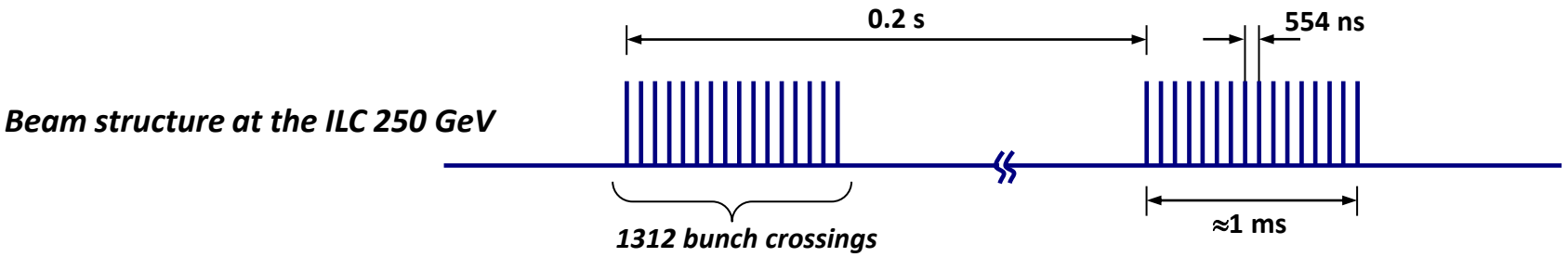
- Major advances demonstrated since 2008
- Thick epitaxial layer ~40 µm, MIP signal ~3000 e^-
- Small sense node, low noise (10 e^-)
- Low power $\propto (C/Q)^m, m = 2 \ldots 4$
- Radiation hardness not an issue for ILC
- Technology is suited for larger (50-150 µm) pixels

"Quadruple well" – 100% fill factor, full CMOS in pixel (2008)



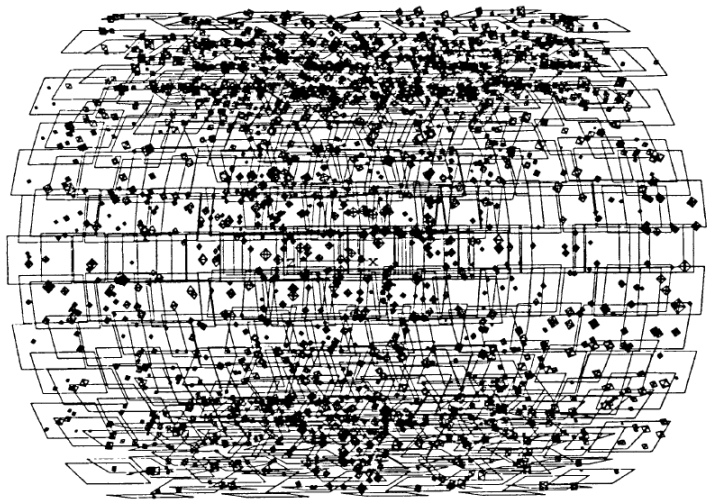
W. Snoeys et al., NIM A871 (2017) 90–96

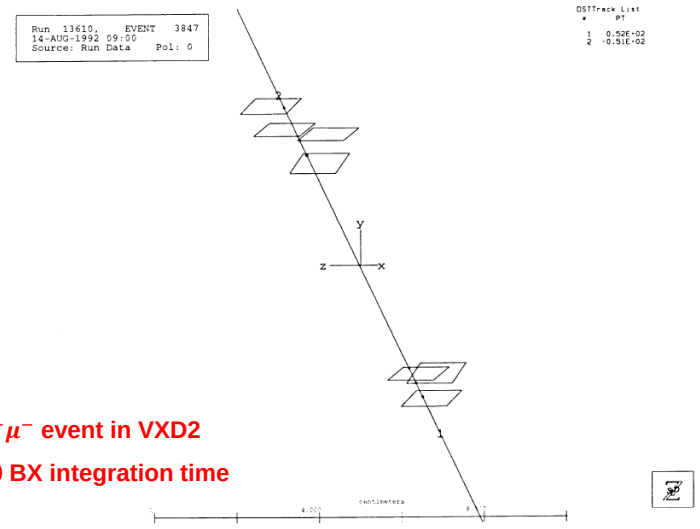
Readout schemes for the SPT



- Two readout schemes:
  - Time-integrating through the bunch train – in the tracking layers
  - Single bunch time stamping – in the timing layers

Time-integrating tracker

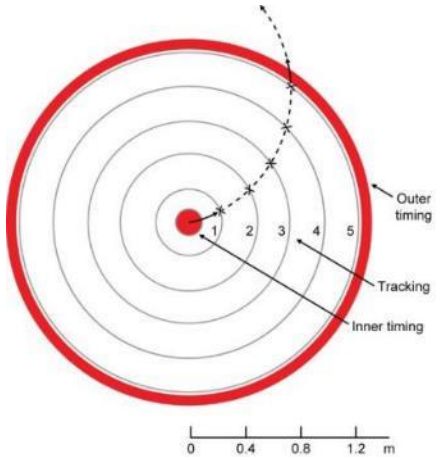




$\mu^+\mu^-$ event in VXD2

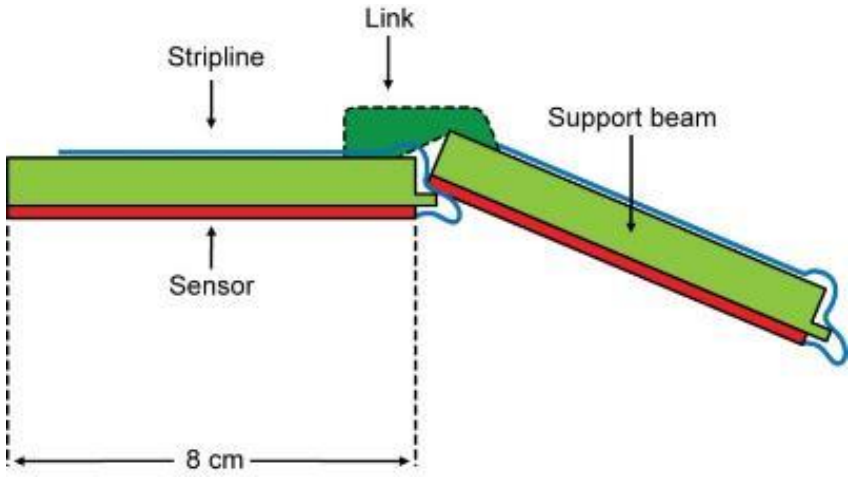
10 BX integration time

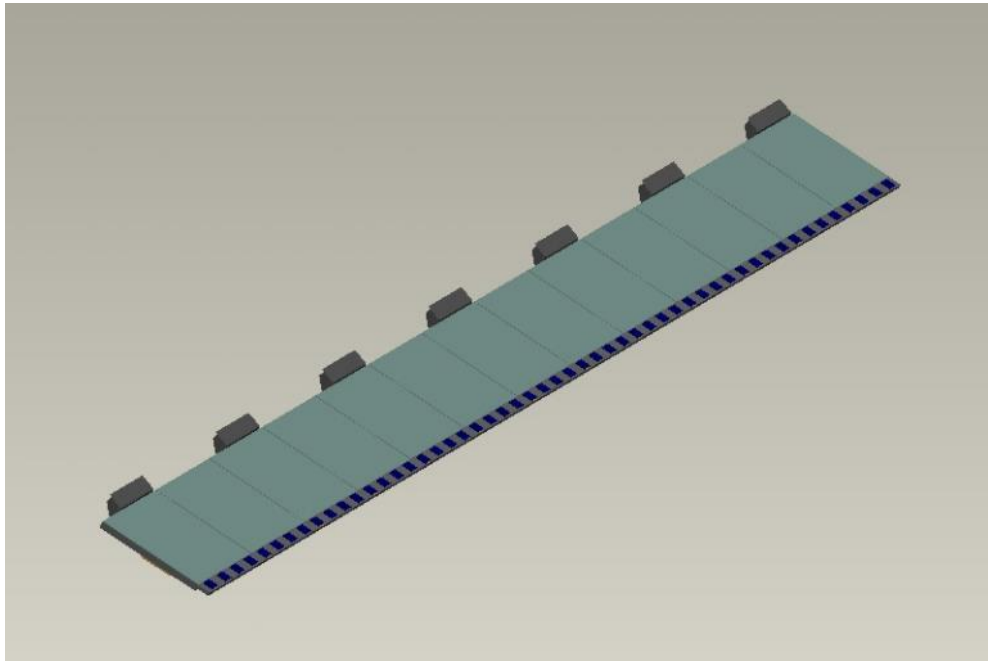
- **Operation:**
  - **Each pixel stores analogue hit information on its sense node**
  - **The detector is read out in the long time in between the bunch trains**
  - **Low noise readout with sparsification**
- **Digitised (e.g. 5-bit) output signal from a 3×3 pixel area around a hit to provide centroid peak fitting and help understand backgrounds**
- **Lowest mass and power**
  - **Near-constant power ~*O*(100 W), air-cooled**



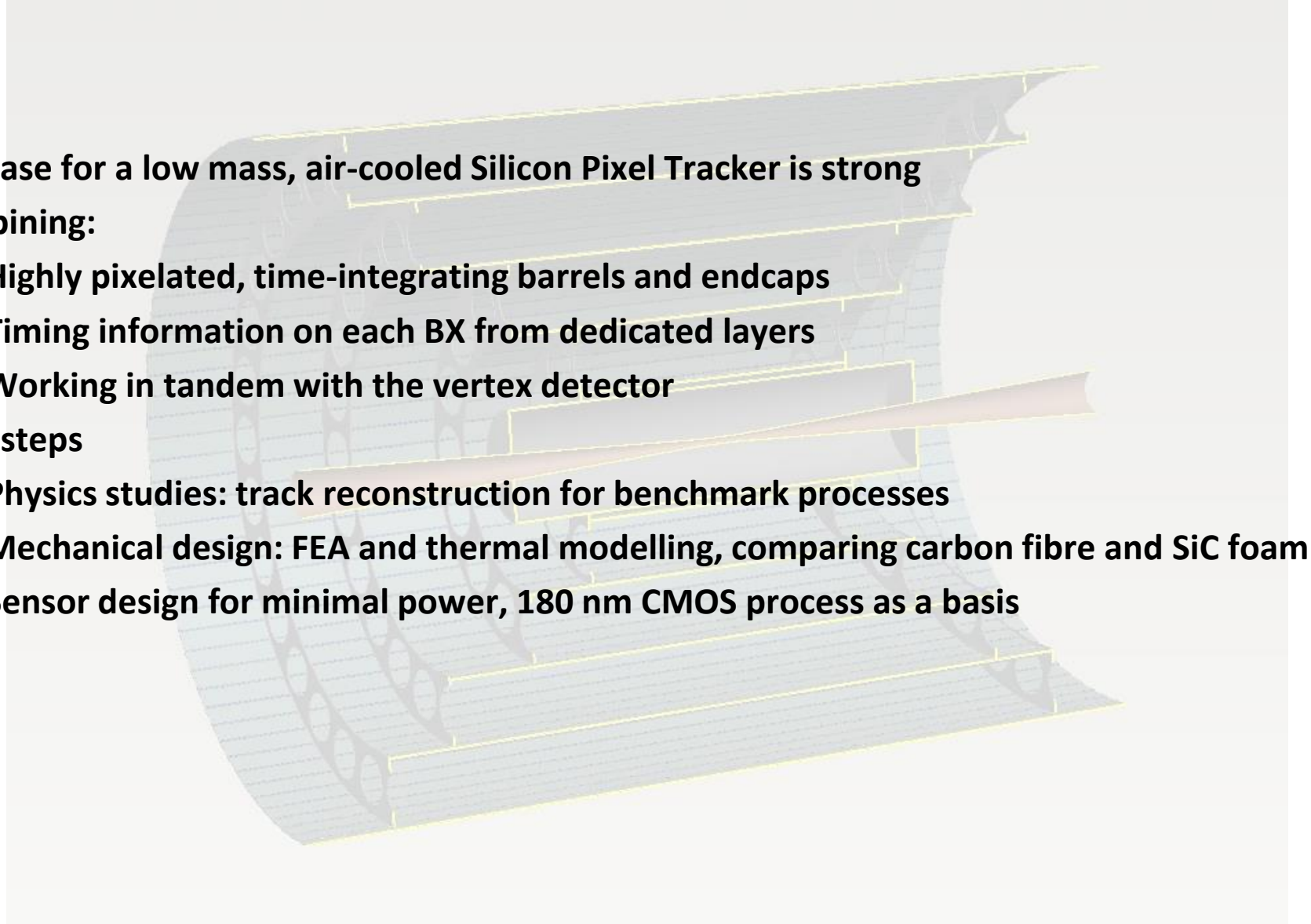
Mechanical

- Geometry largely following the SiD design, but with some new ideas:
  - Less material, 100 µm thick sensors
  - Long staves made entirely from 4-8% SiC foam (5 mm thick, at most 0.45% X_0)
  - SiC is a good thermal match to Si
  - Self-supporting barrel with SiC joining blocks
  - Each half-barrel is attached to its pair of endcaps to form a rigid structure
  - The 5-layer structure provides additional stability
- Detailed study needed





Conclusions and possible next steps



- The case for a low mass, air-cooled Silicon Pixel Tracker is strong
- Combining:
  - Highly pixelated, time-integrating barrels and endcaps
  - Timing information on each BX from dedicated layers
  - Working in tandem with the vertex detector
- Next steps
  - Physics studies: track reconstruction for benchmark processes
  - Mechanical design: FEA and thermal modelling, comparing carbon fibre and SiC foam supports
  - Sensor design for minimal power, 180 nm CMOS process as a basis