Vertex detectors : beyond the CMOS sensors pixel detectors

- **FROM CMOS (MIMOSA Like) pixels**
- **Trend to Depleted pixels for radiation hardening**
- **DotPiX pixels (under development at IRFU and associate laboratories)**

1. How to improve point to point resolution below < 5 µm ?
2. With better other characteristics (radiation hardness and possibly time tagging)
3. Simulations (material, device quantum, electrical) are needed due to the device's dimensions

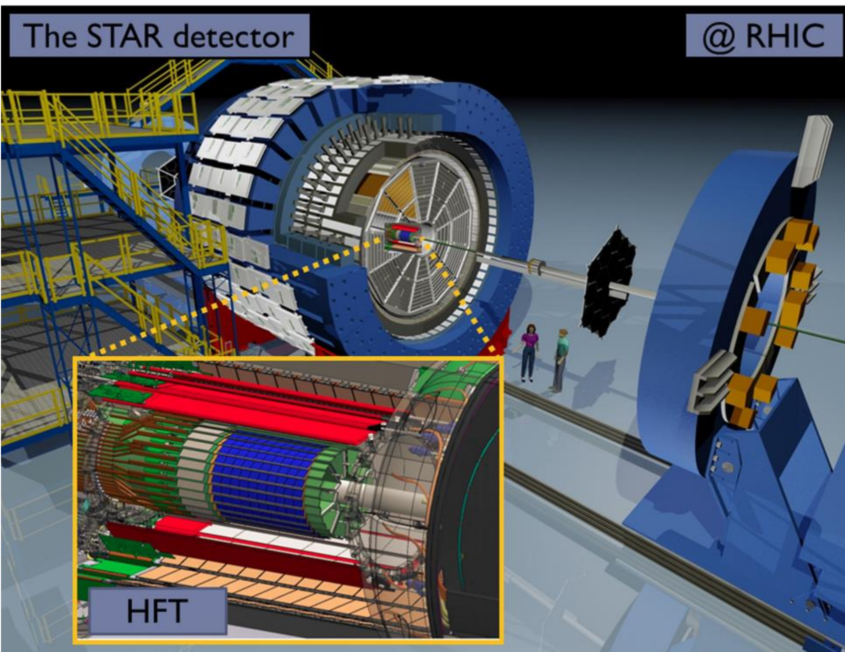
Irfu - CEA Saclay
Institut de recherche sur les lois fondamentales de l'Univers

Vertex detectors : beyond the CMOS sensors pixel detectors

One example : STAR tracker and vertexer at RHIC

- Monolithic Active Pixel Sensors were implemented in the STAR RHIC experiment
- Aim : heavy flavor domain , D0 →K π process at RHIC

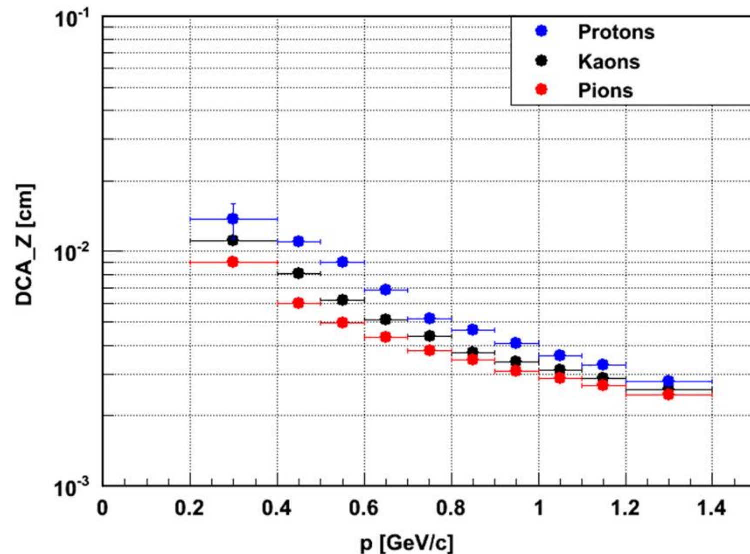
How does it like ? https://doi.org/10.1016/j.nima.2016.04.109



The MAPS-based vertex detector for the STAR experiment: Lessons learned and performance
Giacomo Contin for the STAR collaboration , 2016

Vertex detectors : beyond the CMOS sensors pixel detectors

One example : STAR tracker and vertexer at RHIC



- Along the beam coordinate (z) (projected)
- Resolution 10-100 µm , (not at pT)
- Reference : STAR collaboration
- https://doi.org/10.1016/j.nima.2016.04.109

- 20.7 µm pixel pitch and 185 µs readout time
- 2.8 cm and 8 cm from the beam line
- Power : 170 mW/cm2
- p Au events
- Air cooled
- Good resolution : innermost layers
- Cosmic ray tests : 25 µm point to point resolution

Radiation hardness issues :

- the runs were done NIEL 3x1012/cm2
- and : < 150 krads ionizing dose
- Not more ??
- Lot of latch-up according to the STAR collaboration (2014)

Vertex detectors : beyond the CMOS sensors pixel detectors

So what to improve : radiation hardness

- **Latch-up mitigation :**

1. **Use separate devices, high resistivity substrate or SOI**
2. **Limit the in pixel number of devices, use anti-latch-up tricks : spaced gates**
3. **Limit npnp (SCR) parasitic structures >> single Transistors structures in pixel may be efficient , we'll see this**

- **Ionizing radiation effects**

1. **Alternative gate oxides (Hafium Oxide….etc ...) to reduce gate leakage current**
2. **And Vt shift should be studied of the process**

- **NIEL effects :**

1. **Small dimensions of the active detecting volume (charge collecting length << trapping length)**
2. **Increase electric field in the structure by dimension reduction and no decrease in bias voltage**
3. **This is possible by improving the gate oxide : high field , high K , high bandgap**

- **et al.**

Vertex detectors : beyond the CMOS sensors pixel detectors

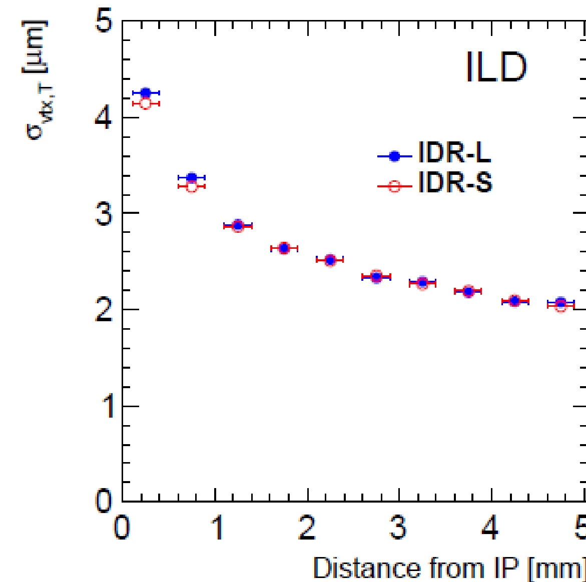
Pixel detector improvements :

- **ILC incident beam with small radius**
- **Layers could be very close (~ 1 cm) to the IP**
- **6 layers , reconstruction by brute force methods**
- **High point to point resolution σ (r,Φ,z) ~3 μm (Interim Design Report , 2020, lower figures)**

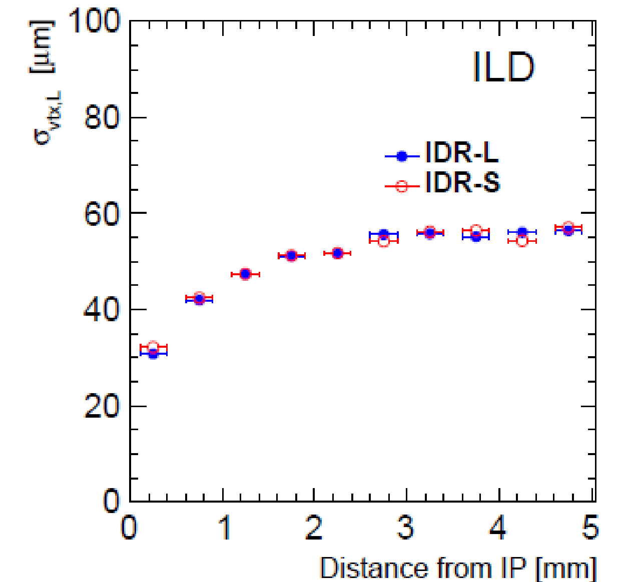
- **Primary vertex from the beam**

spot position : O(10 nm)

- **Reduction of beam pipe radius**
- **Beam size at the IP : 640 nm x 5.7 nm**



(a)



(b)

Vertex detectors : beyond the CMOS sensors pixel detectors

One solution : single MOS transistor pixel with buried gate :

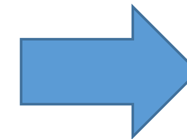
- **Constraints : radiation length X0 is 9.370 cm in silicon** (https://pdg.lbl.gov/2009/AtomicNuclearProperties/HTML_PAGES/014.html)
- **100 microns of silicon, thinned wafer 0.01 cm = 0.01/51 = 0.0010 radiation length**
- **This means that we could increase the wafer thickness for better mechanical strength**
- **Or use a long and light holding material base/substrate**
- **The reduction in pixel active height will decrease the aspect/ratio (height/pitch) and increase the electric field in the detection volume**
- **Requirements : CMOS process with < 0.1 micrometer line feature**
- **Epitaxial with a Ge On Si starting wafer or Selective Ge On Si epitaxy (we'll develop this later)**

Vertex detectors : beyond the CMOS sensors pixel detectors

Pixel Size (μm^2) X Thickness (μm)	E_{avg} (keV)	E_{MPV} (keV)	Ratio avg (%) $(E_N/E_p)^*$	Efficiency (E_{Th}= 500eV)
1 * 1 *10	3.28	2.17	4.74	99.3
1 * 1 * 20	6.76	4.89	4.9	99.82
1 * 1 * 30	10.86	7.84	-	>99
1 * 1 * 40	14.36	9.68	-	>99
1 * 1 * 50	17.98	13.21	-	>99
10 * 10 * 10	3.26	2.15	0.994 1	99.9
10 * 10 * 50	16.68	13.17	2.08	>99
10 * 10 * 100	34.76	24.3	2.35	>99

V. Kumar Master thesis GEANT4 simulation with 130 GeV pions on a silicon target 500 eV ~ 140 e threshold)

1. **Lowest pixel size with aspect ratio of 1/10 . Detection efficiency ~ 99.3**
2. **The noise level should be equivalent or lower than that of MIMOSAs ~ 12 e**
3. **There should be margin to reduce the pixel thickness to 5 micrometers**



Substrate=Si wafer+Si epilayer (5 microns)+Ge epilayer +Si epilayer

Vertex detectors : beyond the CMOS sensors pixel detectors

Table 1. Size of the pixels, area, number of hit per unit area (N), address length for a pixel, data flow.

Size (lateral dimensions)	Resolution (first order binary)	Area (array)	Number of pixels: N_p in an array	Number of hits per unit area and per second $=n/S_a$	Address length in bits $L=\log(N_p)/\log(2)$	Data flow in bits/second
1×1 $\mu m \times \mu m$	~ 1 µm	10 cm squared	10^9	N	Approximately 30	$30 \times N$
10×1 $\mu m \times \mu m$	~ 3 µm	10 cm squared	10^8	N	Approximately 27	$27 \times N$
10×10 $\mu m \times \mu m$	~ 10 µm	10 cm squared	10^7	N	Approximately 24	$24 \times N$

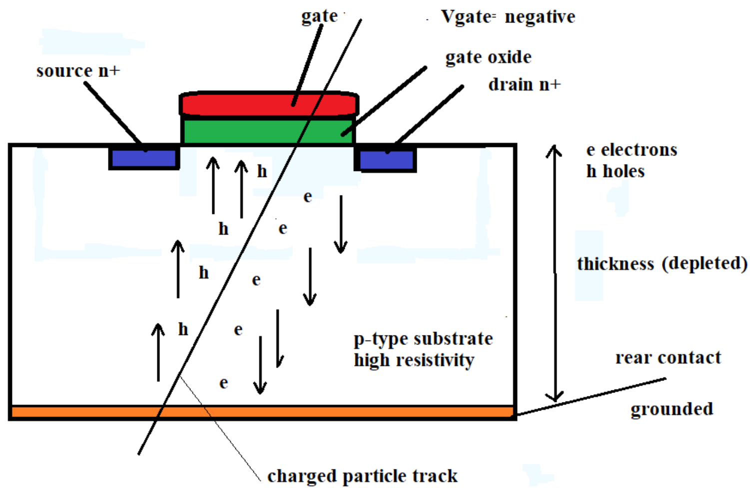
In this table the dataflow is computed versus pixel size

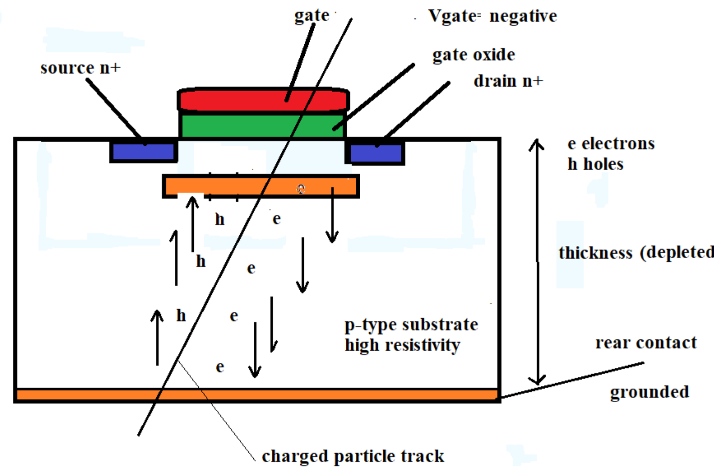
- It depends on the hit rate
- Less dependant on the number of pixels if we eliminate zeros on the pixel chip
- So if the 1 x 1 mm squared are technologically feasible the advantage is clear

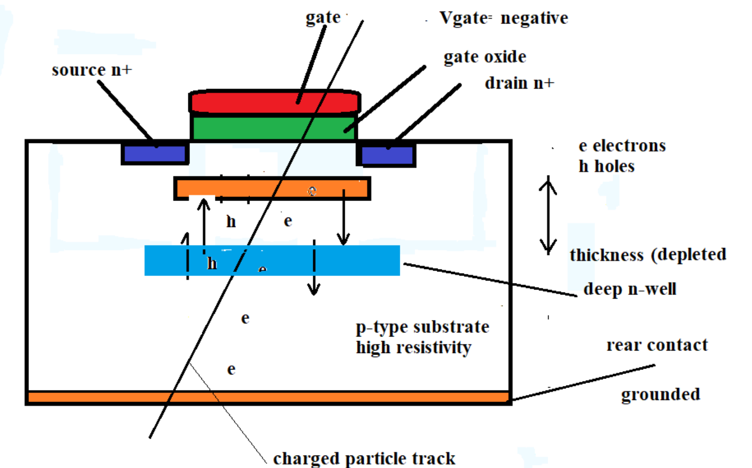
Setting a limit on power : 1 cm2 == 10^8 pixels then 10^8nW/cm2 leads to 1nW per pixel

- No power dissipation during detection (as in standard CMOS sensors)
- Readout time per pixel of 10 ns at most
- Readout time of 100 µs , 10^6 pixels read per scan, 100 frames per cm2
- Only one pixel read after each other the read bias current is 100 µA ~ 0.3 mW/frame
- Power 300mW/cm2 there is little margin !!!

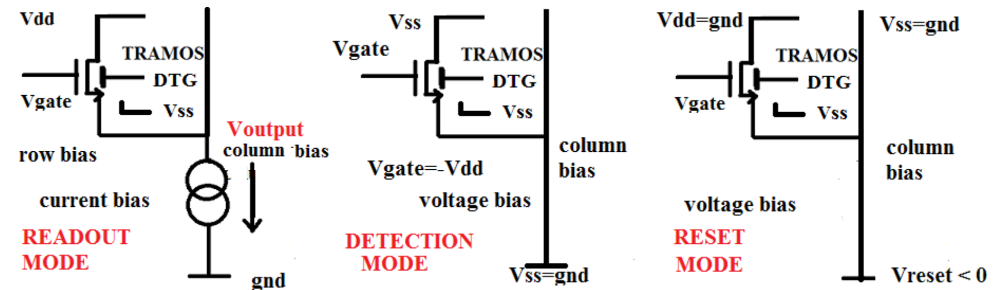
Vertex detectors : beyond the CMOS sensors pixel detectors







With a negative voltage on the gate holes drift to the buried gate (orange, made of Ge or SiGe and modulate the source to drain current when an positive voltage is put on the upper gate, Deep n-well optional

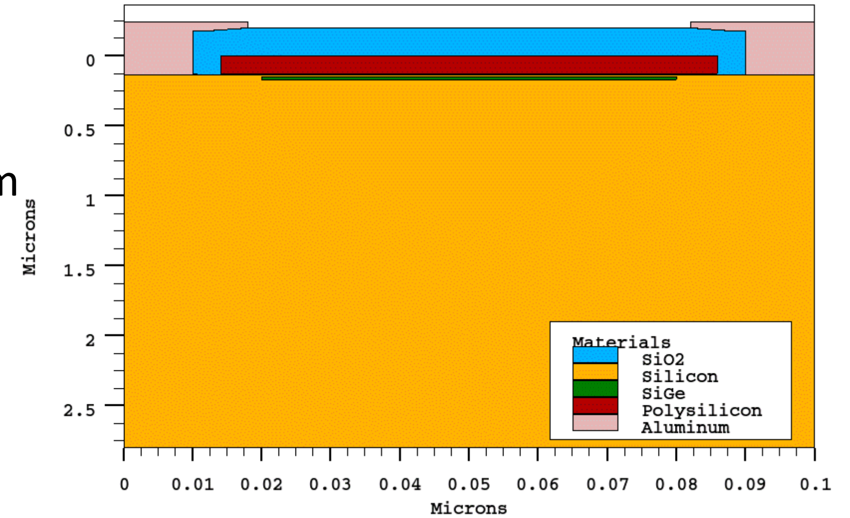


Vertex detectors : beyond the CMOS sensors pixel detectors

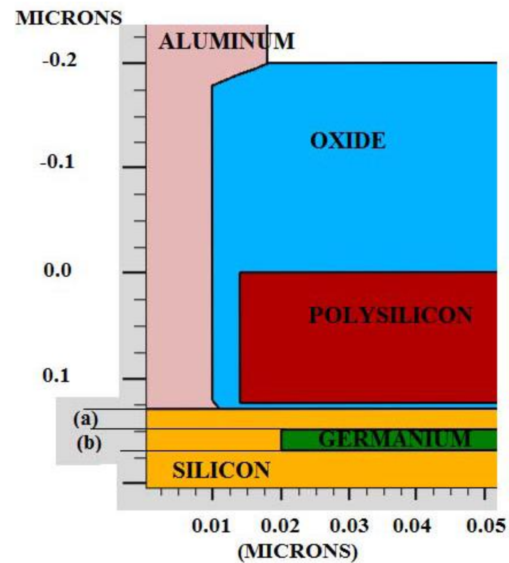
- Device simulations , general simulations

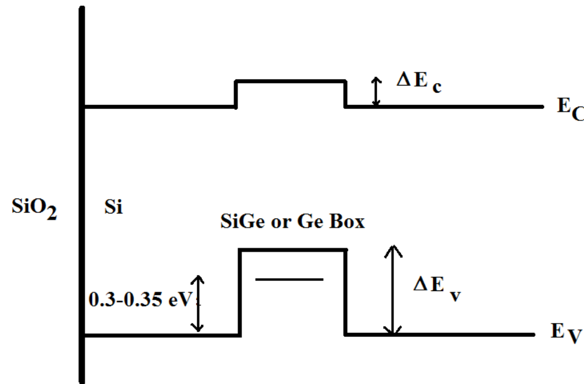
L (µm) Gate Length	Buried Gate transconductance (µA/V)	Buried Gate-Upper Gate capacitance	ΔV (buried gate) for 80 e charge deposited	ΔV (source) for 80 e charge deposited and a 5 kohms source resistance	Conversion Factor in µV/e (source of the transistor) 5 kohms source resistance
1 µm	52	5.31 fF	3.01 mV	785 µV	9 µV/e
0.5 µm	60	2.65 fF	6.00 mV	1.56 mV	19.5 µV/e
0.25 µm	55	1.32 fF	12.0 mV	3.3 mV	41.25 µV/e
0.1 µm	60	0.531 fF	24.1 mV	7.23 mV	90.4 µV/e
Gate width 1µm	Simulated using Silvaco ATLAS	Gate width 1µm	Silvaco ATLAS	Silvaco ATLAS simulations	Silvaco ATLAS , Gate width 1µm simulations

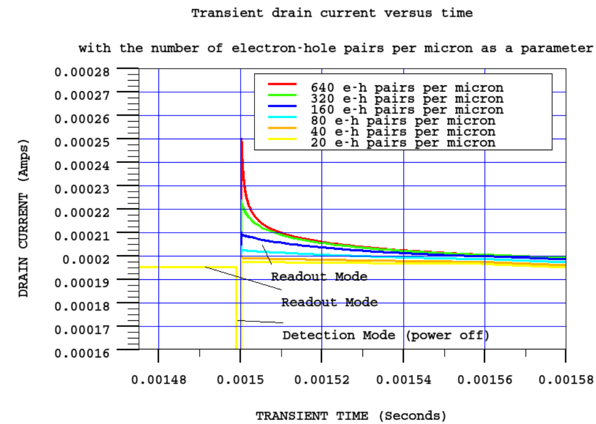
Thickness ~ 2 µm

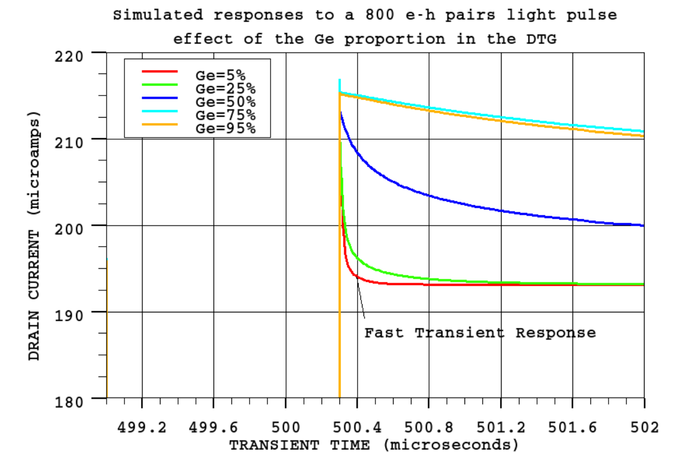


- The buried Ge gate is 20 nm thick for a 1 micrometer width (2016)









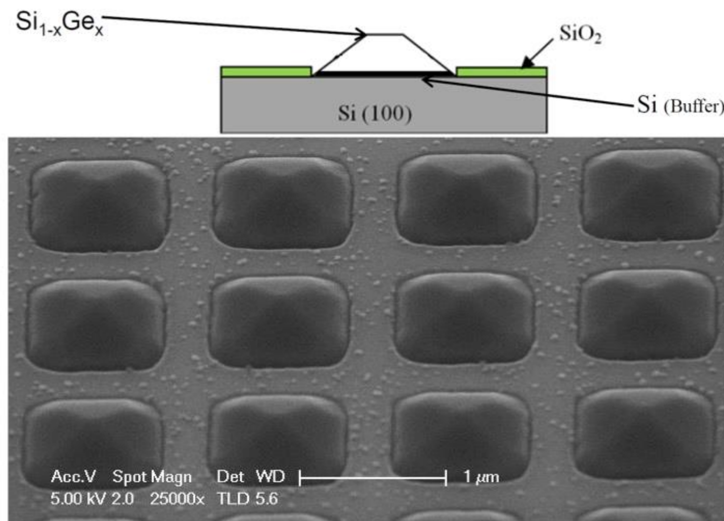
Vertex detectors : beyond the CMOS sensors pixel detectors

Simulations , conclusions

- readout should be < 100 µs >>> because of the time constant in readout mode , new simulation results show a detection time constant > 20 µs
- We have to reduce drain current (power) . This may done by operation in triode mode> IDS can set by the column current source
- The quantum box should contain at least 50 % Ge to be effective
- It should not be a relaxed structure but strained, for band offset and defect free considerations

Vertex detectors : beyond the CMOS sensors pixel detectors

- Technology, fabrication :



- Selective epitaxy using Ultra High Vacuum Chemical Vapor Deposition
- Facilities of the CNRS/ Centre de Nanoscience et de Nanotechnology
- Thin layers ~ 10 nm
- CMOS process may be studied at CNRS/LAAS for compatibility with standard CMOS processes
- Characteristics : pyramidal structures or planar
- Other processes have been investigated but only give thick layers

FWHM = 100 nm so not very adequate

The best full wafer epitaxy Si on Ge on Si on Si substrate.

1. Issues :
2. surface roughness
3. Contamination
4. Effect of thermal treatments such as high temperature oxidization
5. Using alternative Oxides sur as HfO2 to reduce possible leakage current , but Radiation hard ?

Vertex detectors : beyond the CMOS sensors pixel detectors

2020 DOTPIX COLLABORATION :

CEA
IRFU/DEDIP, IRAMIS and
CNRS/C2N and others
Use UHV-CVD to grow a Ge thin films on Si

Planning this study

- Epitaxial and structural characterizations :
- CNRS / C2N
- Electrical characterizations : latency evaluation
- How effective is the quantum well ? IRFU
- We acquiring a cryostat for this purpose

  - Good crystalline quality
  - Roughness sufficiently low
  - Some hole in the material
  - May be corrected by improved cleaning and oxidization

C2N

Substrate Si n-doped <100> Resitivity: 0,3-5 Ω.cm-1
epi-ready quality

Cleaning

- Diluted HF (1min)
- H_2SO_4/H_2O_2 (10min)
- Diluted HF (1min)

Protective chemical oxidation
-$HCl/H_2O_2/H_2O$(10min) → 0,6nm SiO_2

Vacuum deoxidization (10^{-7} à 10^{-8}mbar)

Ultra-high vacuum CVD growth

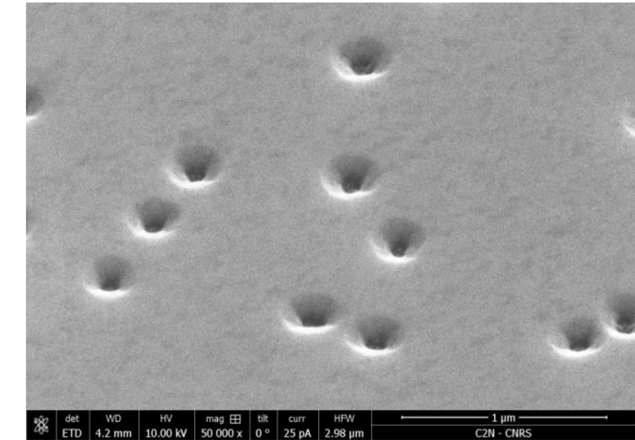
- <u>Si Buffer</u>

SiH_4 flux=7sccm
P = 3.10^{-4} Torr
Temperature 700°C

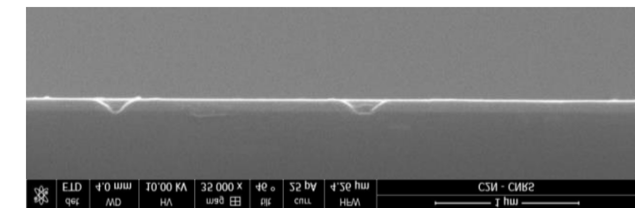
- <u>Ge deposition</u>

GeH_4 flux =10sccm
P = 3.10^{-3} Torr
Temperature 330°C

Characterizations
MEB and Rheed in-situ



SEM image SEM top view tilt = 45°



SEM image tranverse view

sccm : standard cubic cm per minute

- What's next :
- MOS structures with alternative oxide studies (ongoing)
- MOS process compatible with future Ge On Si substrates (RTB/CNRS)
- DotPIX array design and test whenever possible
- Simulations/evaluation of timing characteristics

Selective bibliography :

- N. T. Fourches, "Ultimate Pixel Based on a Single Transistor With Deep Trapping Gate," IEEE Transactions on Electron Devices, vol. 64, pp. 1619-1623, Apr. 2017. [Online]. https://doi.org/10.1109/TED.2017.2670681
- N. Fourches et al., "Limits in point to point resolution of MOS based pixels detector arrays," Journal of Instrumentation, vol. 13, pp. C01011--C01011, Jan. 2018. [Online]. https://doi.org/10.1088%2F1748-0221%2F13%2F01%2Fc01011
- Mathieu Halbwax, "Elaboration et caractérisation de couches de germanium épitaxié sur silicium pour la réalisation d'un photodétecteur en guide d'ondes,« PhD Thesis. 2004.
- R. Cariou, J. Tang, N. Ramay, R. Ruggeri, and P. Roca Cabarrocas, "Low temperature epitaxial growth of SiGe absorber for thin film heterojunction solar cells," Solar Energy Materials and Solar Cells, vol. 134, pp. 15-21, 2015. [Online]. http://www.sciencedirect.com/science/article/pii/S0927024814005984

Vertex detectors : beyond the CMOS sensors pixel detectors
SUMMMARY and PROSPECTS

1. A new generation of pixel detectors is under study
2. Better track discrimination close to the interaction point
3. Much improved and precise pT reconstruction
4. It will meet the needs for ILC requirements in terms of precision in track and vertex reconstruction
5. It may be useful for study (indirect or not) the invisible or undectable decays
6. Higgs physics and Dark Matter Investigations

Extra views

Couche de Ge(60nm environ) 2D avec beaucoup trous

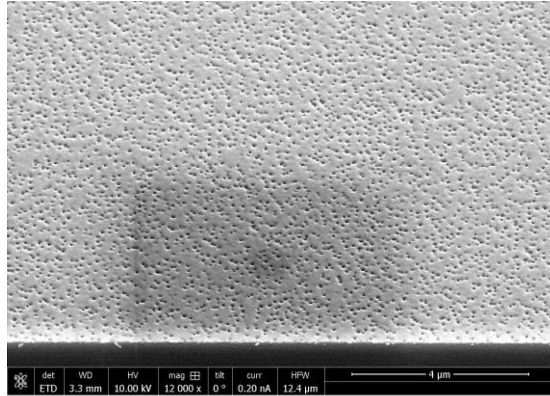


Image SEM tilt 45°

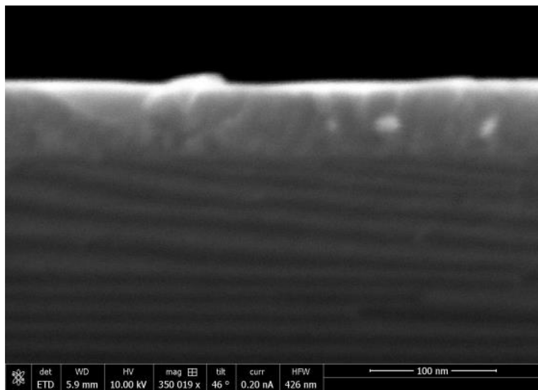


Image SEM tilt 90°

Couche de Ge(100nm environ) 2D avec moins trous

Amélioration du procédé de désoxydation

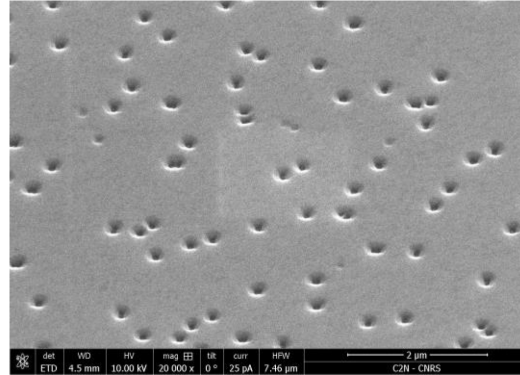


Image SEM tilt 45°

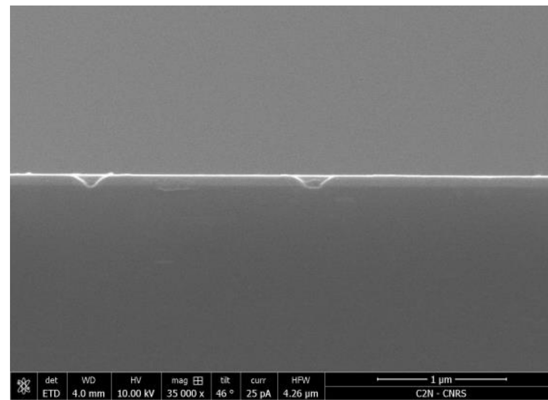


Image SEM tilt 90°

Couche de Si(100nm environ) partie en 3D mais avec une densité de trous pour le moment satisfaisante pour continuer

Amélioration du procédé de nettoyage et substrat épi-ready d'une boite neuve

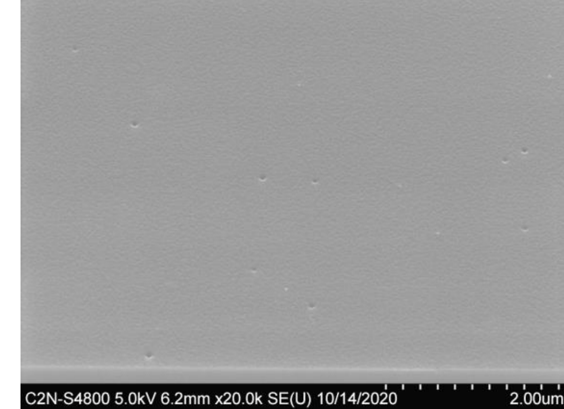


Image SEM tilt 45°

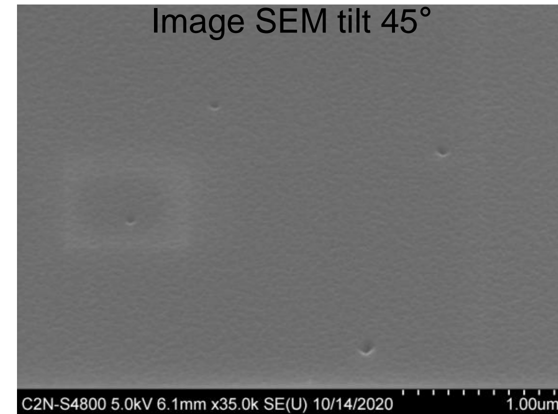


Image SEM tilt 45°