

# Performance Evaluation of Stiched Passive CMOS Strip Sensors

Marta Baselga, Leena Diehl, Ingrid-Maria Gregor, Marc Hauser, Tomasz Hemperek, Jan-Cedric Höning,  
**Sven Mägefessel**, Ulrich Parzefall, Arturo Rodriguez, Surabhi Sharma, Dennis Sperlich, Tianyang  
Wang, Liv Wiik-Fuchs

Albert-Ludwigs-Universität Freiburg



# Passive CMOS strip detectors

First stitched strip sensors produced on 8" wafer by a commercial foundry

- ▶ L-Foundry 150 nm process (deep N-well/P-well)
- ▶ Up to 7 metal layers
- ▶ Wafer Resistivity:  $> 2 \text{ k}\Omega\cdot\text{cm}$
- ▶ Float-Zone silicon

Frontside process: **Reticle stitching**

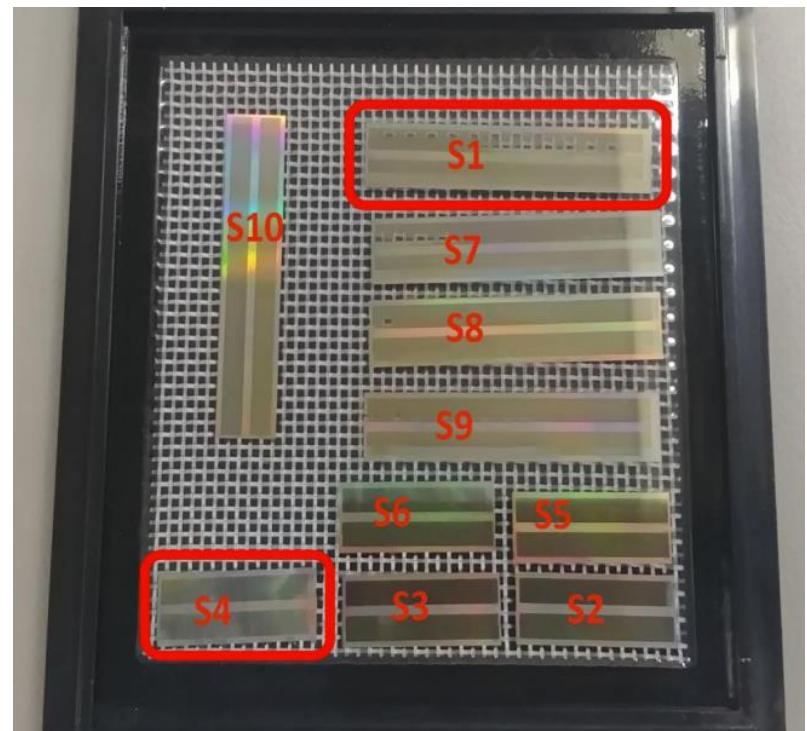
➡ larger sensors

Two sensor lengths:

- ▶ 2 cm (short sensor)
- ▶ 4 cm (long sensor)

Two different batches:

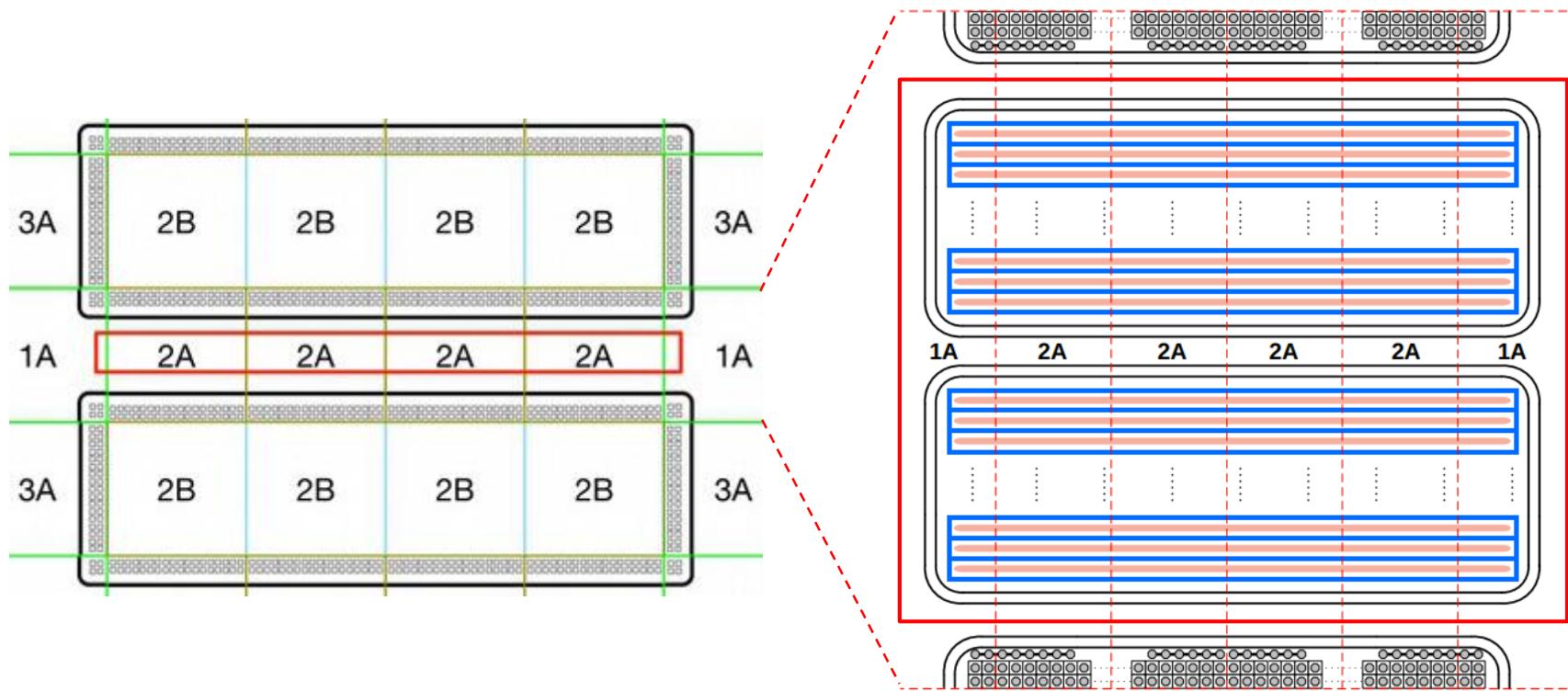
- ▶ low concentration backside implant without metallization
- ▶ higher concentration backside implant with metallization



# Passive CMOS strip detectors

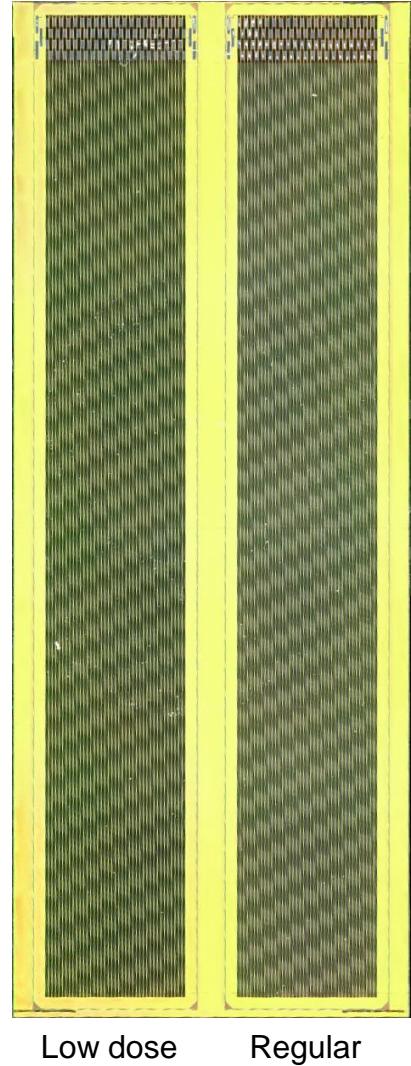
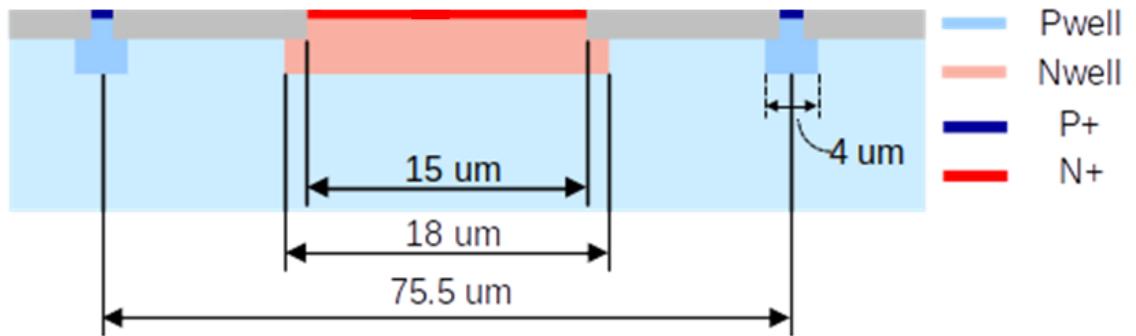
## Stitching process

- ▶ Strip sensor produced with 1A and 2A reticles
- ▶ Stitched every 10mm along strip length
- ▶ Strip pitch of  $75.5\mu\text{m}$

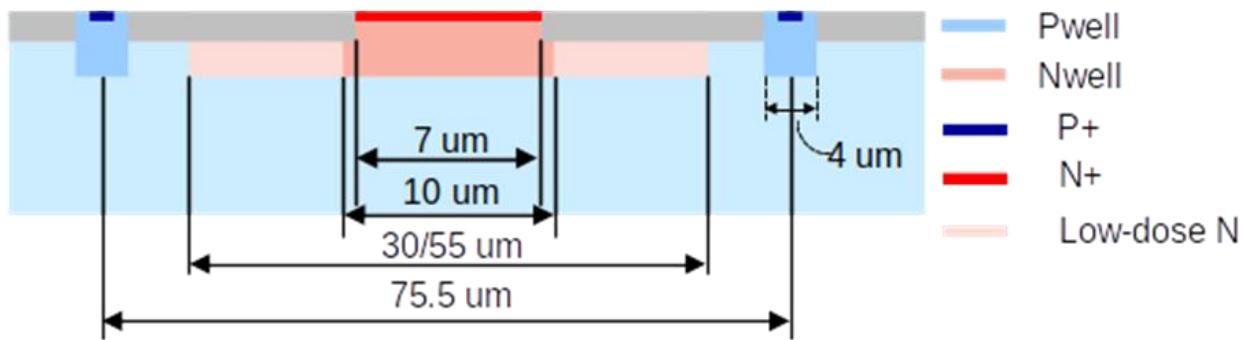


# Passive CMOS strip detectors

Regular design



Low dose design



# IV Results

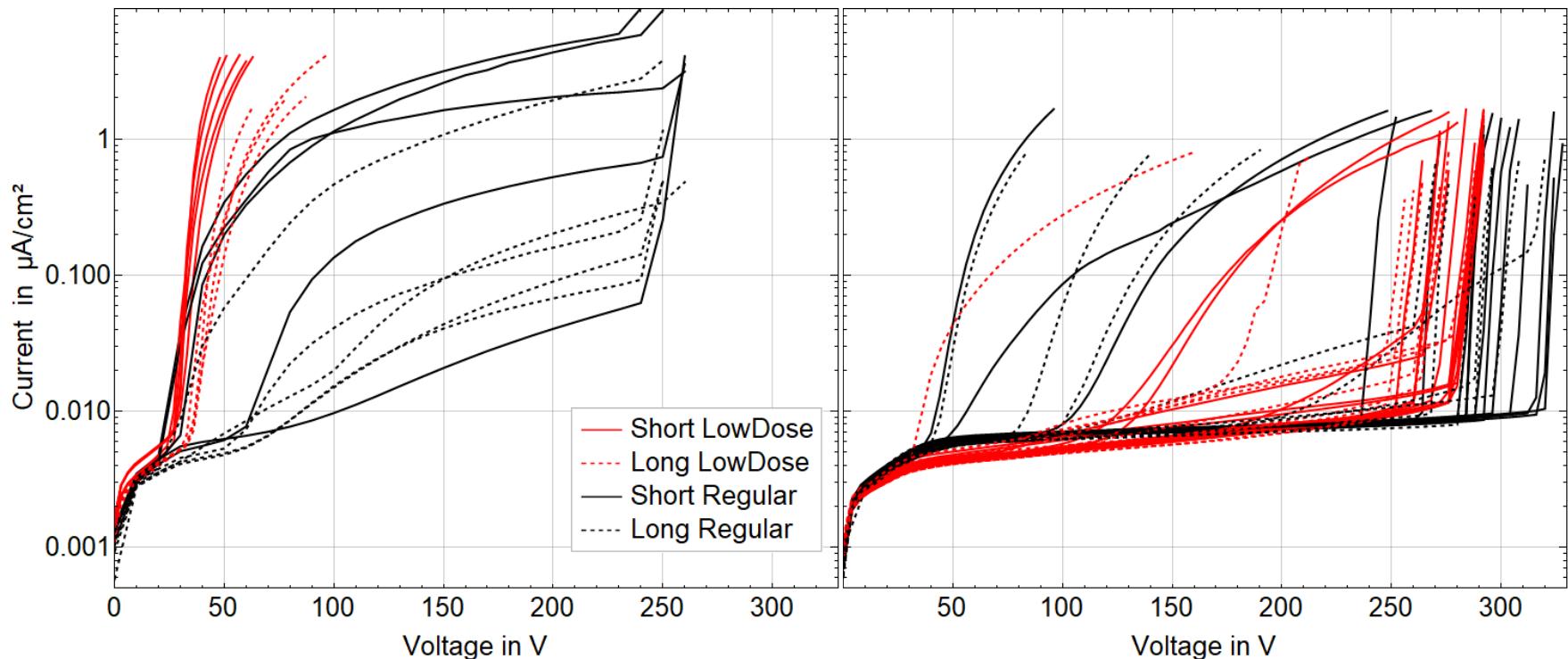
## First Batch:

- ▶ Early breakdown for both designs
- ▶ Steeper current increase for regular design than for low dose

## Second Batch:

- ▶ Breackdown voltage improved to >220V
- ▶ Only few bad sensors for both designs

➡ Clear improvement



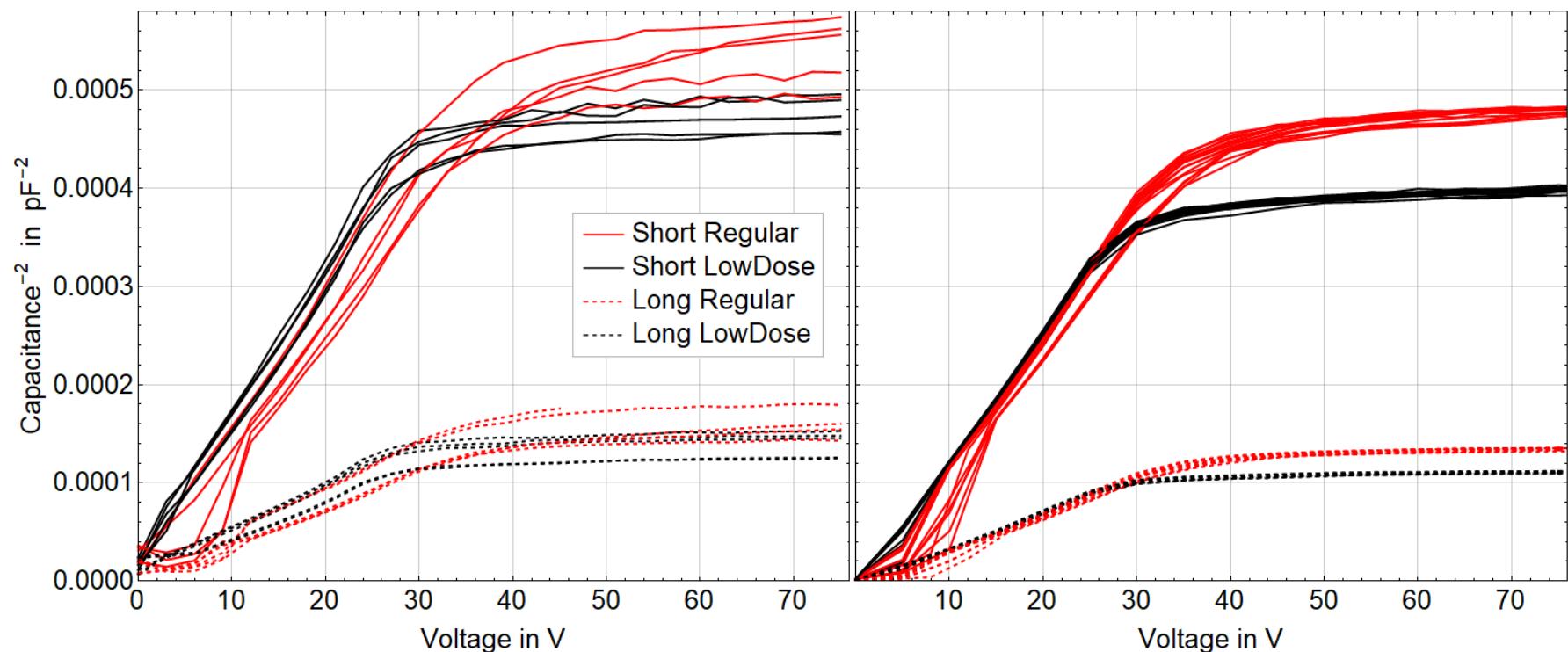
## First Batch:

- ▶ Full depletion around 30-40V
- ▶ Stronger pronounced interstrip depletion for regular design

## Second Batch:

- ▶ Improved homogeneity
- ▶ Lower capacitance for Low Dose design

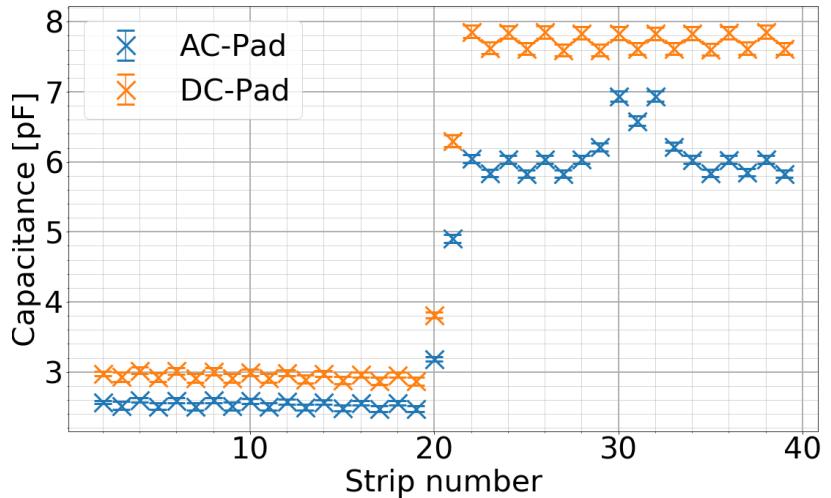
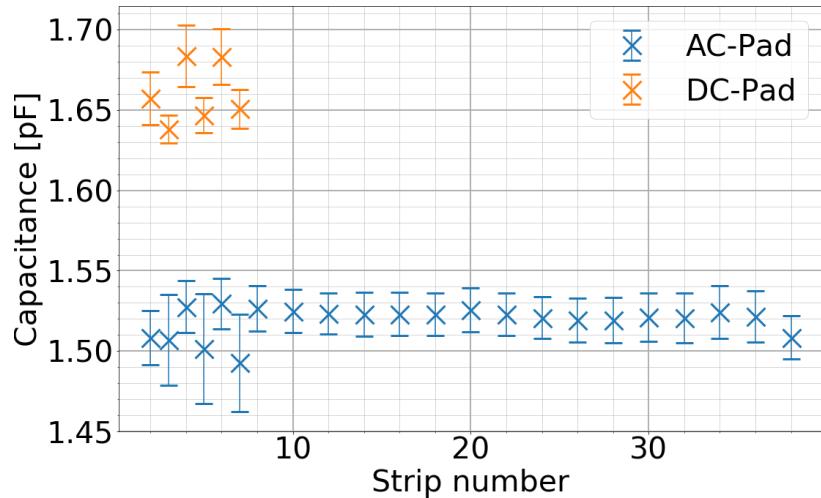
➡ Less noise



# Interstrip capacitance results

Only first batch available

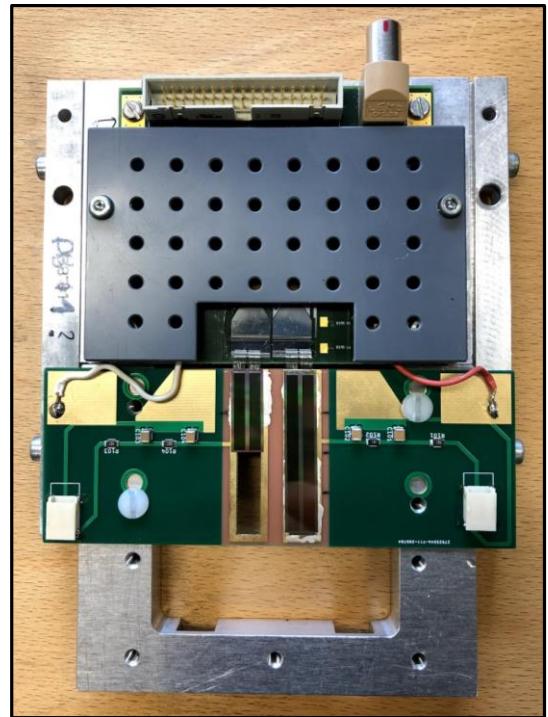
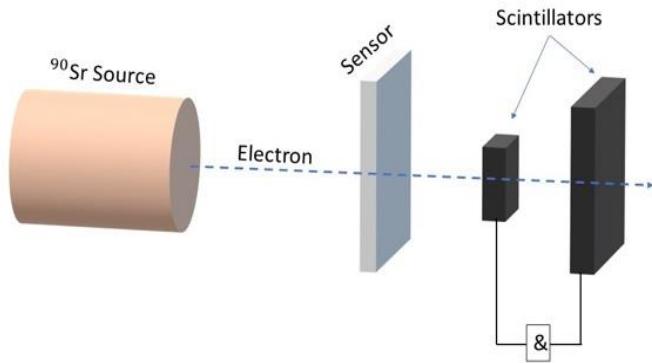
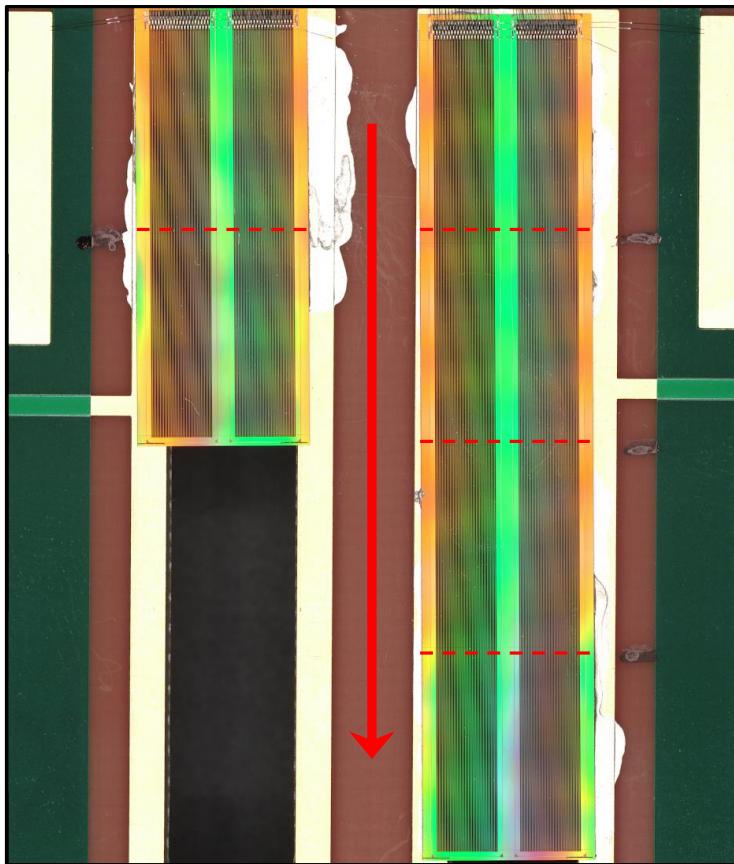
- ▶ Regular
  - ▶ Constant along strips
- ▶ Low Dose
  - ▶ Two different capacitances according to low dose implant widths



All electrical tests didn't show any issues with stitching

# Source measurements

- ▶ Both strips designs bonded to one chip
- ▶ Voltage scan up to 100 V
- ▶ Scan through stitched areas

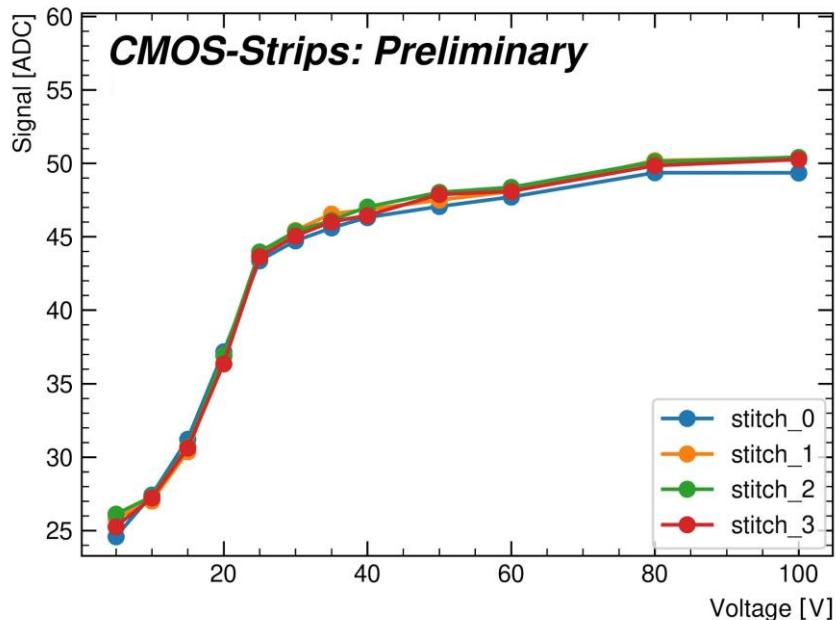


# Source Measurements Results - Signal

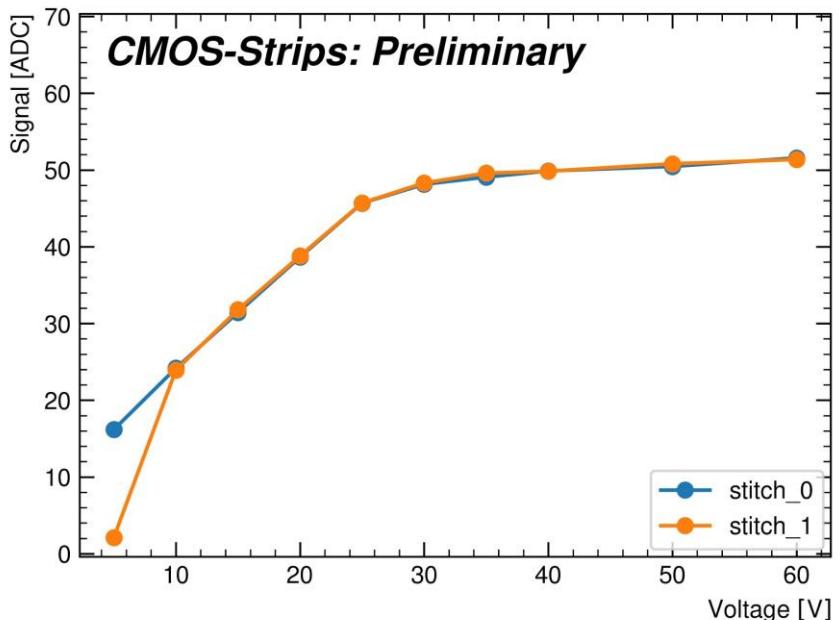
## Regular design

- ▶ Strong charge collection efficiency increase until full depletion
- ▶ Smaller increase for overdepletion
- ▶ No difference between the stitches

Long



Short

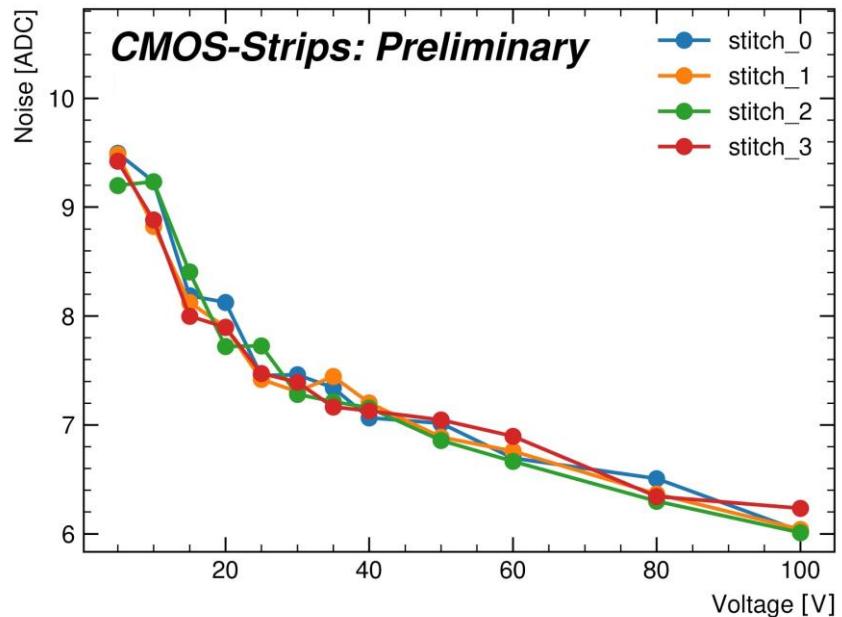


# Source Measurements Results - Noise

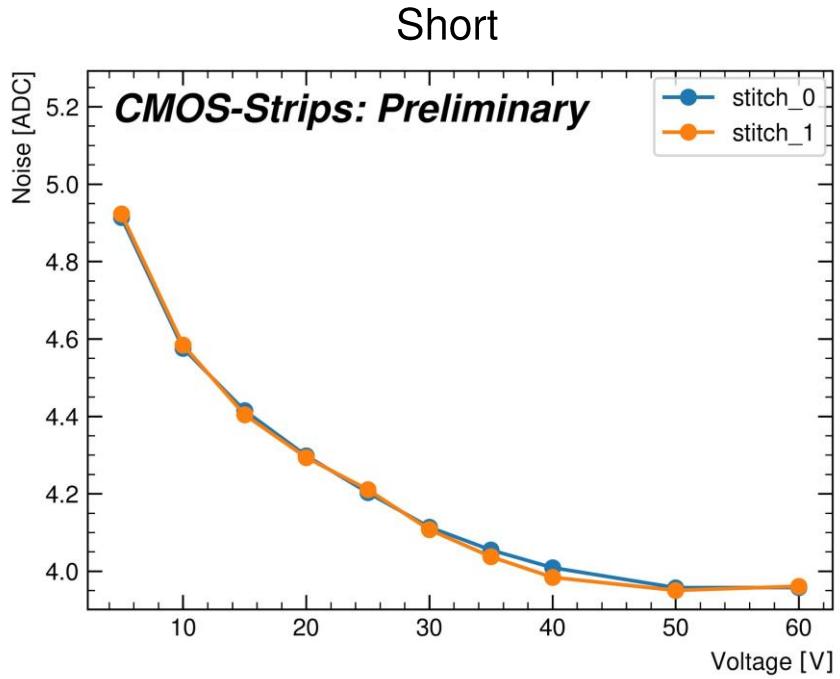
## Regular design

- ▶ Decrease with higher voltage
- ▶ Low signal-to-noise ratio of 45 to 7/4
- ▶ No difference between the stitches

Long



Short

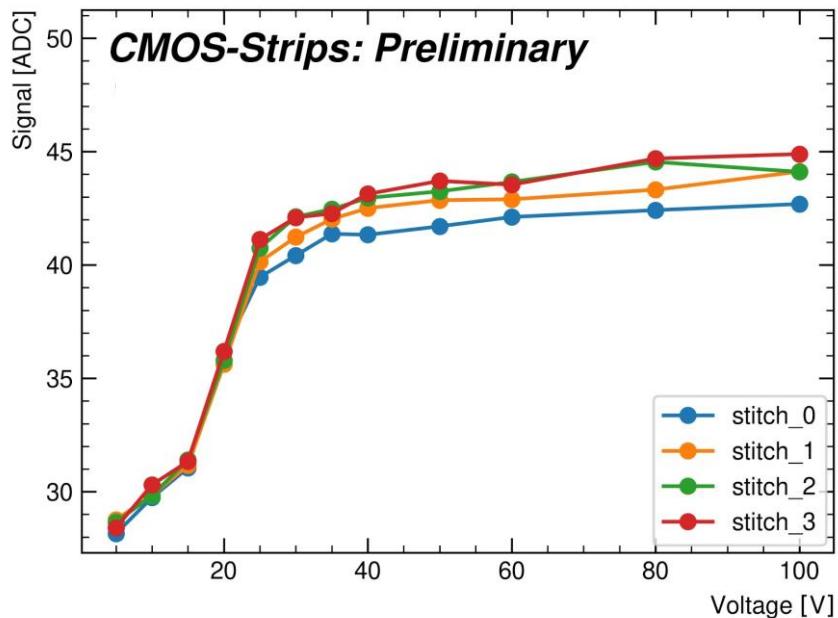


# Source Measurements Results - Signal

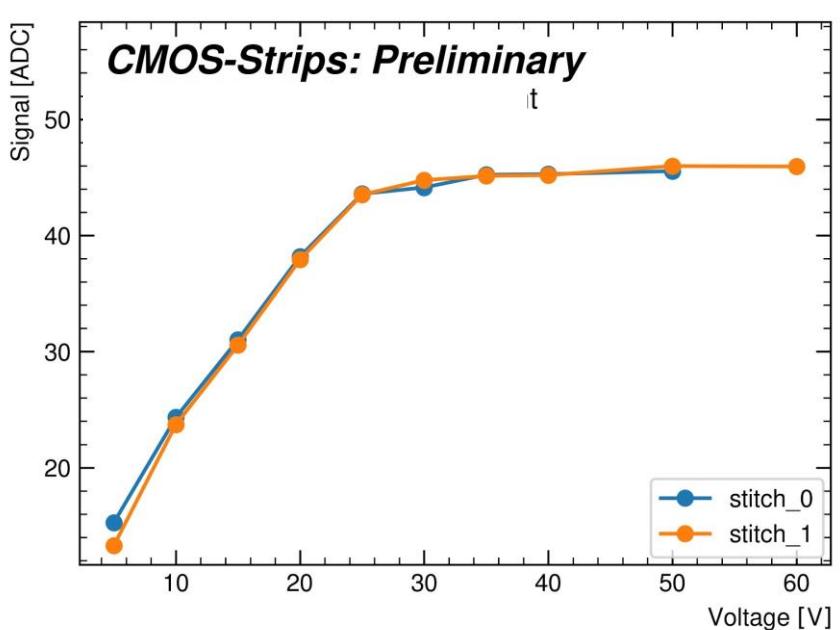
## Low dose design

- ▶ More inhomogeneous than regular design
  - ▶ Maybe due to different strip designs or different masking
- ▶ Less increase for overdepletion

Long



Short

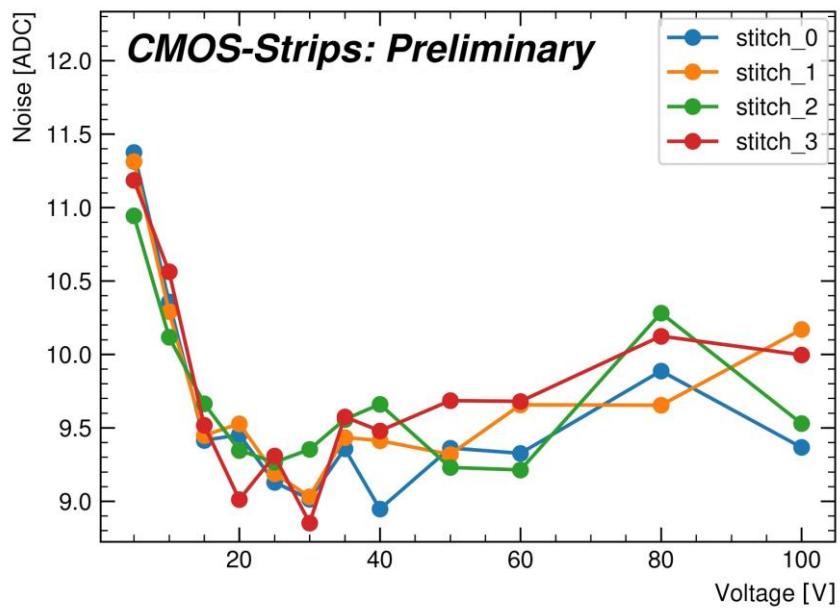


# Source Measurements Results - Noise

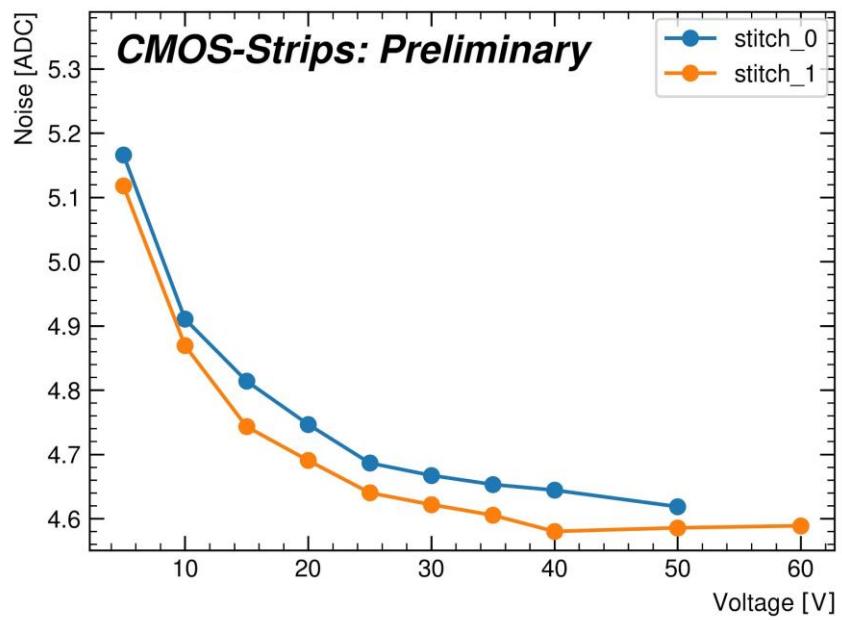
## Low dose design

- ▶ Higher than for regular design
- ▶ Stronger fluctuations
- ▶ Maybe due to different implant width within the sensor

Long



Short



# Summary & Outlook

## Summary:

- ▶ Two batches of stitched passive CMOS sensors electrically tested
  - ▶ Large improvement for second batch
  - ▶ Breakdown way higher than depletion
- ▶ First batch source measured
  - ▶ Expected signal behaviour
  - ▶ Low signal-to-noise-ratio

## **Stitching works**

## Outlook:

- ▶ Complete measurements of second batch
- ▶ Irradiation studies