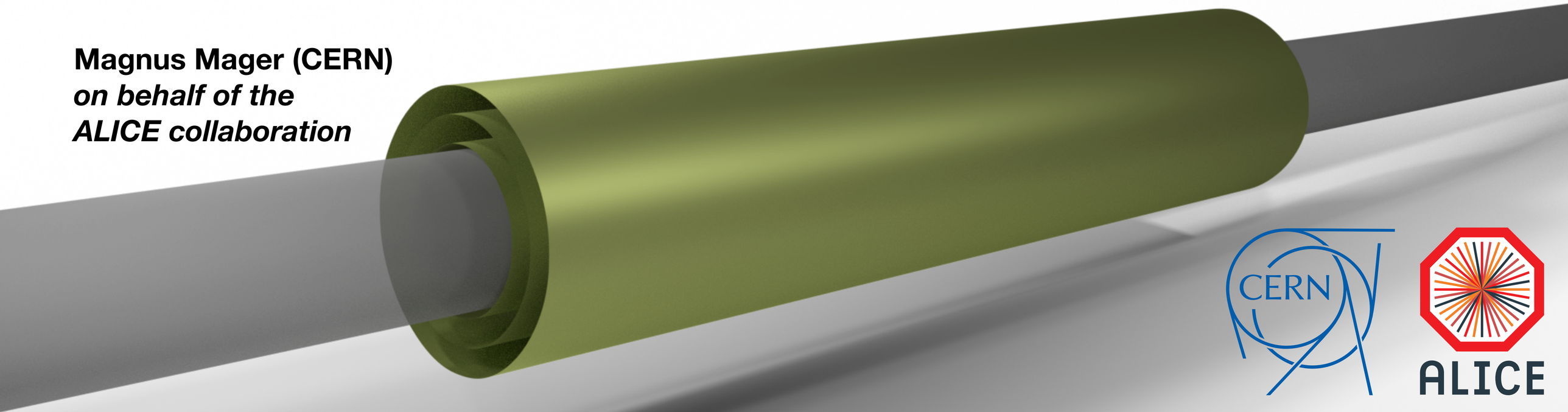
LCWS2021

INTERNATIONAL WORKSHOP ON FUTURE LINEAR COLLIDERS

Monolithic Active Pixel Sensor R&D in 65 nm for high-resolution, minimal-mass, wafer-scale, bent tracking detectors

18.03.2021

Magnus Mager (CERN)
on behalf of the ALICE collaboration

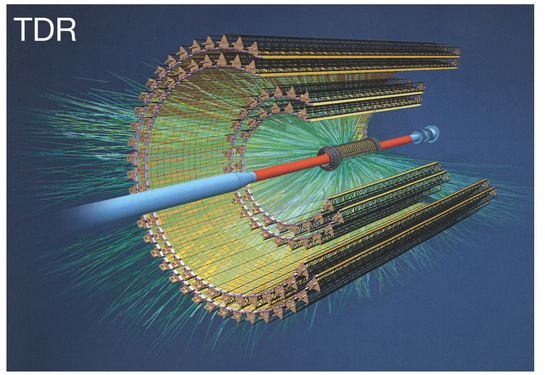


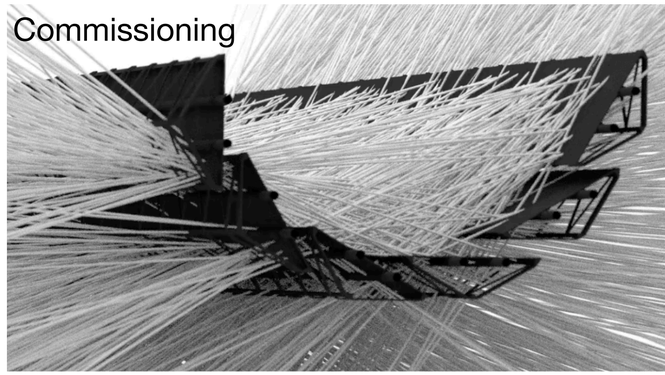
CERN

ALICE

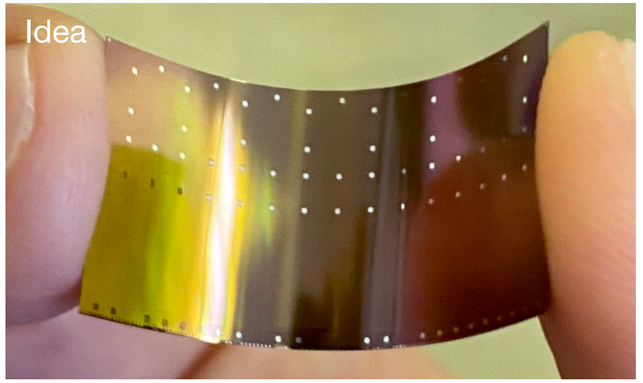
Outline

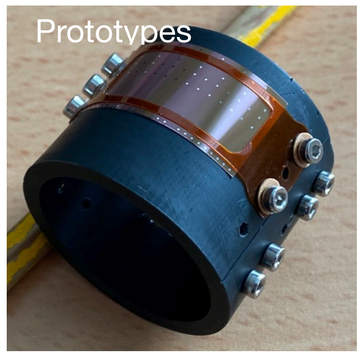
- Starting point: **ALICE ITS2**
  - short review of the detector
  - motivation to go further

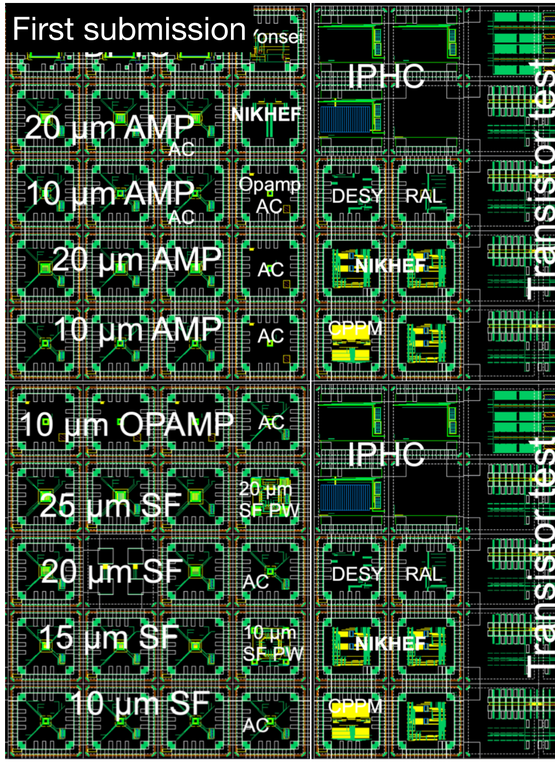




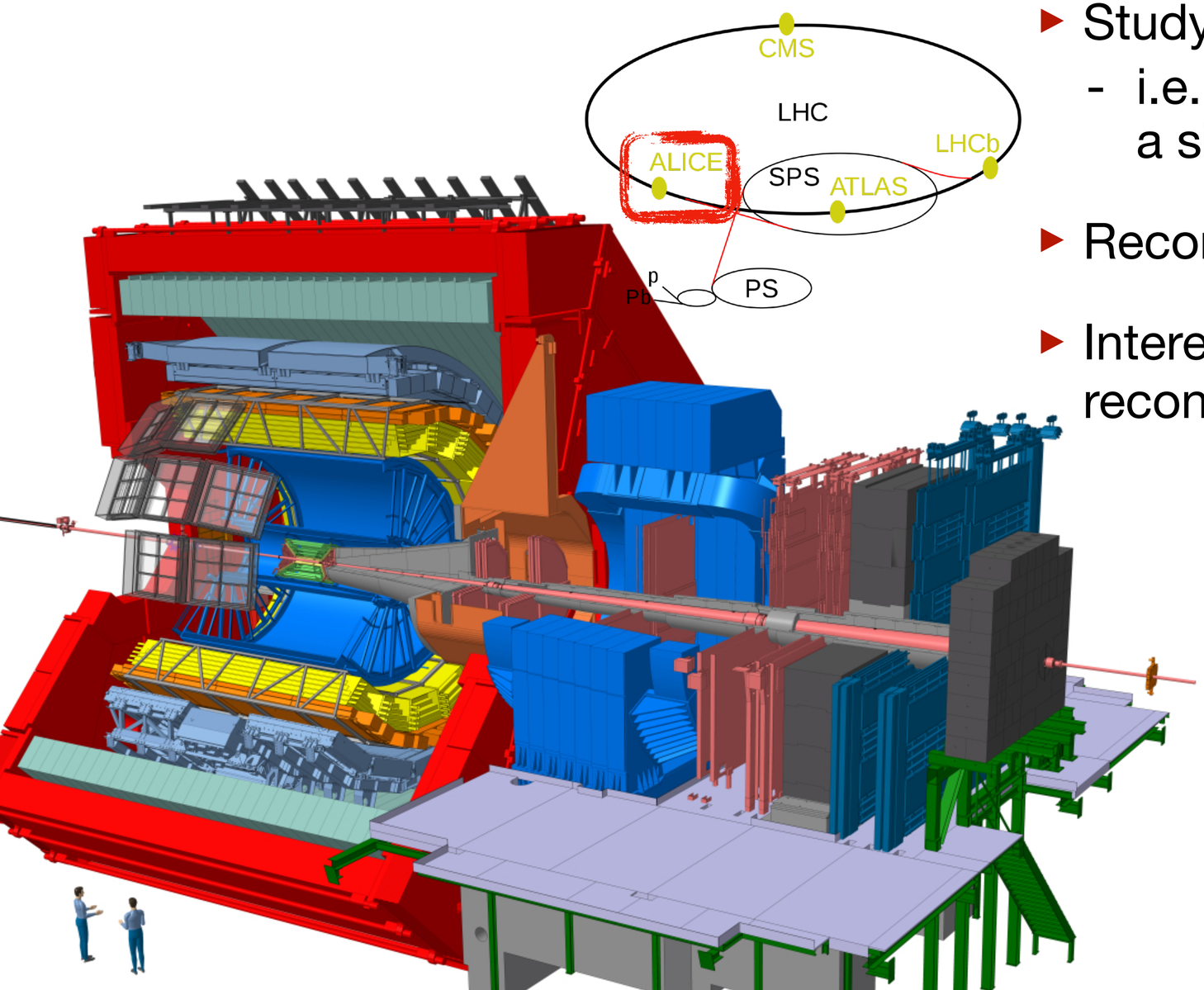
- **ALICE ITS3** (target: LHC LS3)
  - detector and project overview
  - sensor development in 65 nm
  - beam tests with bent MAPS



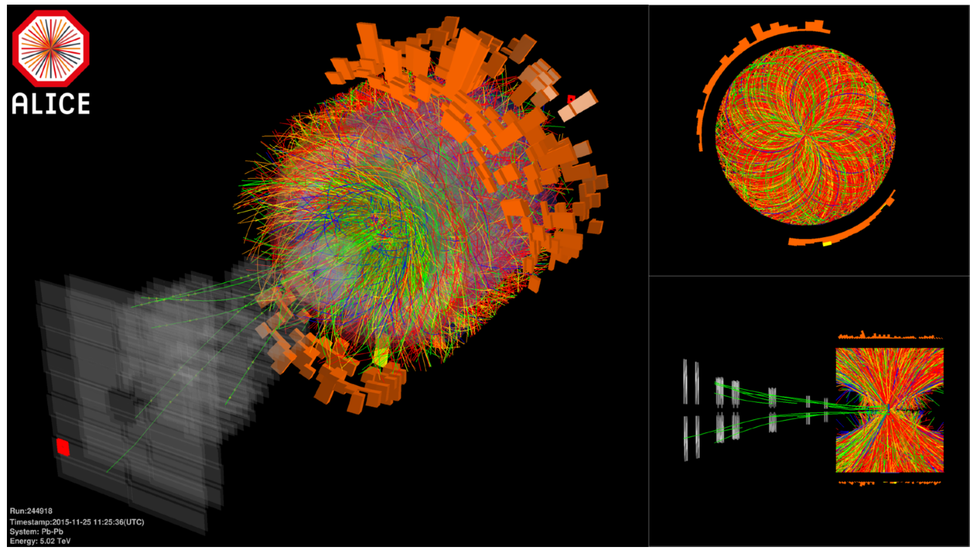




ALICE
Detector and main goals

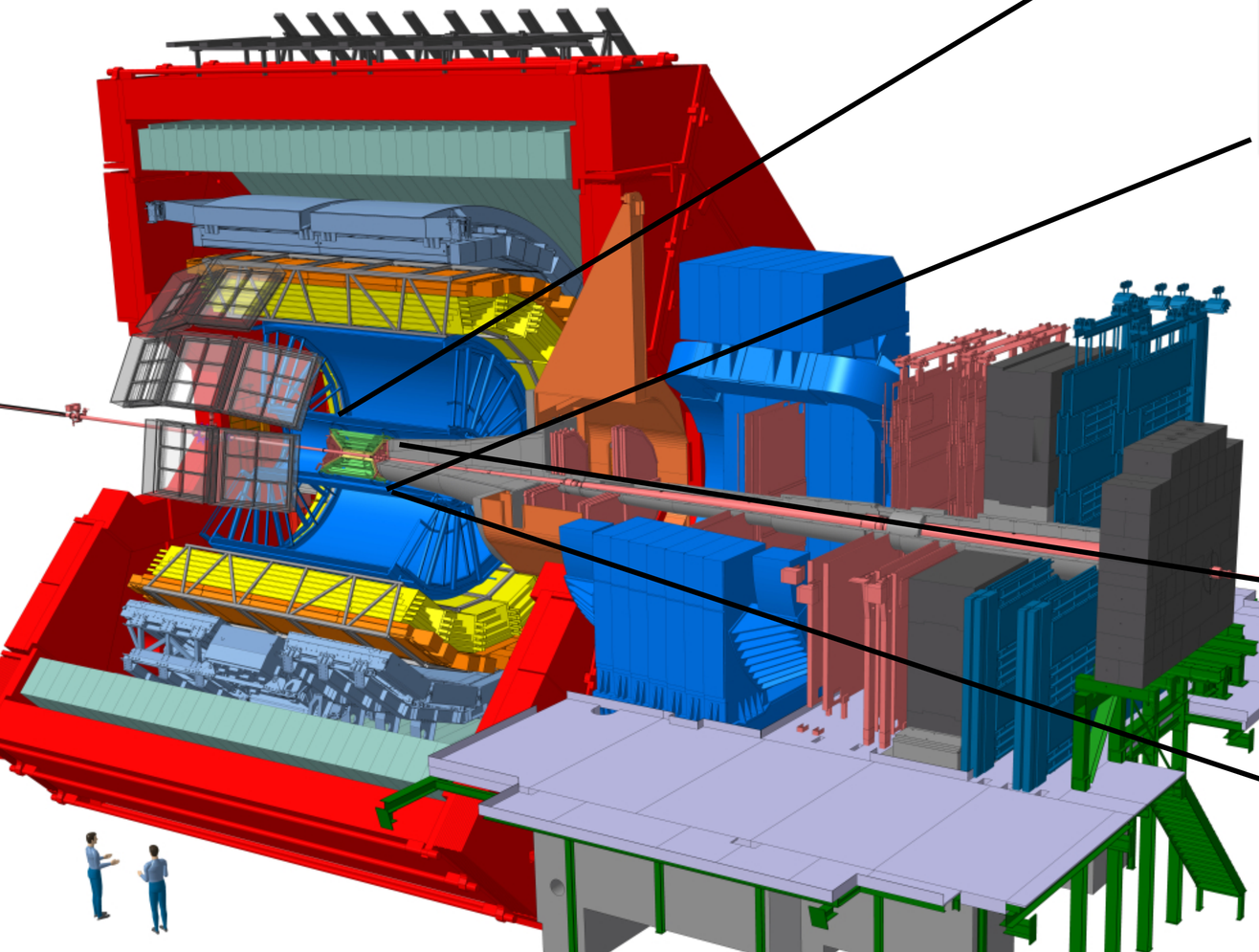


- Study of QGP in heavy-ion collisions at LHC
  - i.e. up to O(10k) particles to be tracked in a single event
- Reconstruction of charm and beauty hadrons
- Interest in low momentum (≲1 GeV/c) particle reconstruction

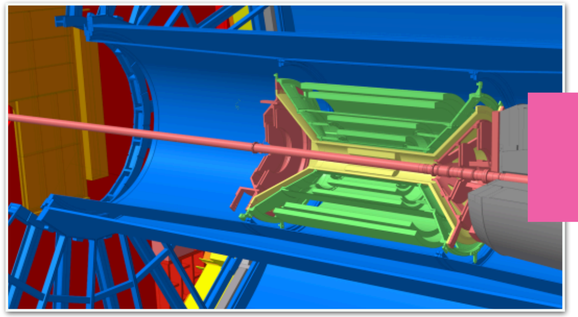


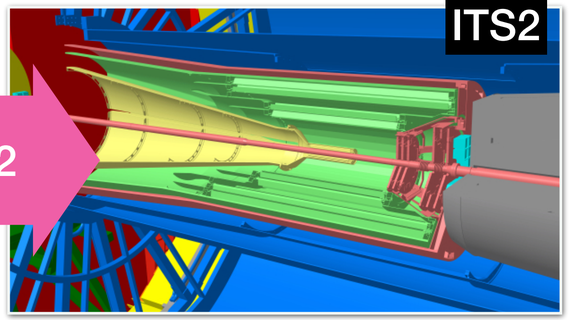
ALICE today

LS2 upgrades with Monolithic Active Pixel Sensors (MAPS)



Inner Tracking System





LS2

6 layers:
- 2 hybrid silicon pixel
- 2 silicon drift
- 2 silicon strip

Inner-most layer:
- radial distance: 39 mm
- material: $X/X_0 = 1.14\%$
- pitch: $50 \times 425\ \mu m^2$

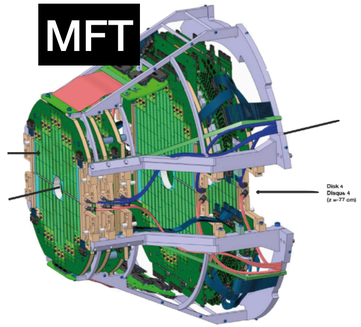
rate capability: 1 kHz

7 layers:
- all MAPS

Inner-most layer:
- radial distance: 23 mm
- material: $X/X_0 = 0.3\%$
- pitch: $O(30 \times 30\ \mu m^2)$

rate capability: 100 kHz (Pb-Pb)

Muon Forward Tracker

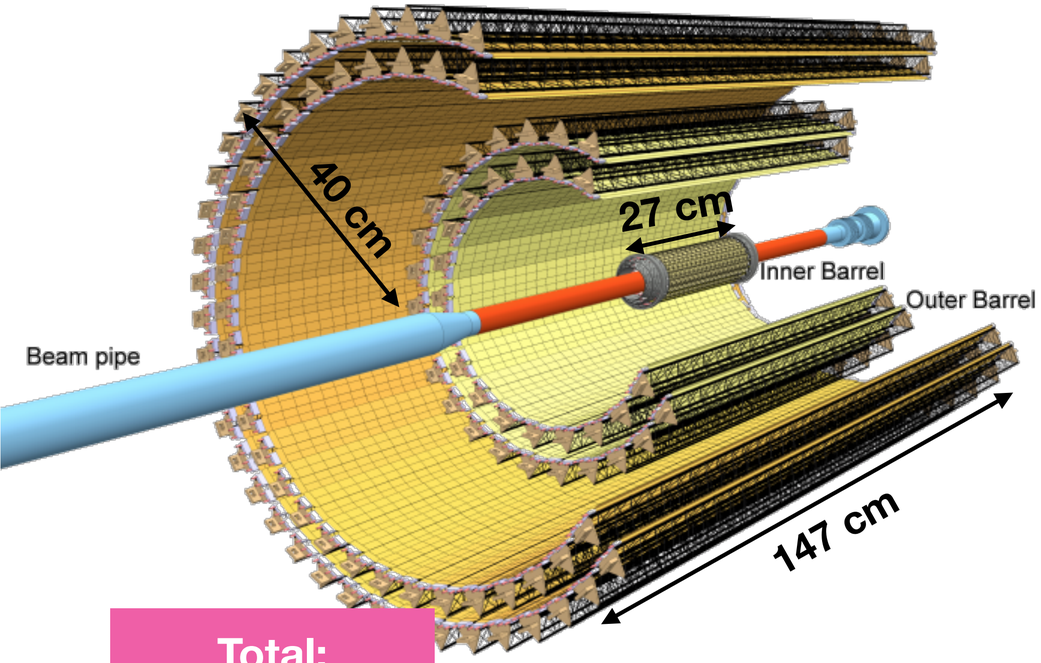


new detector

5 discs, double sided:
- based on same technology as ITS2

ITS2 overview

Layout



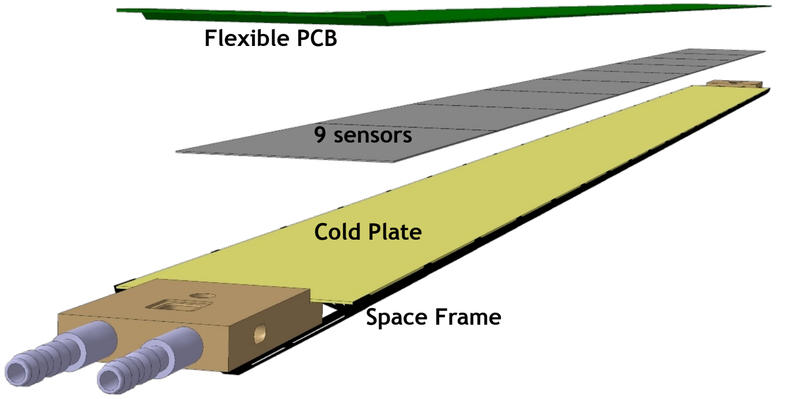
Total:
- 24k chips
- 10 m²
- 12.5 GPixel

Inner Barrel (IB)

3 Inner Layers: 12+16+20 Staves
1 Module / Stave

9 sensors per Module

96 Modules to be produced

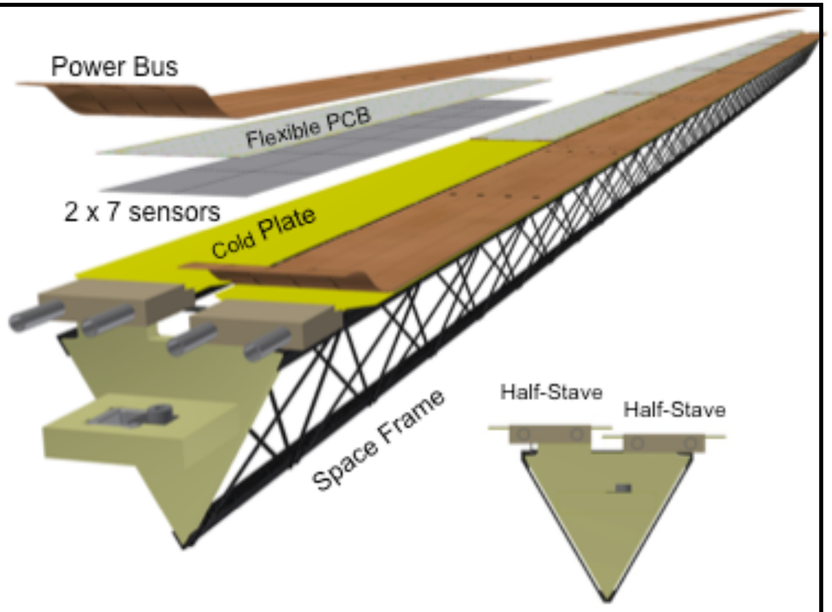


Outer Barrel (OB)

2 Middle Layers: 30+24 Staves
2×4 Modules / Stave
2 Outer Layers: 42+48 Staves
2×7 Modules / Stave

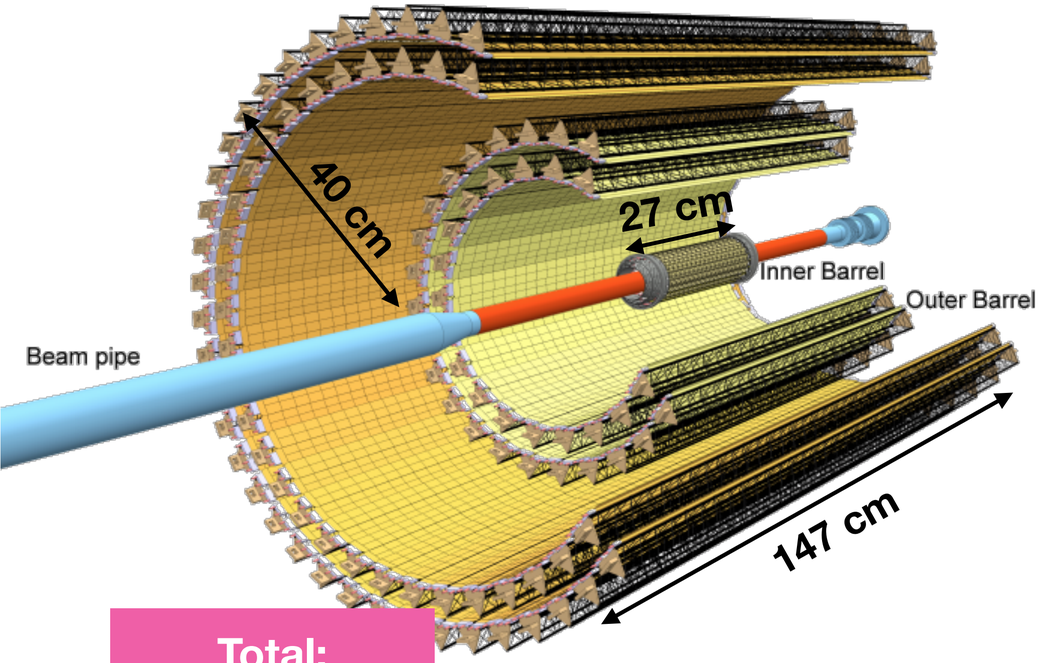
2×7 sensors / Module
(Middle and Outer Layers are equipped with the same Module Type)

1880 Modules to be produced (including spares)



ITS2 overview

Layout



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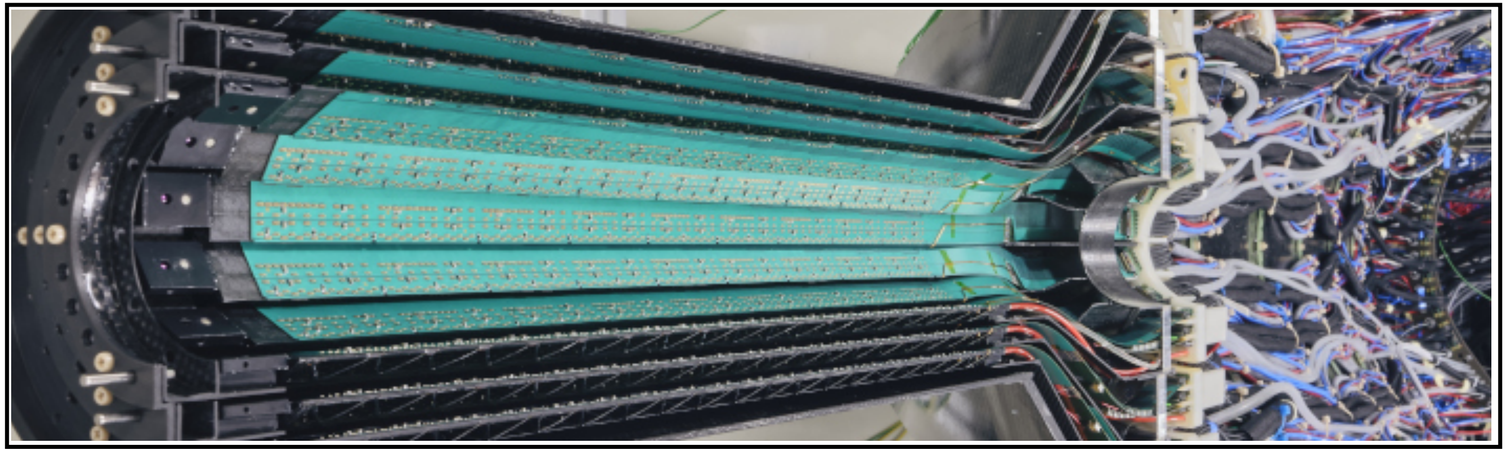
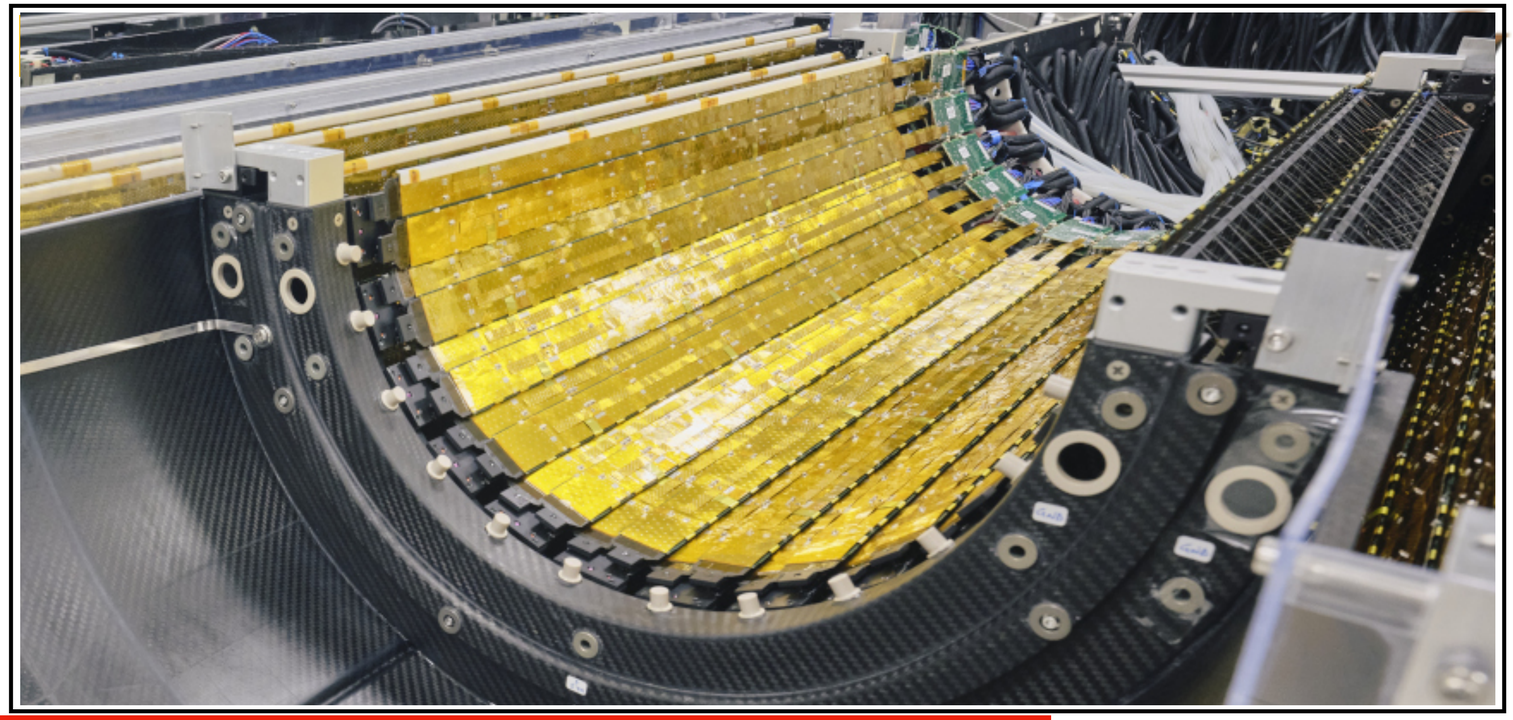
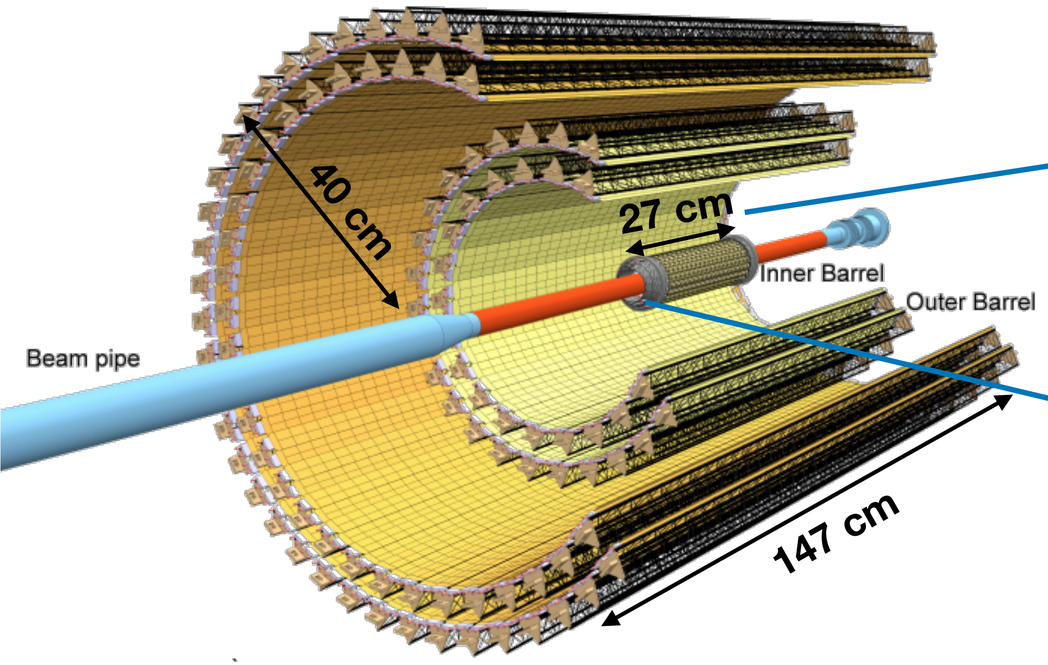




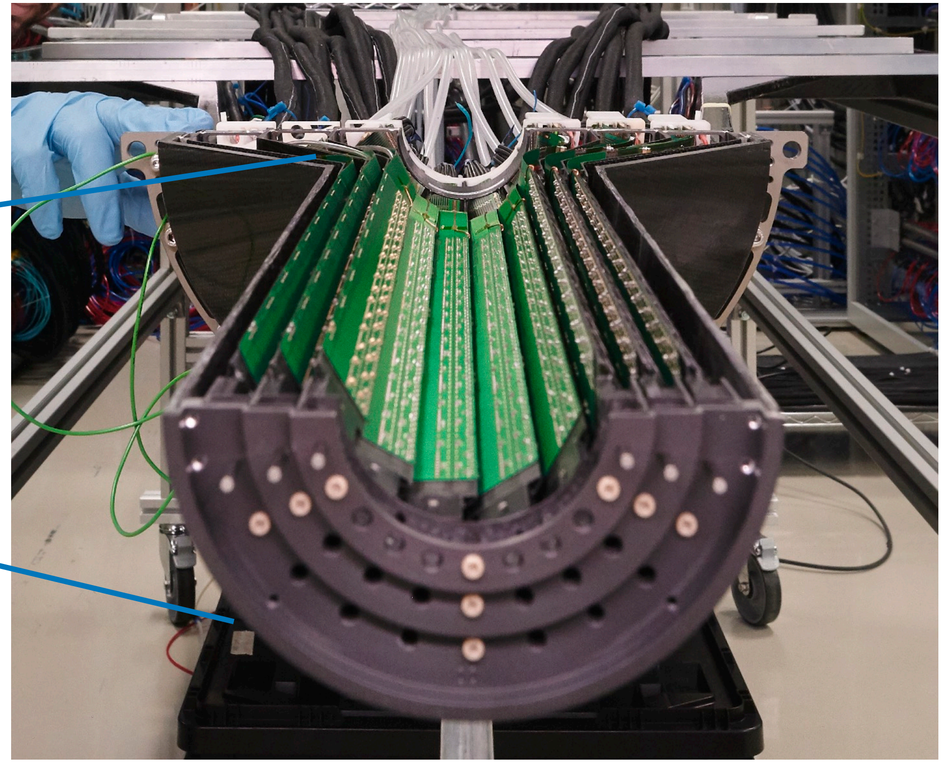
Good news: it was all built, assembled and tested!

ITS2 inner barrel

Layout

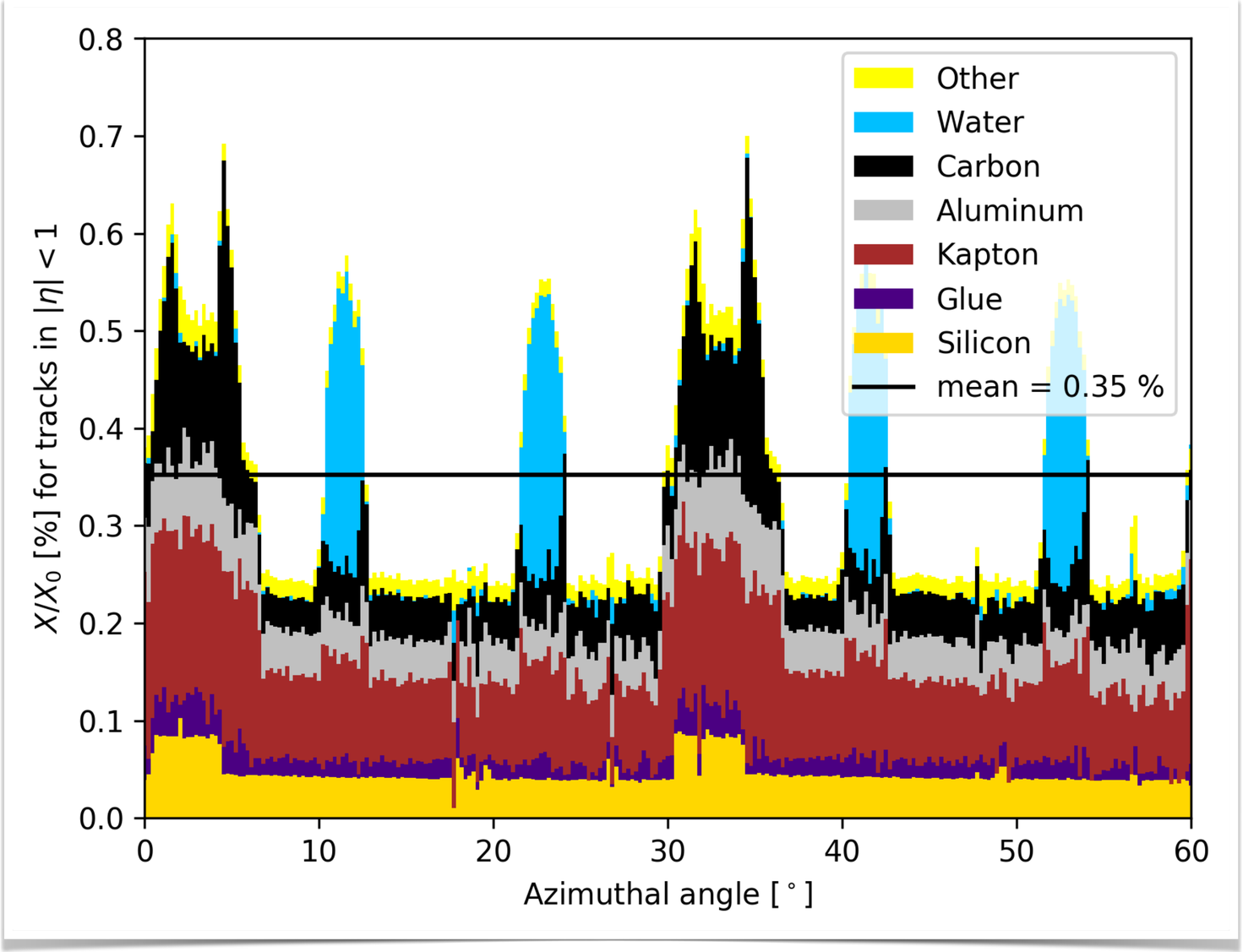


ITS2: assembled three inner-most half-layers



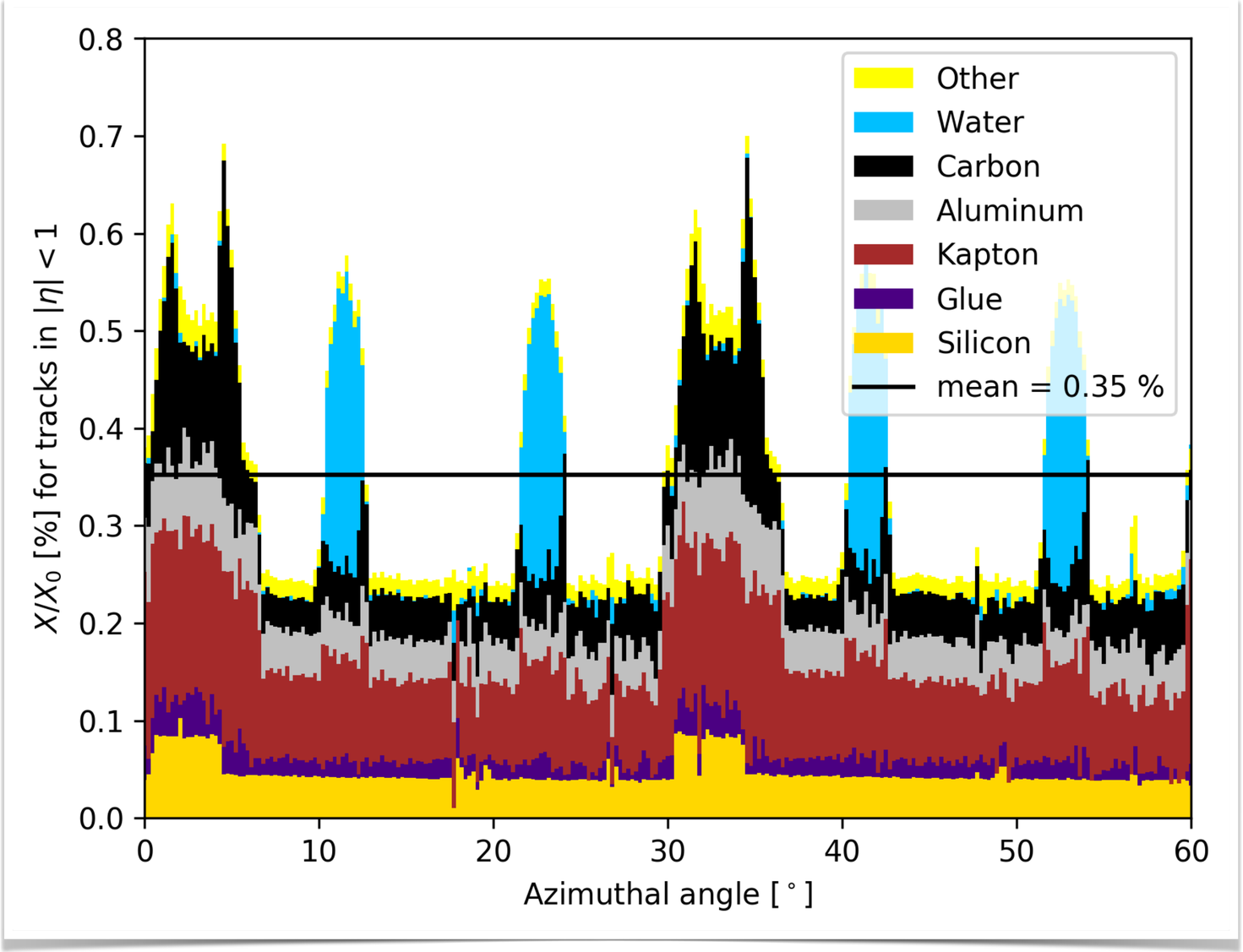
- ITS2 will already have unprecedented performance
- The Inner Barrel is ultra-light but rather packed → further improvements seem possible
- **Key questions: Can we get closer to the IP? Can we reduce the material further?**

Motivation for ITS3



- Observations:
  - Si makes only **1/7th** of total material
  - **irregularities** due to support/ cooling

Motivation for ITS3



- Observations:
  - Si makes only **1/7th** of total material
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- Removal of water cooling
  - **possible** if power consumption stays below 20 mW/cm^2

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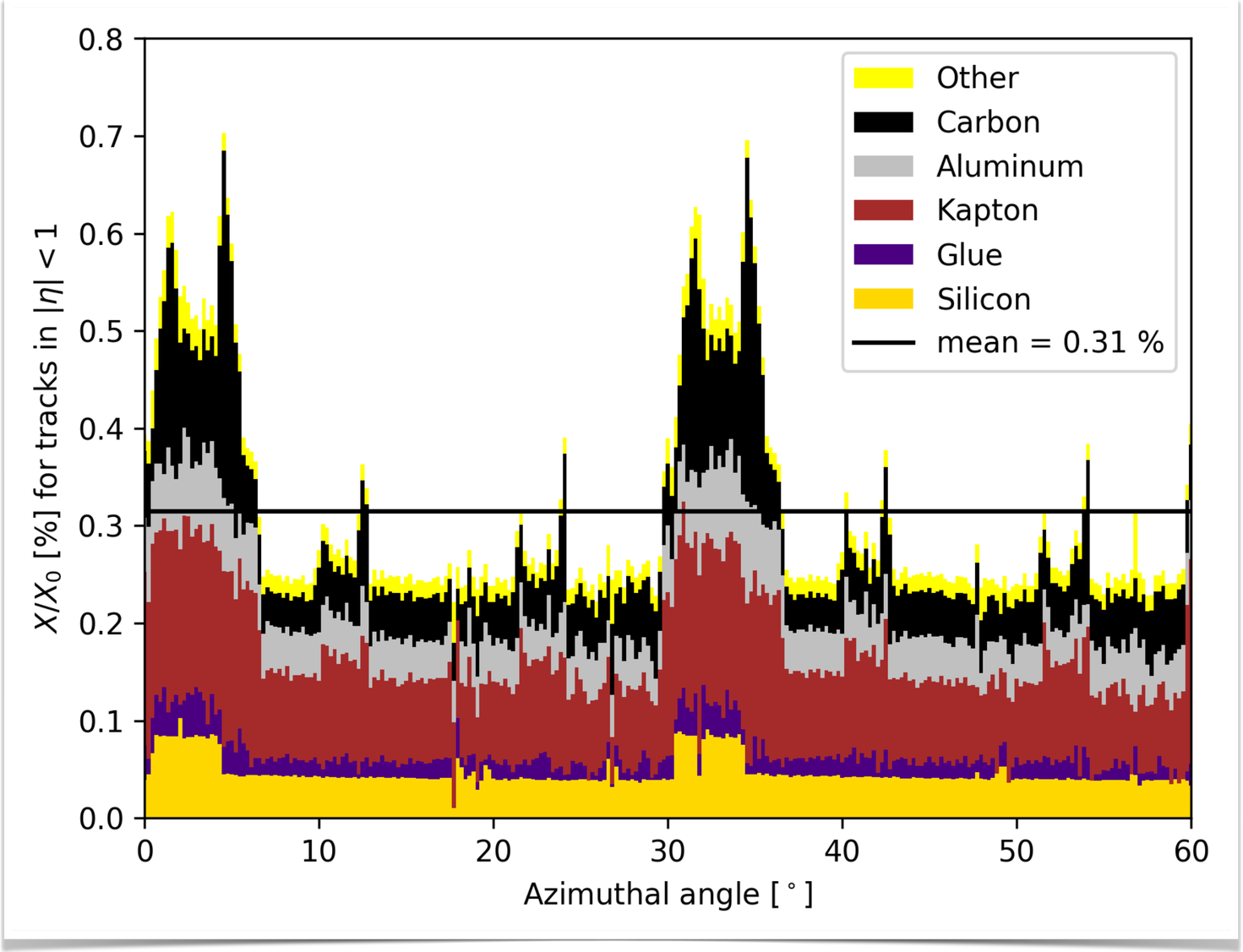

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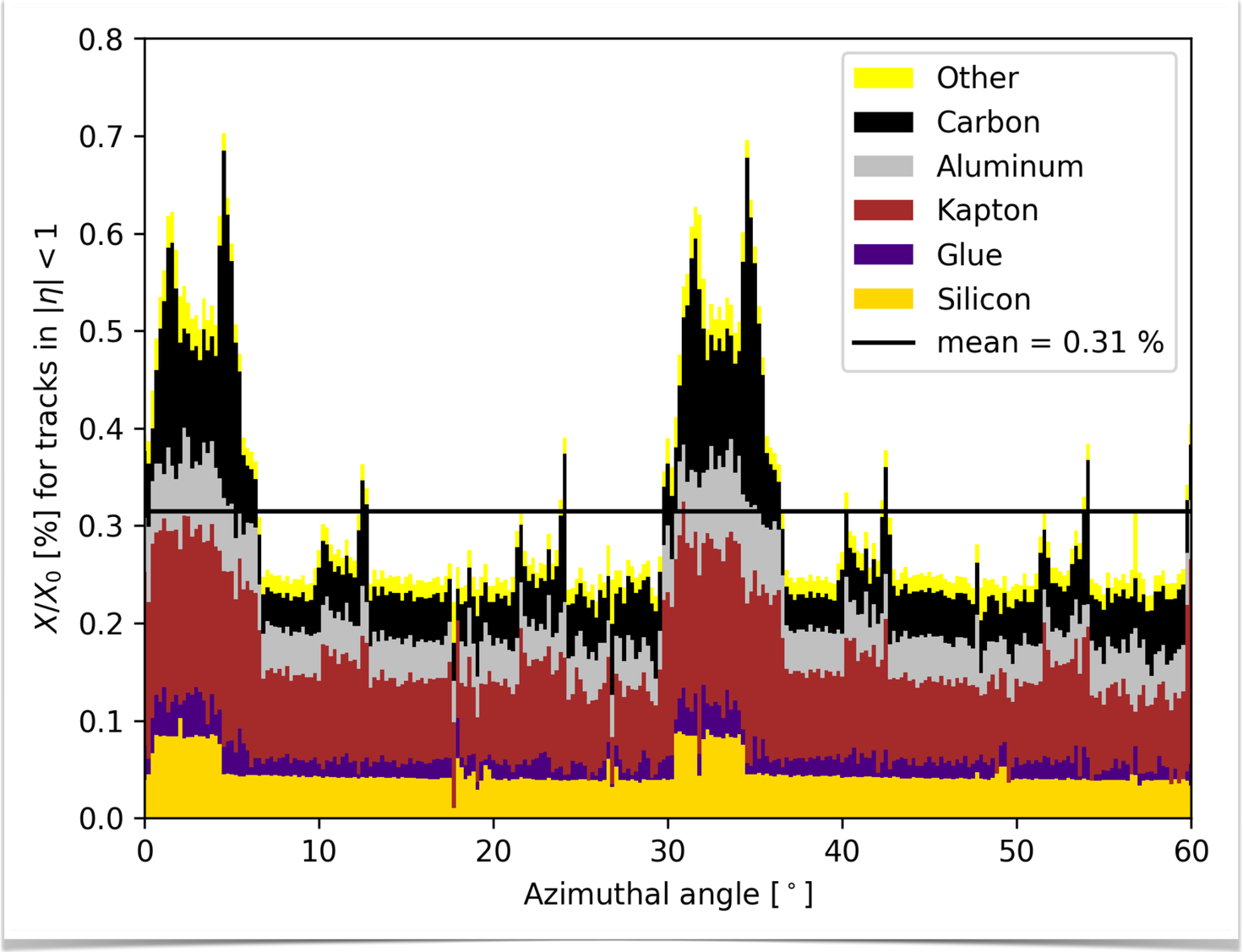

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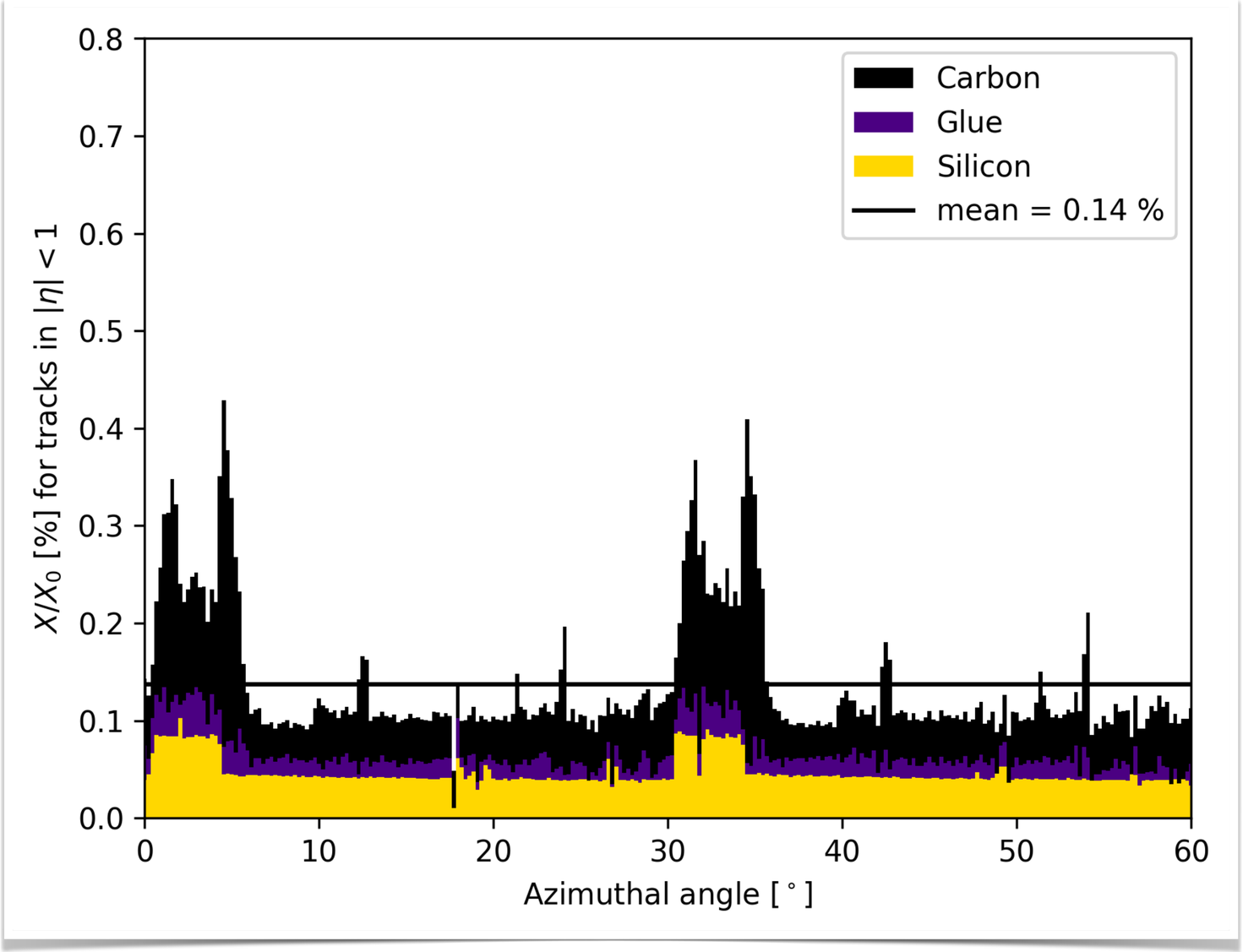

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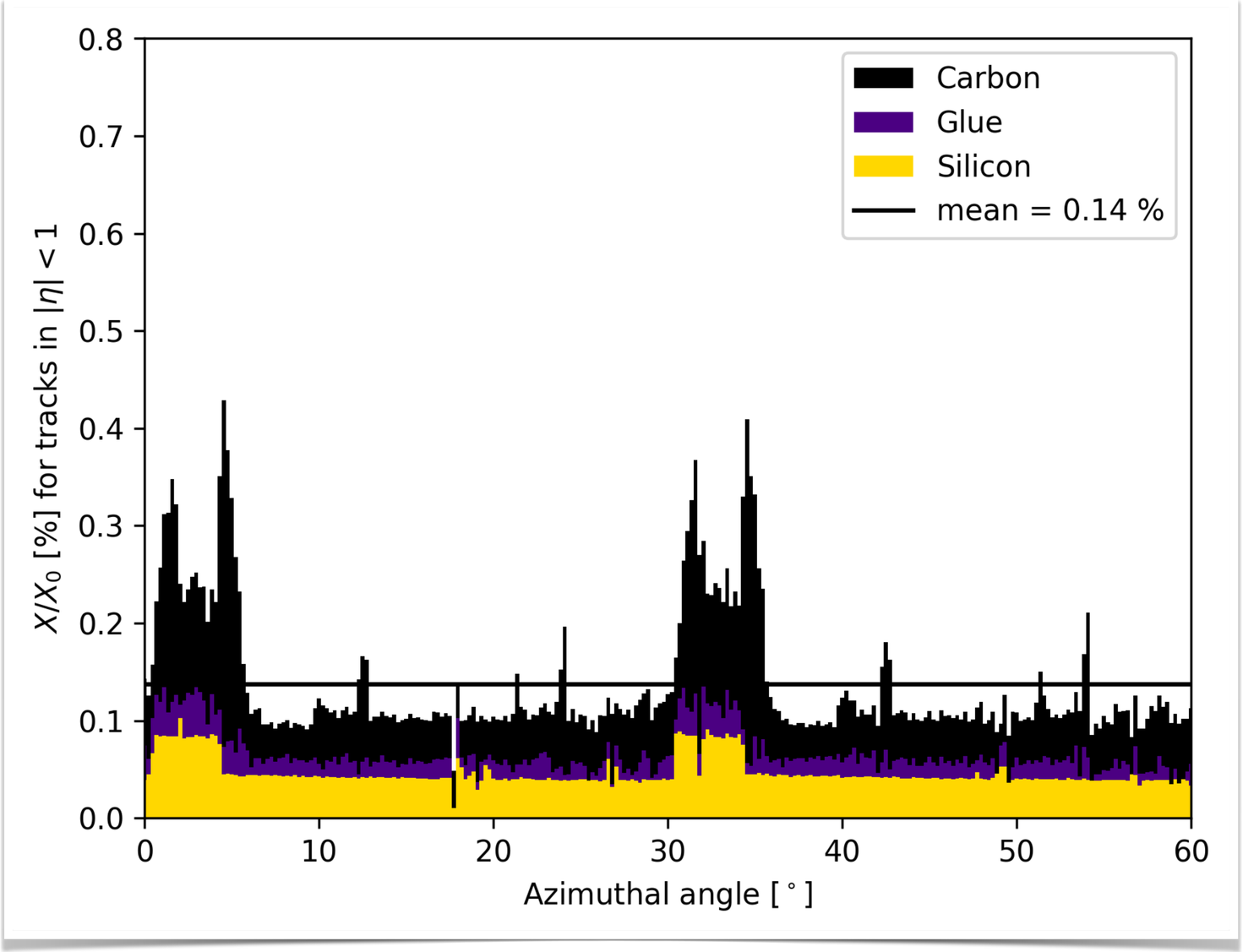

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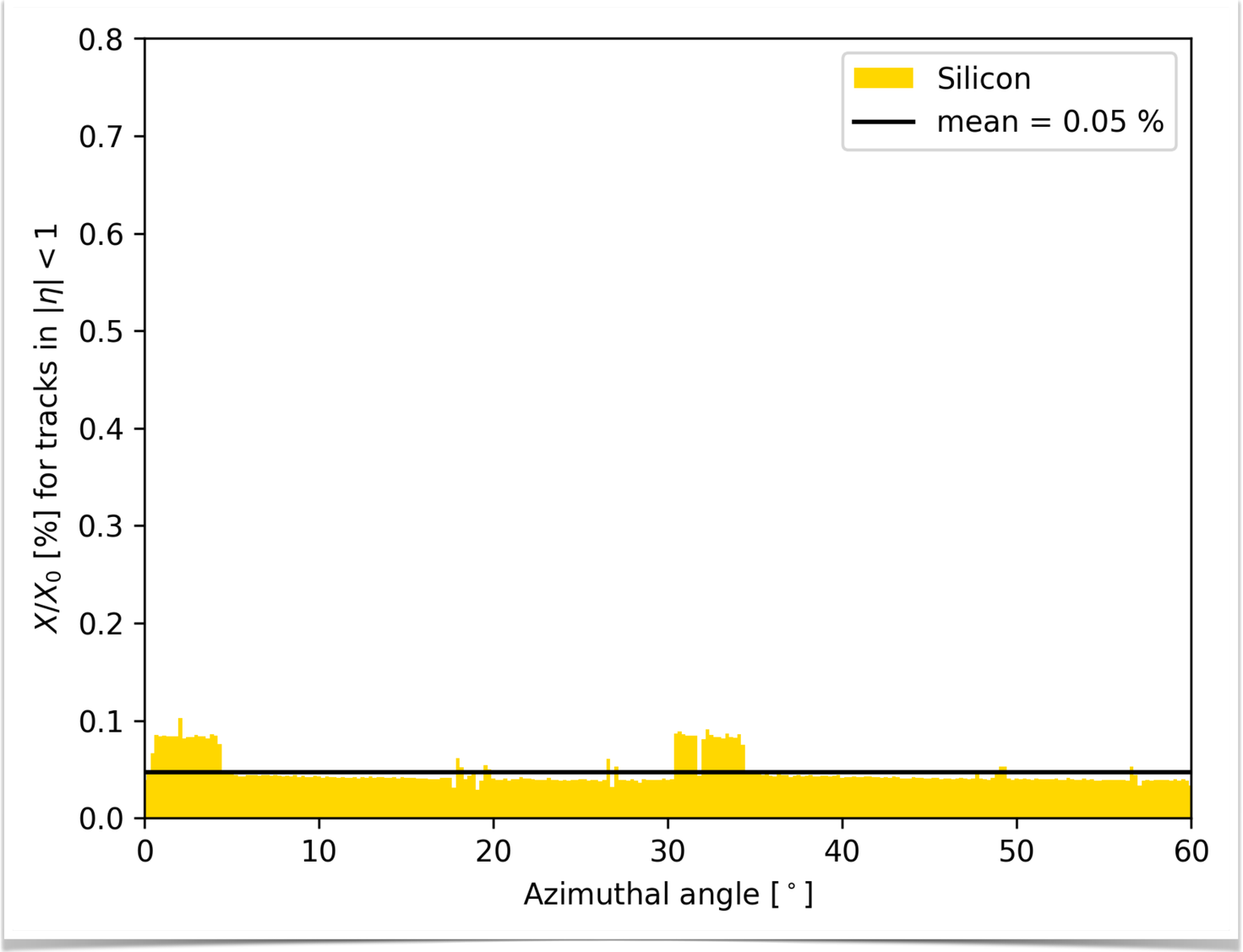
  - **possible** if integrated on chip
- Removal of mechanical support
  - **benefit** from increased stiffness by rolling Si wafers

Motivation for ITS3



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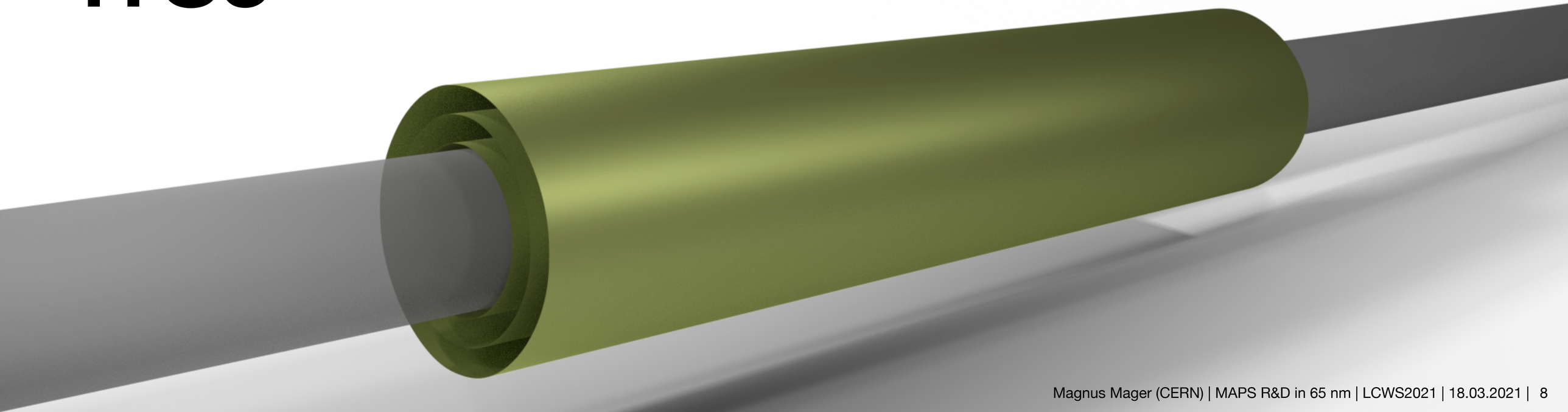
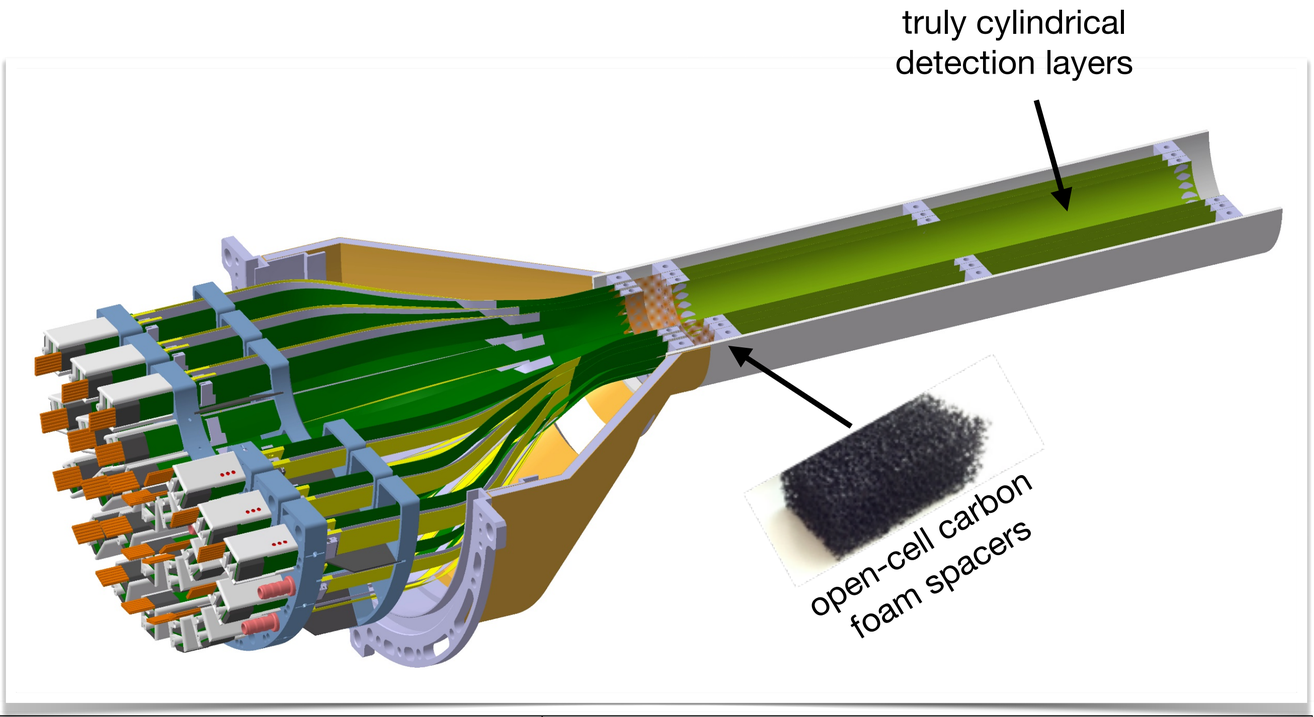
ITS3



ITS3 detector concept



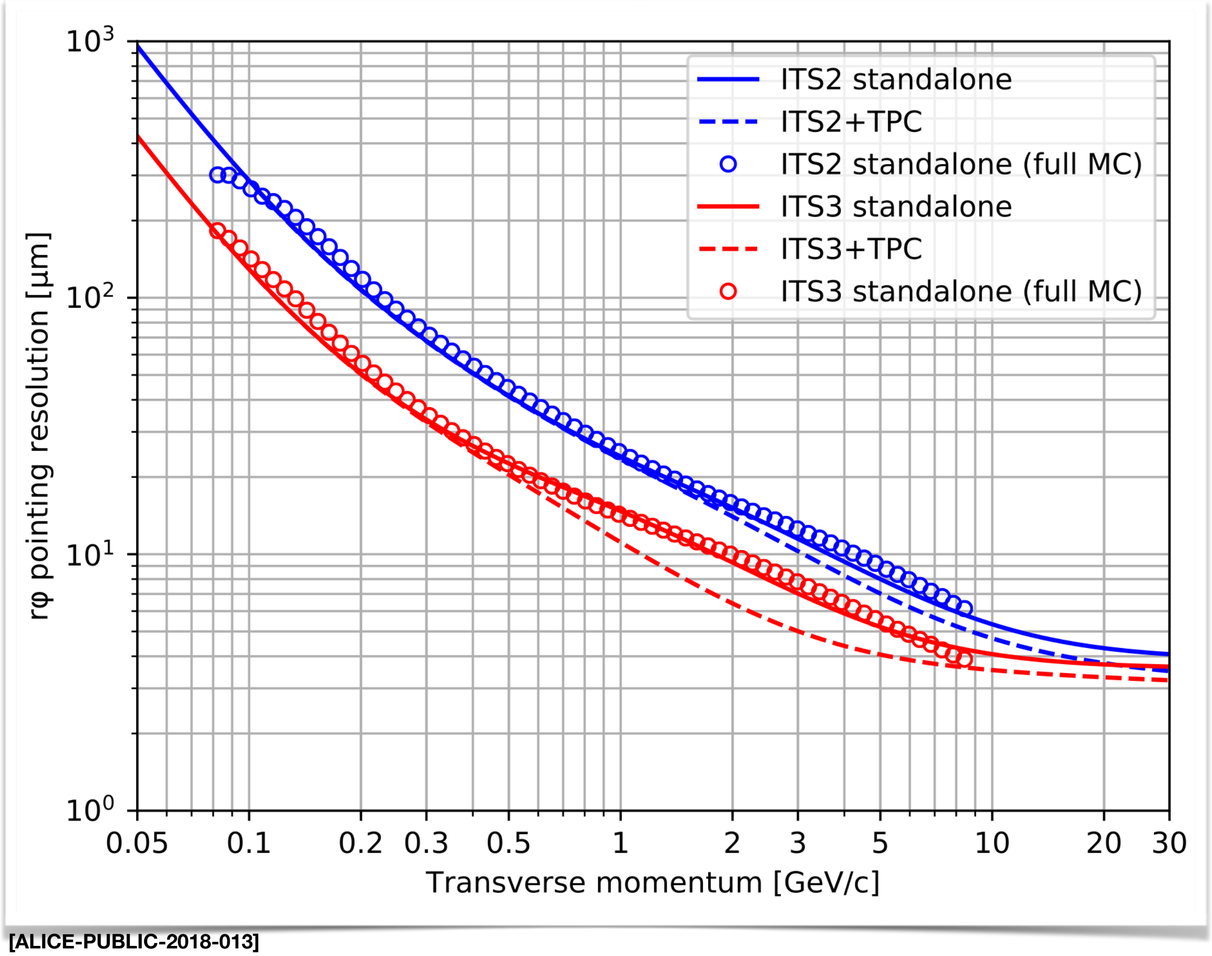
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

- Key ingredients:
  - 300 mm wafer-scale chips, fabricated using stitching
  - thinned down to 20-40 µm (0.02-0.04% X0), making them flexible
  - bent to the target radii
  - mechanically held in place by carbon foam ribs
- Key benefits:
  - extremely low material budget: 0.02-0.04% X0 (beampipe: 500 µm Be: 0.14% X0)
  - homogeneous material distribution: negligible systematic error from material distribution

The whole detector will comprise six (!) chips – and barely anything else

ITS3 performance figures

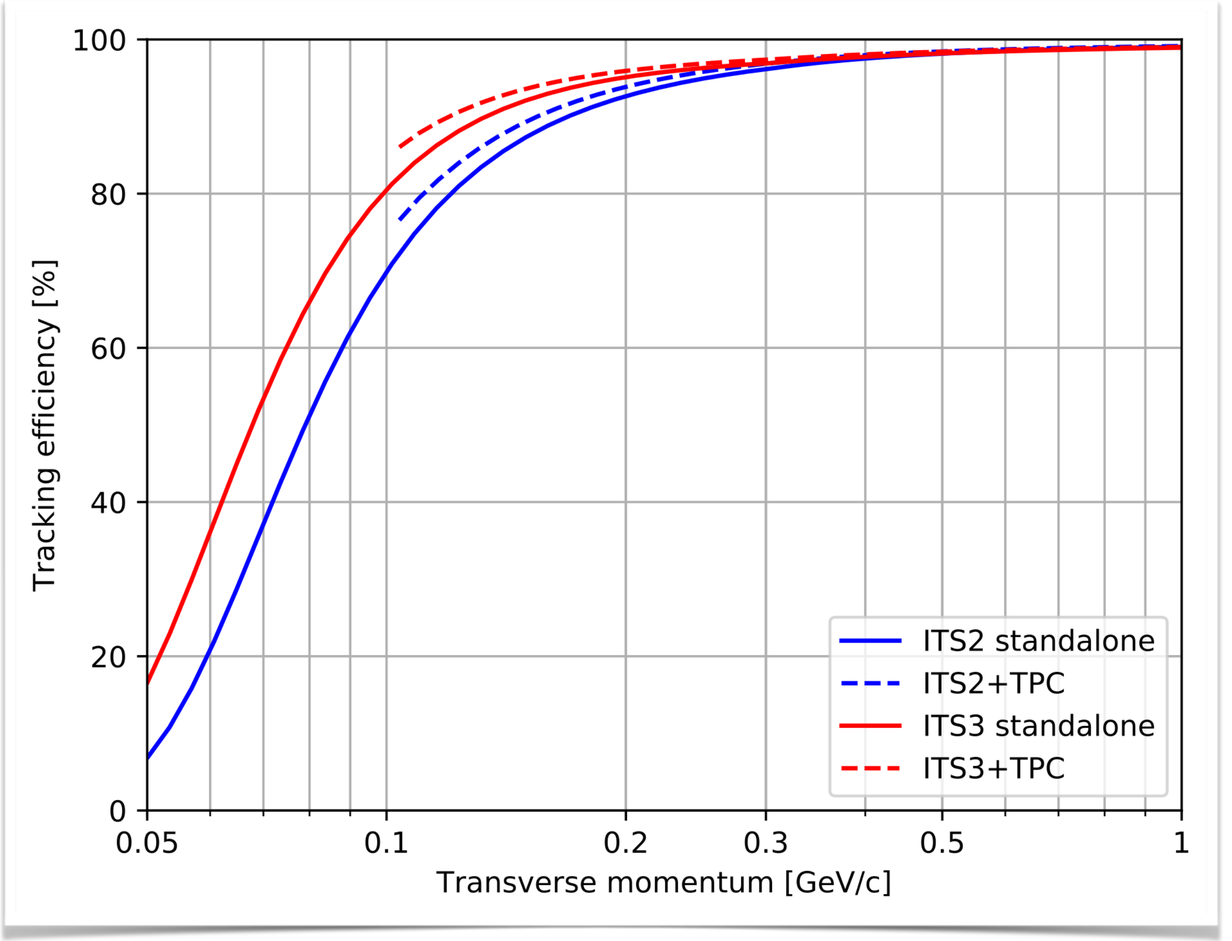
pointing resolution



[ALICE-PUBLIC-2018-013]

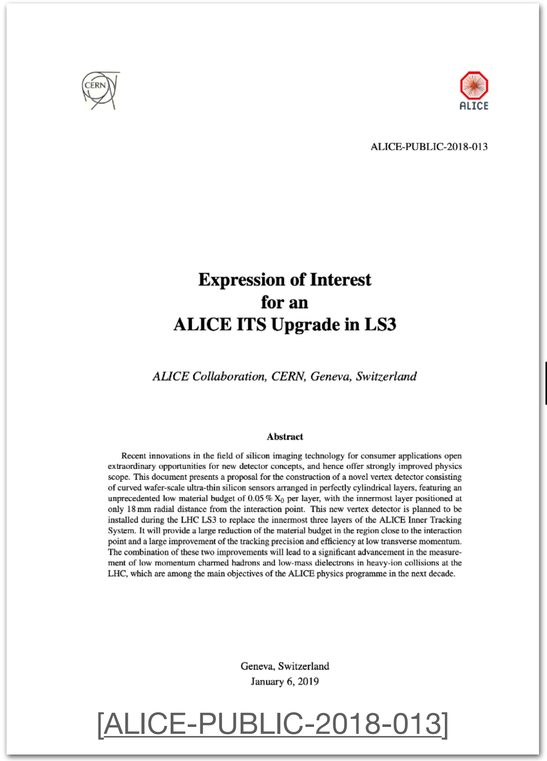
improvement of factor 2 over all momenta

tracking efficiency



large improvement for low transverse momenta

ITS3 project startup
EoI, LoI, start of R&D



ALICE-PUBLIC-2018-013

Expression of Interest for an ALICE ITS Upgrade in LS3

ALICE Collaboration, CERN, Geneva, Switzerland

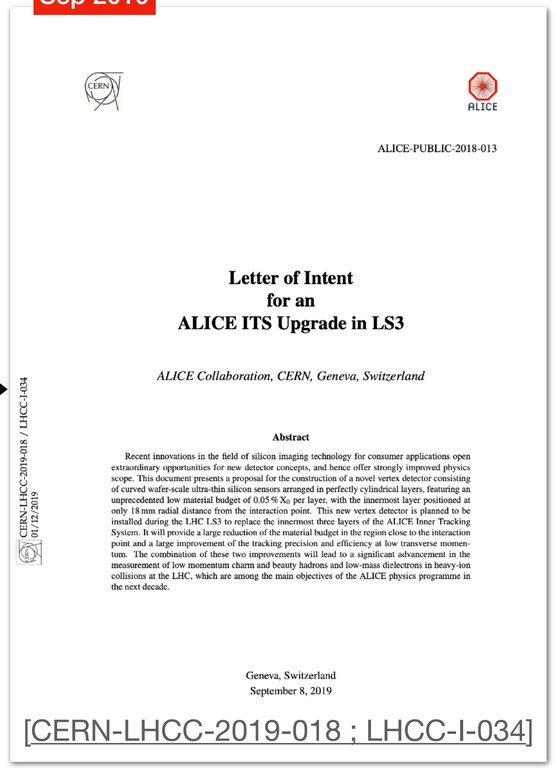
Abstract

Recent innovations in the field of silicon imaging technology for consumer applications open extraordinary opportunities for new detector concepts, and hence offer strongly improved physics scope. This document presents a proposal for the construction of a novel vertex detector consisting of curved wafer-scale ultra-thin silicon sensors arranged in perfectly cylindrical layers, featuring an unprecedented low material budget of 0.05 % X_0 per layer, with the innermost layer positioned at only 18 mm radial distance from the interaction point. This new vertex detector is planned to be installed during the LHC LS3 to replace the innermost three layers of the ALICE Inner Tracking System. It will provide a large reduction of the material budget in the region close to the interaction point and a large improvement of the tracking precision and efficiency at low transverse momentum. The combination of these two improvements will lead to a significant advancement in the measurement of low momentum charmed hadrons and low-mass dielectrons in heavy-ion collisions at the LHC, which are among the main objectives of the ALICE physics programme in the next decade.

Geneva, Switzerland
January 6, 2019

[ALICE-PUBLIC-2018-013]

Sep 2019



CERN-LHCC-2019-018 / LHCC-I-034
01/12/2019

ALICE-PUBLIC-2018-013

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Geneva, Switzerland
September 8, 2019

[CERN-LHCC-2019-018 ; LHCC-I-034]

Dec 4th 2019

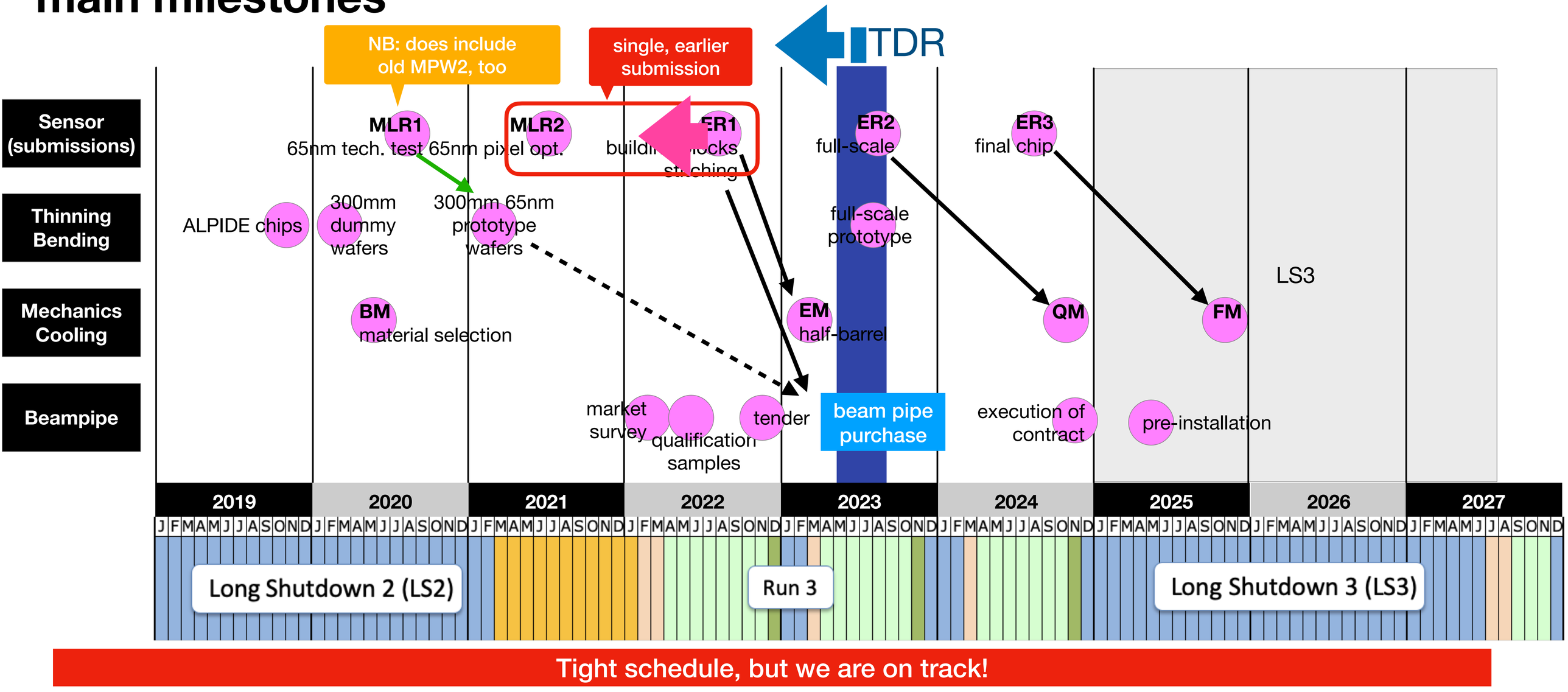
[ITS3 R&D kickoff meeting]

R&D!

[…]
The **LHCC is impressed** by the new concept for the ITS3
[…]
The **LHCC endorses** the plan of ALICE to carry out the necessary R&D
[…]
[LHCC minutes: CERN-LHCC-2019-010 ; LHCC-139]

[…]
The **LHCC congratulates** the ITS3 groups for the successful start of the project.
[…]
[LHCC minutes: CERN-LHCC-2020-008 ; LHCC-142]

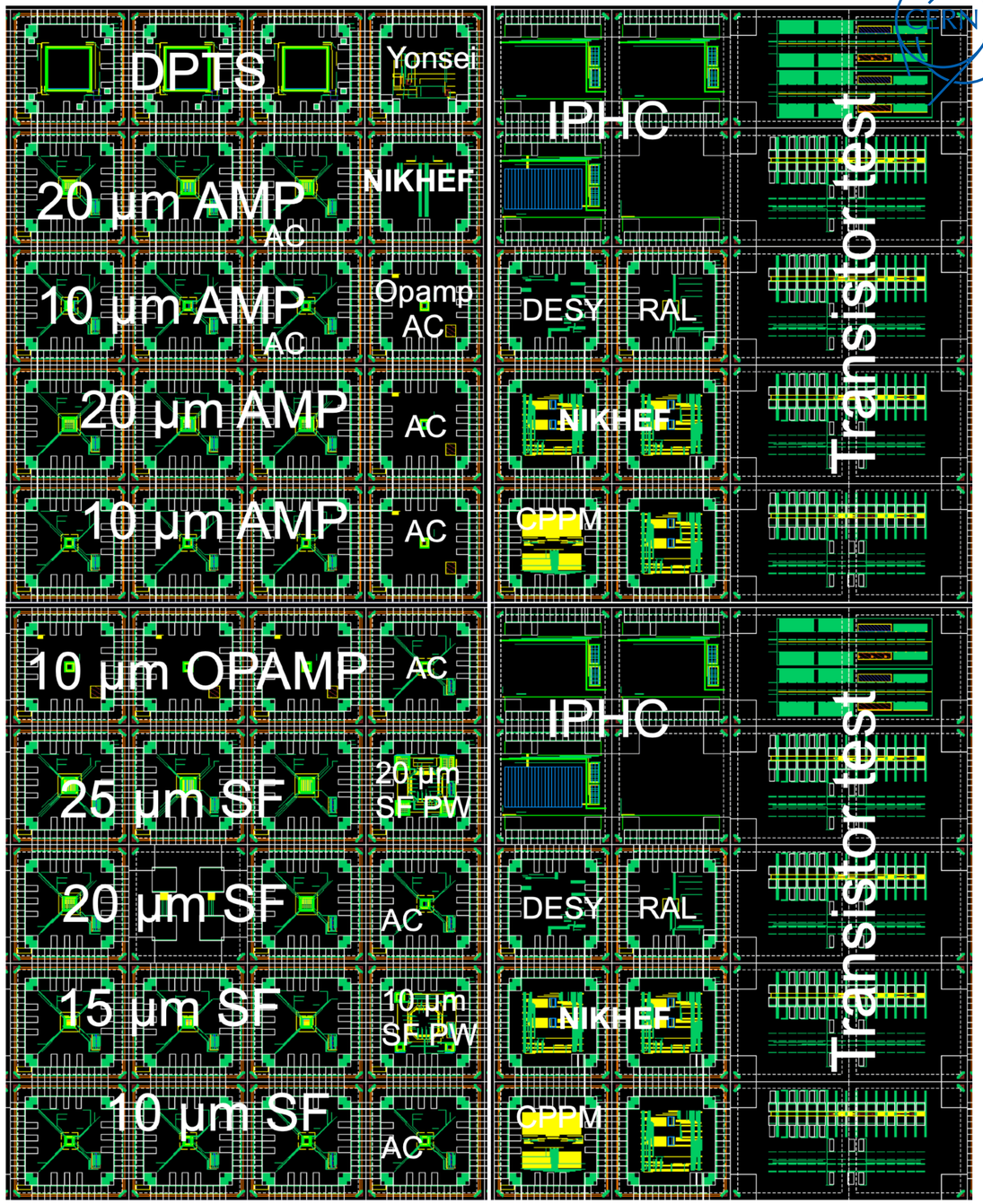
ITS3 timeline
main milestones



Tight schedule, but we are on track!

MLR: multiple layer per reticle, **ER:** engineering run,
BM: breadboard module, **EM:** engineering module, **QM:** qualification module, **FM:** final module

65 nm


DPTS
Yonsei
20 µm AMP
AC
NIKHEF
10 µm AMP
AC
Opamp
AC
20 µm AMP
AC
10 µm AMP
AC
IPHC
DESY
RAL
NIKHEF
CPPM
Transistor test
10 µm OPAMP
AC
25 µm SF
20 µm
SF PW
20 µm SF
AC
15 µm SF
10 µm
SF PW
10 µm SF
AC
IPHC
DESY
RAL
NIKHEF
CPPM
Transistor test

Sensor challenges
and mapping to 65 nm

- **Low power consumption** (< 20 mW/cm²) inside pixel matrix to allow for air-cooling
- **Stitching** to obtain wafer-scale sensors
  - 300 mm wafer process to reach z-coverage
- **Thinning to < 50 µm** to become bendable
- … while keeping other parameters (high spatial resolution, moderate radiation hardness, …) as for ITS2 (ALPIDE)

TowerJazz 65 nm

✅ generally lower consumption when scaling to deeper sub-micron

✅ produced on 300 mm wafers

✅ stitching is available

⚠️ design needs to be optimised for yield

⚠️ radiation hardness to be checked

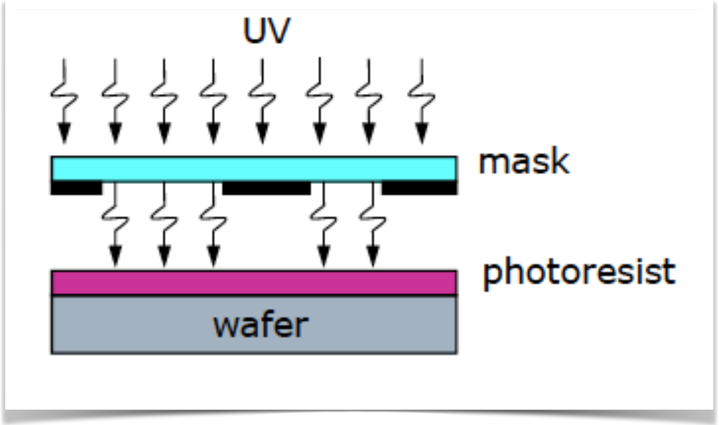
⚠️ charge-collection to be checked/ optimised

Switching from 180 nm (ALPIDE) to 65 nm seems like a perfect fit!

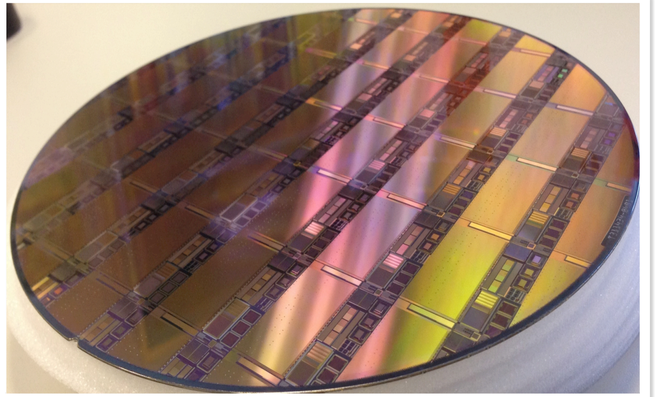
Wafer-scale chip

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm^2
  - modules are tiled with chips connected to a flexible printed circuit board

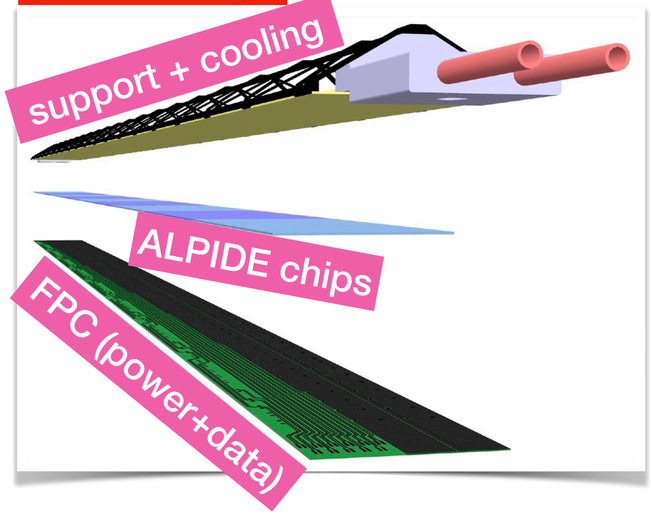
Principle of photolithography



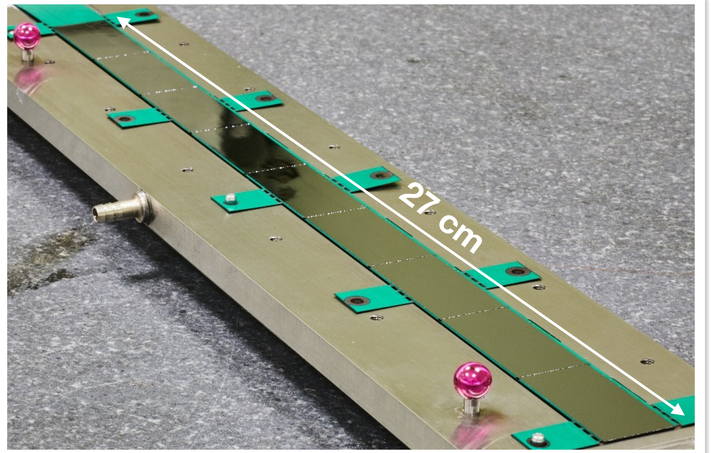
200 mm ALPIDE prototype wafer



Stave design



FPC + chips



Wafer-scale chip

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
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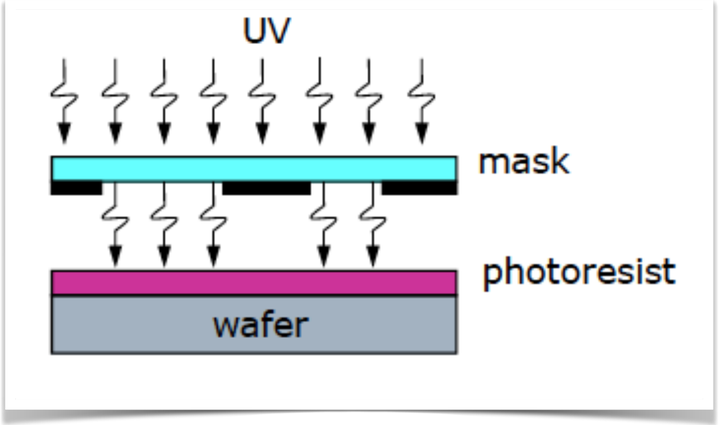
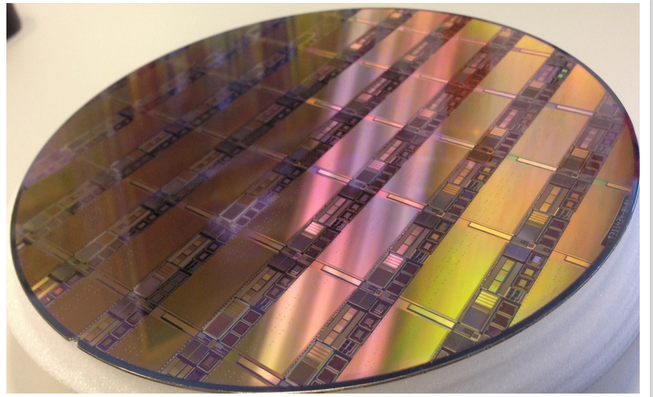
  - modules are tiled with chips connected to a flexible printed circuit board
- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - actively used in industry
  - a 300 mm wafer can house a chip to equip a full half-layer
  - *requires dedicated chip design*

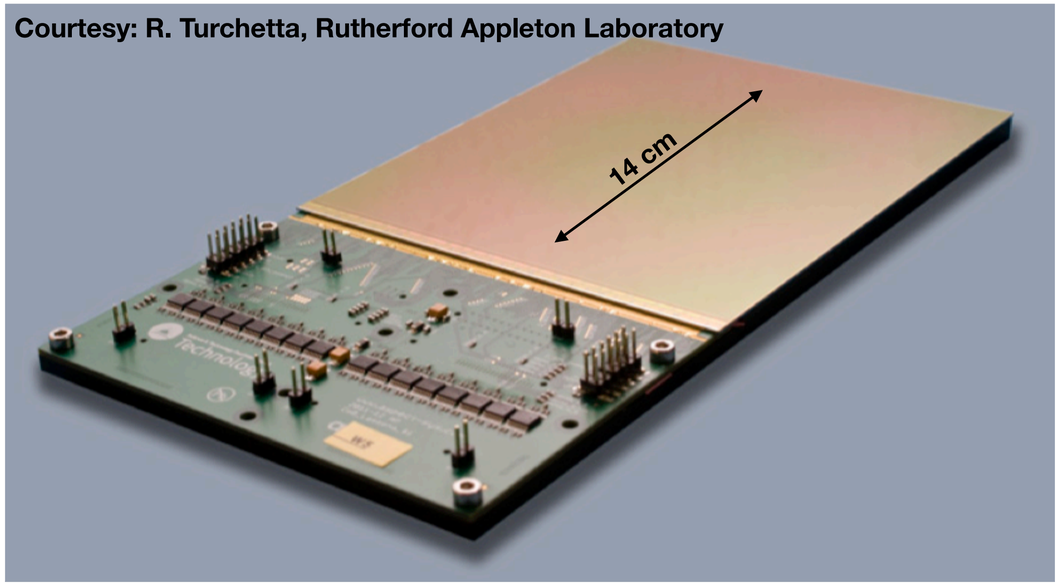
Principle of photolithography



200 mm ALPIDE prototype wafer

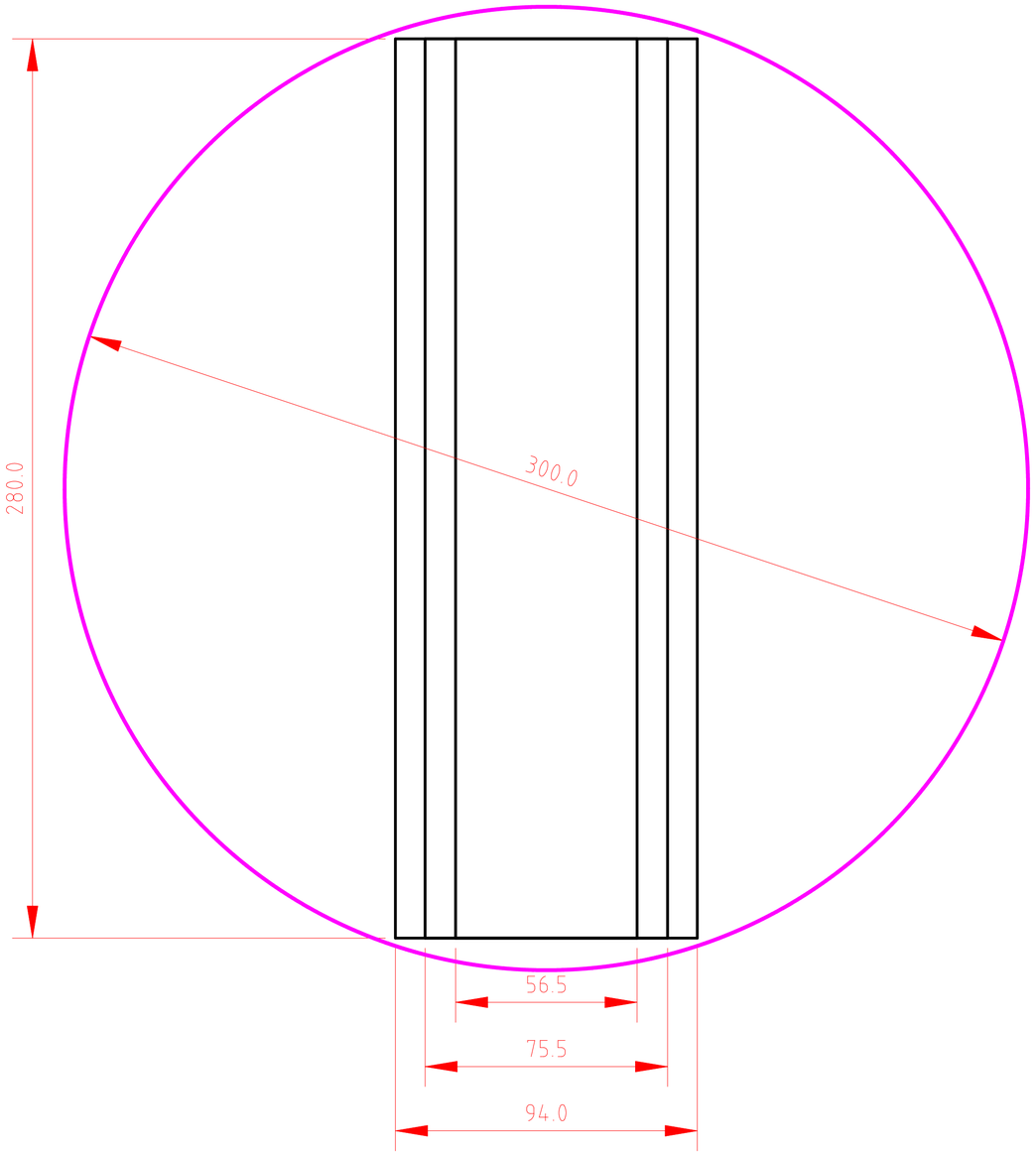


Wafer-scale sensor



Sensor dimensions
65 nm process

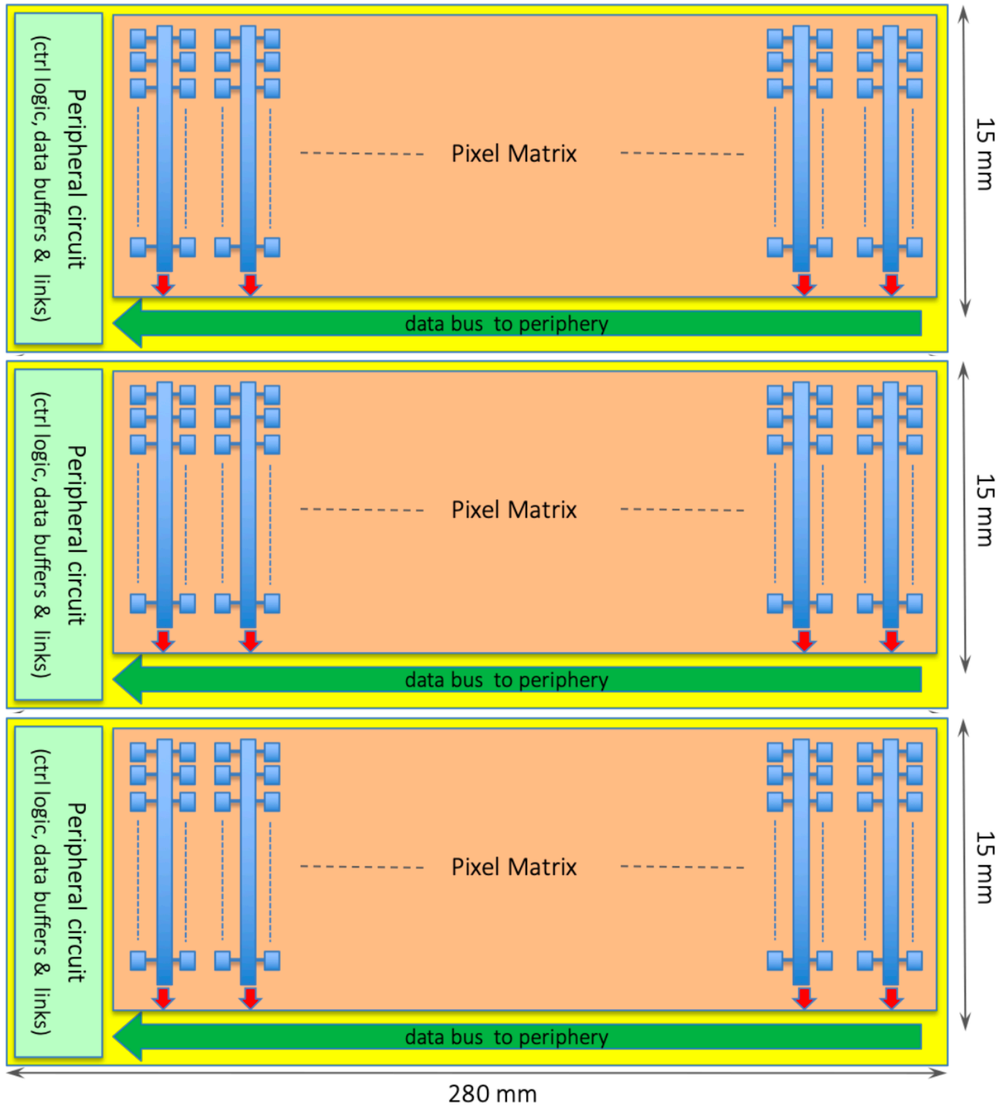
- All the three foreseen (half-) layers can be equipped with a single chip of a 300 mm wafer
- This is the driving argument for ITS3 to go to the 65 nm process
- At the same time, ITS3 wants to exploit the technology at its best, potentially:
  - lower power
  - more logic
  - smaller pixels
  - faster readout



Architecture
Ideas + Challenges

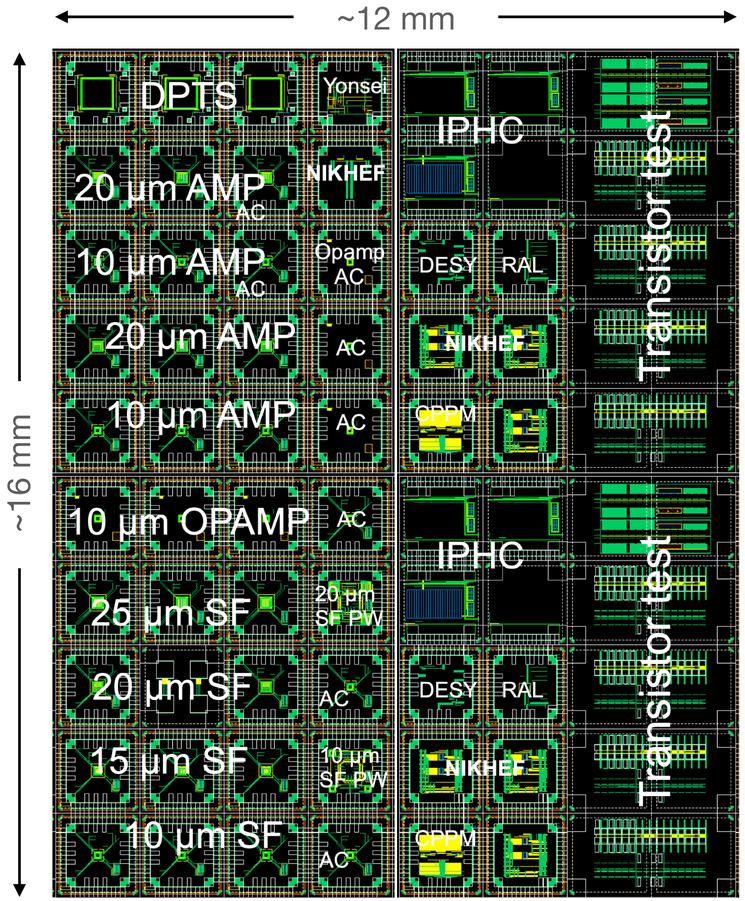
- Stitching requires a regular, periodic structure of the matrix
- Different architectures are under study
  - here, the concept laid out in the LoI is mostly inspired by ALPIDE
- ITS3 needs three different chip sizes
  - naturally comes with stitching a variable number of “rows”
  - likely adaptable to other geometries (e.g. square-like matrices)
- Electrical interface only on one side
- Power consumption needs to stay low in the matrix region, but can be larger at periphery
  - dictated by air cooling capabilities and acceptable voltage drop along the sensor

Possible architecture – many more being explored right now!



Sensor prototyping
First 65nm submission “MLR1”

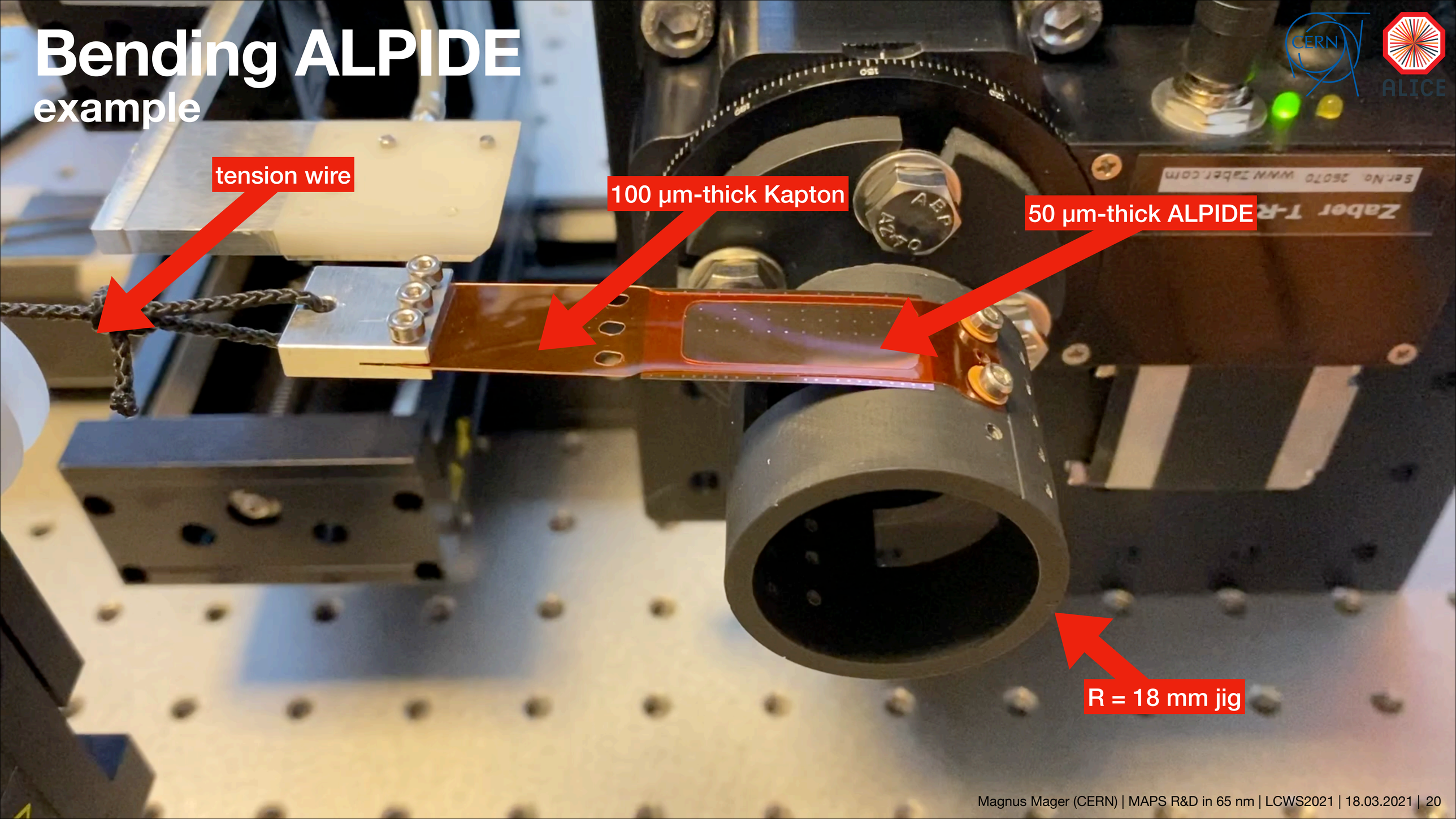
- ITS3 plays a leading role in the evaluation of the TowerJazz 65 nm technology for MAPS
- First test structures in 65 nm have been just submitted
  - transistor test structures for radiation hardness studies
  - various diode matrices for charge-collection studies
  - analog building blocks
- Large number of dies in different processing flavours are expected
  - will provide crucial input into the next design steps
- Wafer-scale blocks will be diced out to study mechanical properties
- First chips expected mid 2021: **stay tuned!**



expect O(500) dies per wafer

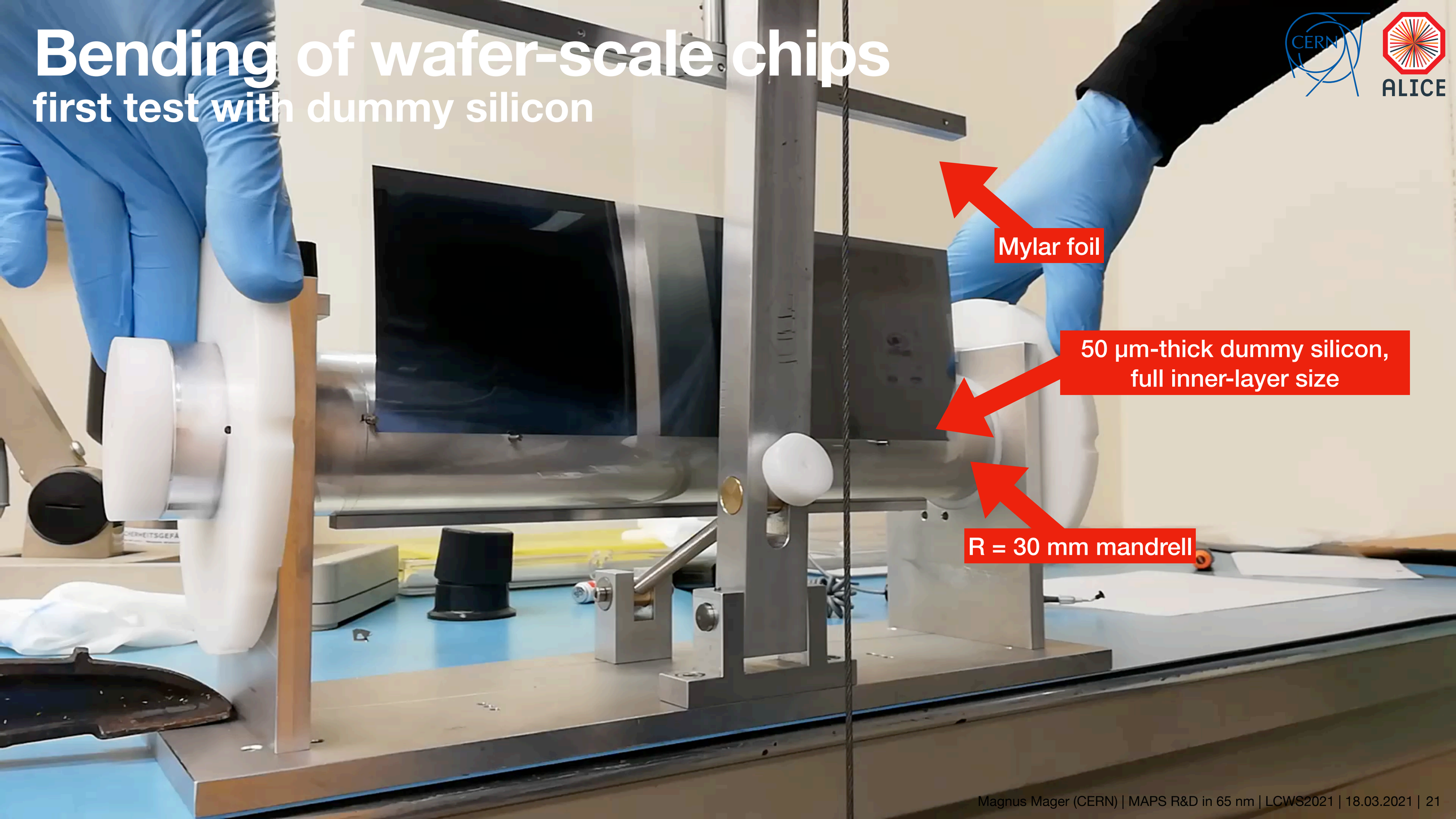
Bent MAPS

Bending ALPIDE
example



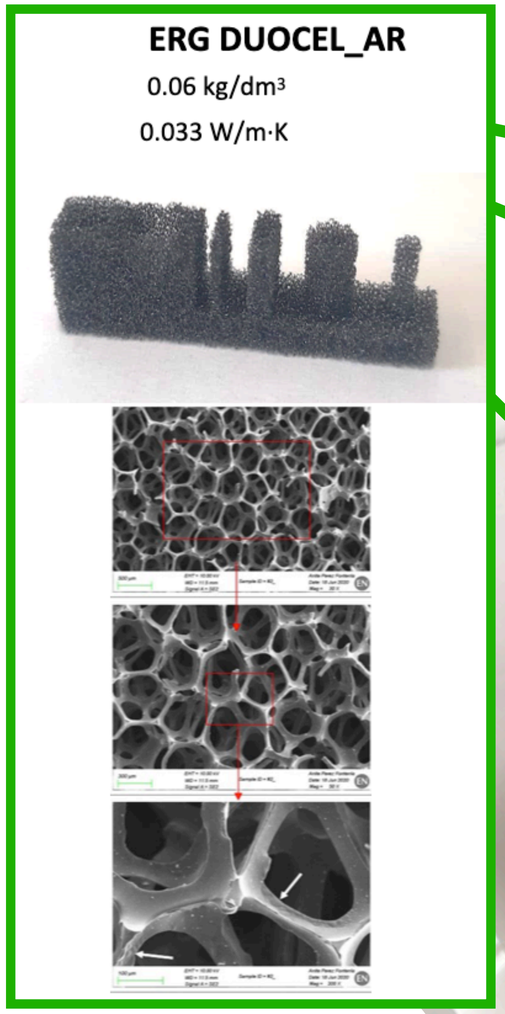
Bending of wafer-scale chips

first test with dummy silicon



Mechanics
demonstrator

- Layers can be held in shape and position with a minimal amount of material
- A very light carbon foam is already sufficient
- Detailed mechanical and thermal characterisation ongoing



50 µm dummy Si wafer-scale chip

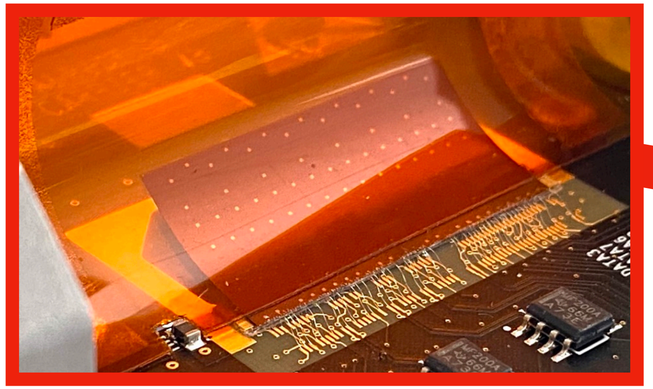
[ITS3 Layer 2 (R = 30 mm) engineering module]

Test beams
overview

- 3 beam tests at DESY in 2020
- different DUTs
- comprehensive data set

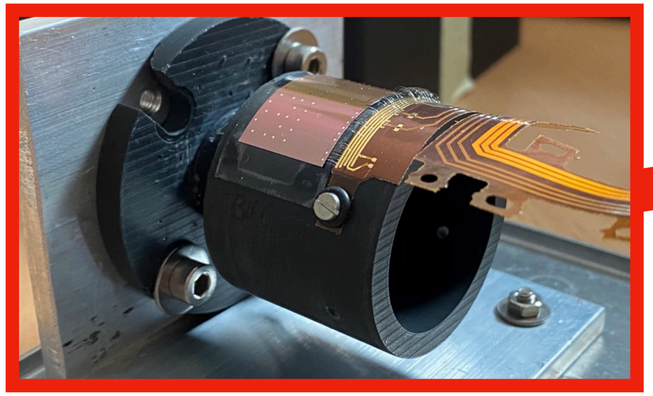
a) Jun 2020

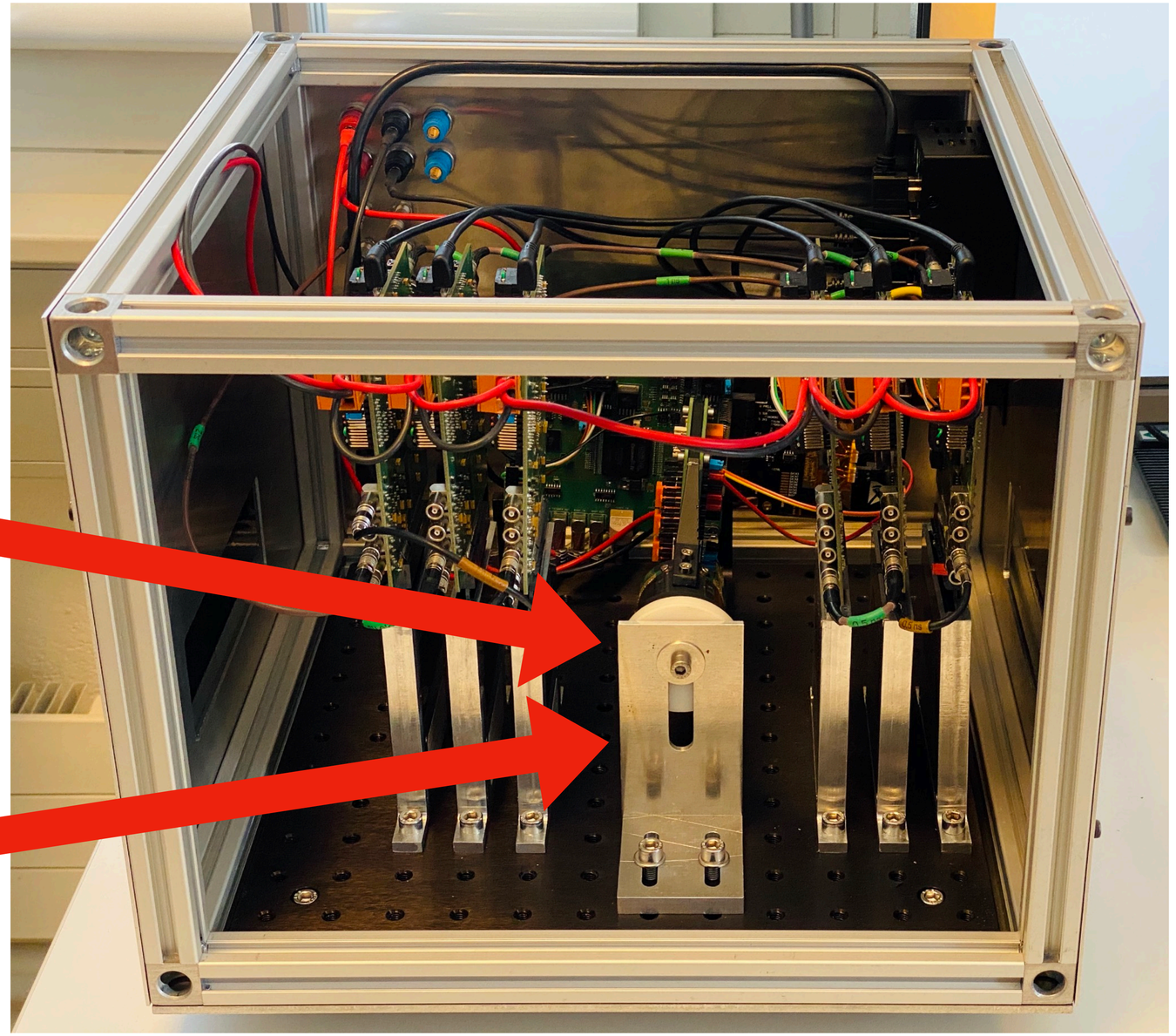
first bent ALPIDE
on “standard carrier”



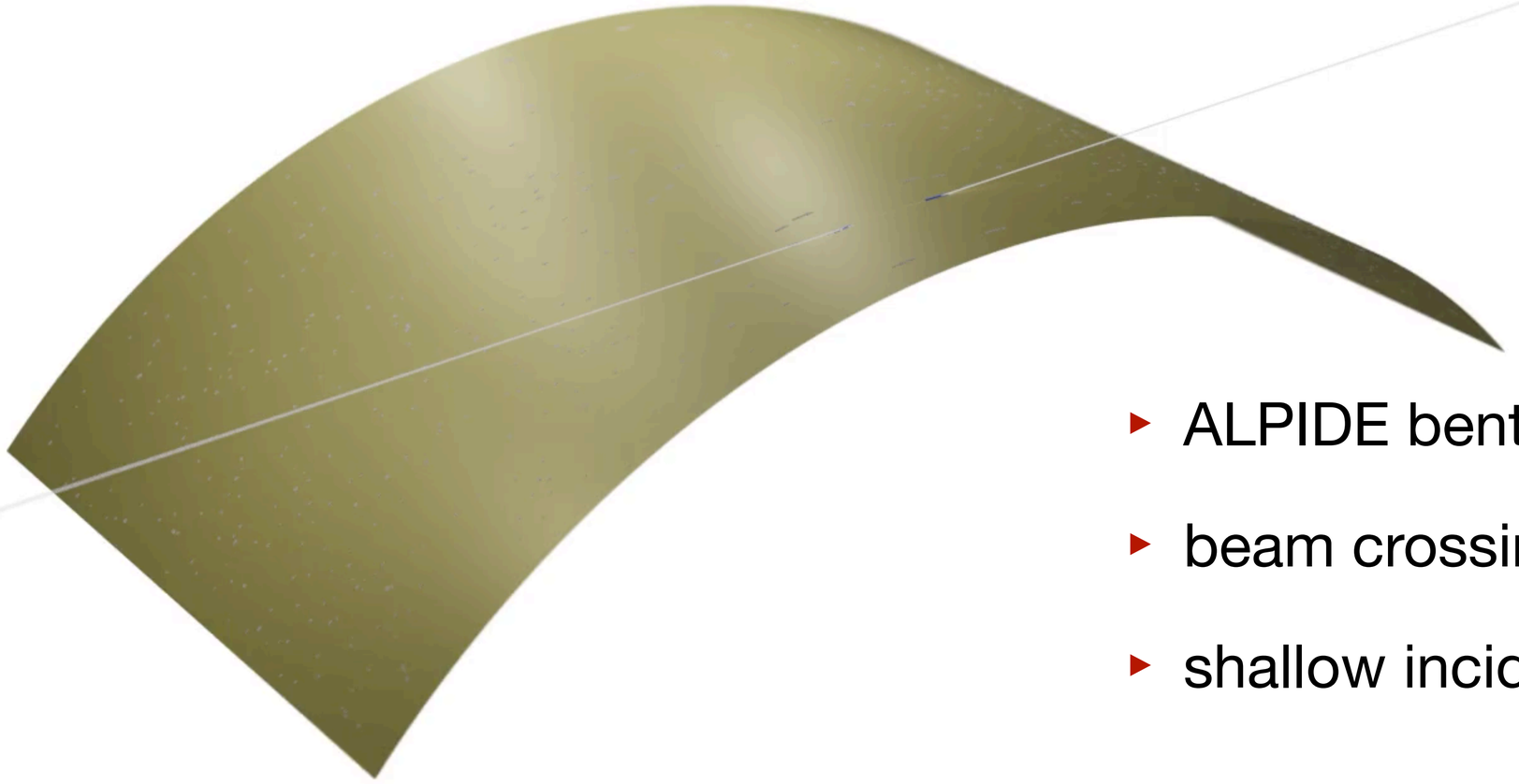
b) Aug/Dec 2020

bent ALPIDE
on cylindrical mount



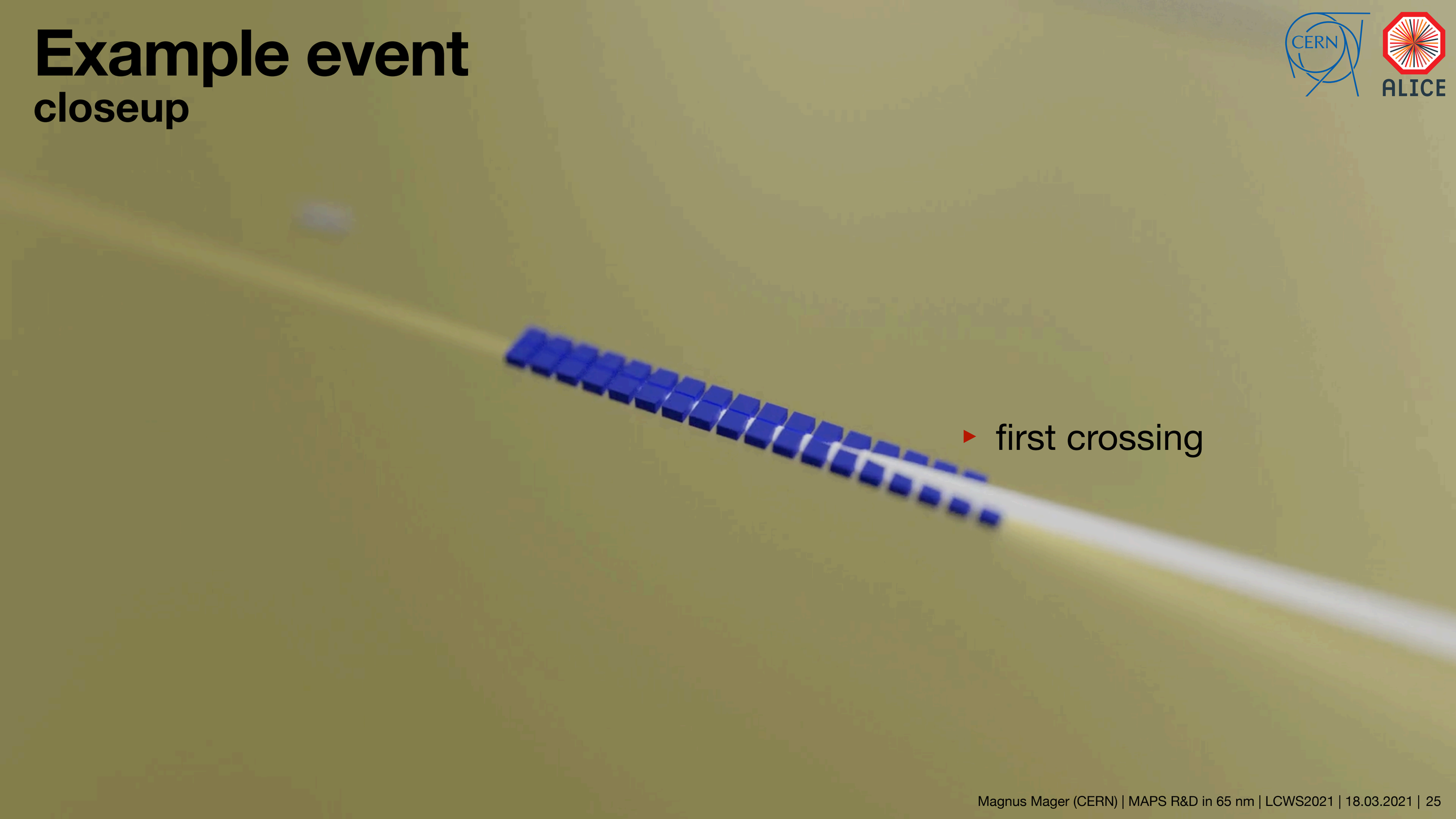


Example event

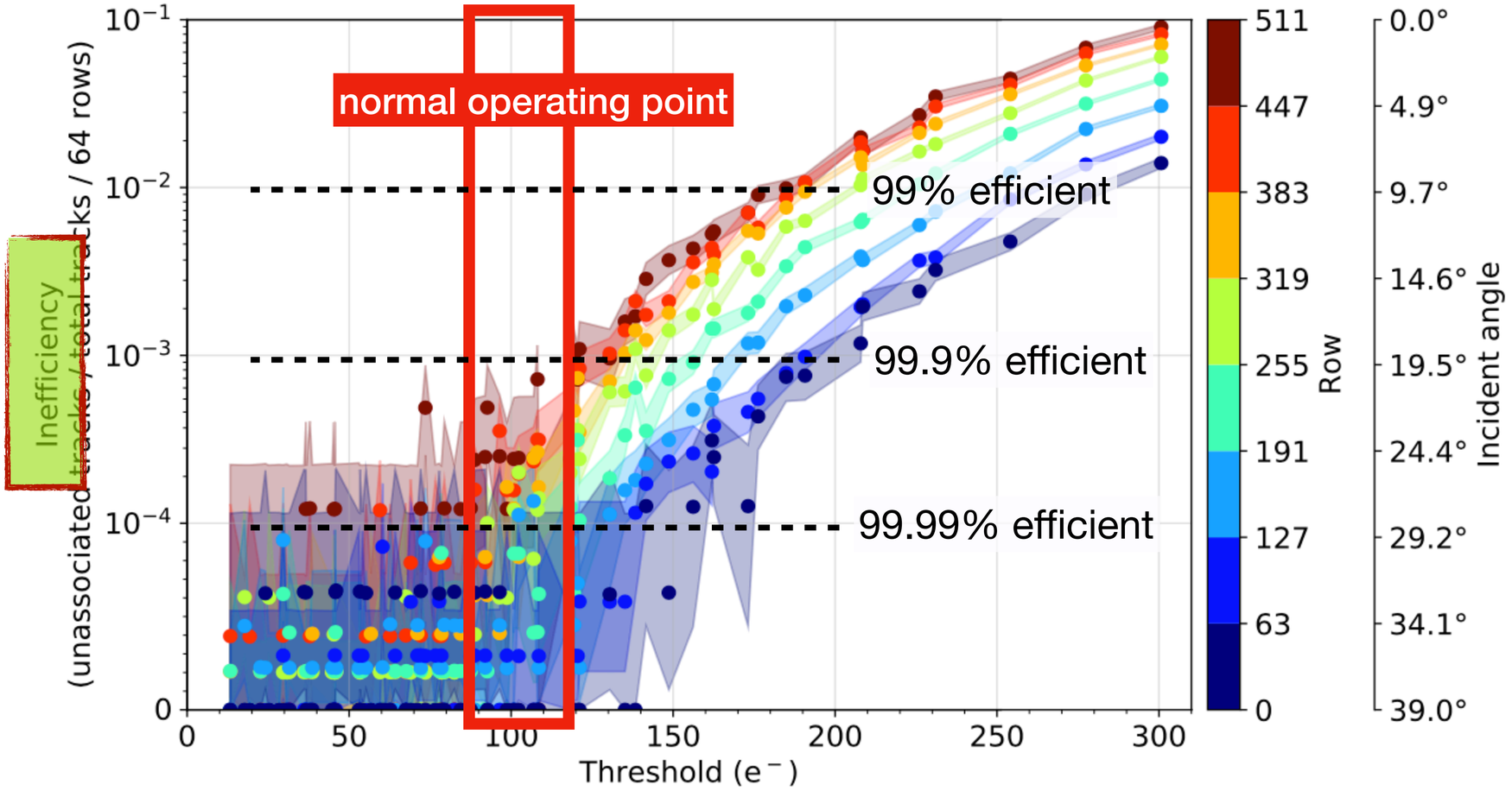


- ALPIDE bent to R = 18 mm
- beam crossing sensor twice
- shallow incident angles

Example event
closeup



Test beams
1st paper (draft)



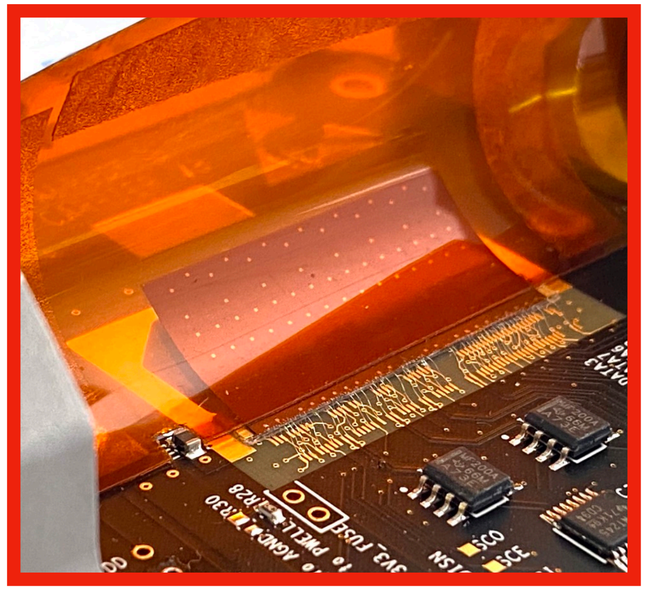


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

The chips just continue to work!

Summary

- **ALICE ITS2** is the first really **large-scale** (O(10 m^2)) application of **MAPS** in HEP
  - the development of **ALPIDE** marks a **new generation** of MAPS in terms of functionality and performance figures
- **ALICE ITS3** will push the technology even further, approaching the massless detector
  - R&D encouraged by LHCC in Sep 2019 and progressing at full steam
  - **65 nm prototype chips** were submitted, expected back mid 2021
  - feasibility of curved silicon detectors, marking **the start of a new chapter** on silicon-detector designs
  - fully integrated, **wafer-scale sensors** will allow large-scale **minimal material budget** applications

Thank you!