



Upgrade of the vertex detector of the Belle II experiment

Benjamin Schwenker, for the VXD Upgrade R&D Working Group of the Belle II collaboration



- Context of the current VXD
- Opportunity for a VXD upgrade
- On-going relevant R&Ds
- Full simulations for optimisation

The VXD roles within the Belle II setup



- Physics program @ SuperKEKB with Belle II
 - Thorough test of Std Model
 - Direct/indirect search for New Physics
 - Hadronic Physics



⇒ The Belle II physics book PTEP 12 (2019) 123C01

- Colliding e^++e^- at $\sqrt{s}=M_{Y(4S)}$ with luminosity $8x10^{35}cm^{-2}s^{-1}$

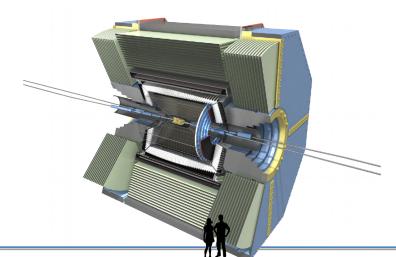
SuperKEKB collider implementing the nano-beam scheme @ high currents



"classical" B-factory detector + enhanced features

High collision rate

High beam-induced bkg



- The vertex detector (VXD)
 - Better vertexing ← lower boost
 - Smarter tracking ← higher hit rate
 - Tracking det.: VXD & Central Drift Chamber (CDC)
 - + Harsher radiation environment
 - + Belle II trigger rate ~ 30 KHz

The current VXD

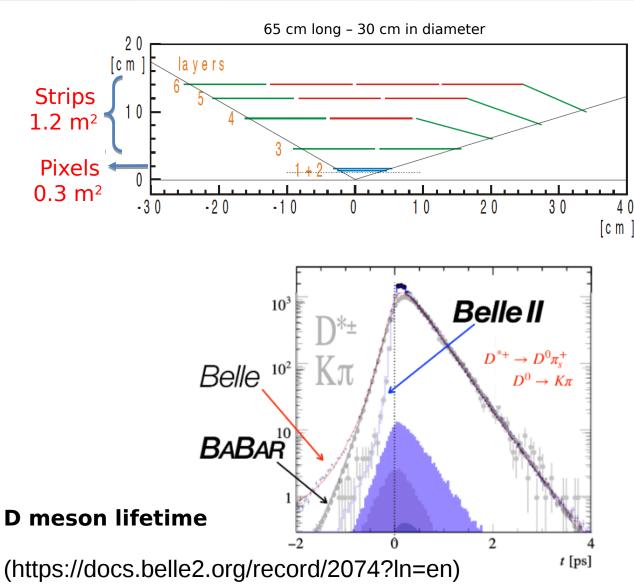


Two technology system

- SVD = Double-Sided Strip Detector
 - Read-out sensor connected on sensor = Origami
 - Hit time-stamping $\sigma_{t} \sim 2-3$ ns
 - Spatial resolution $\sigma_{s.p.}$ ~ 20 μm

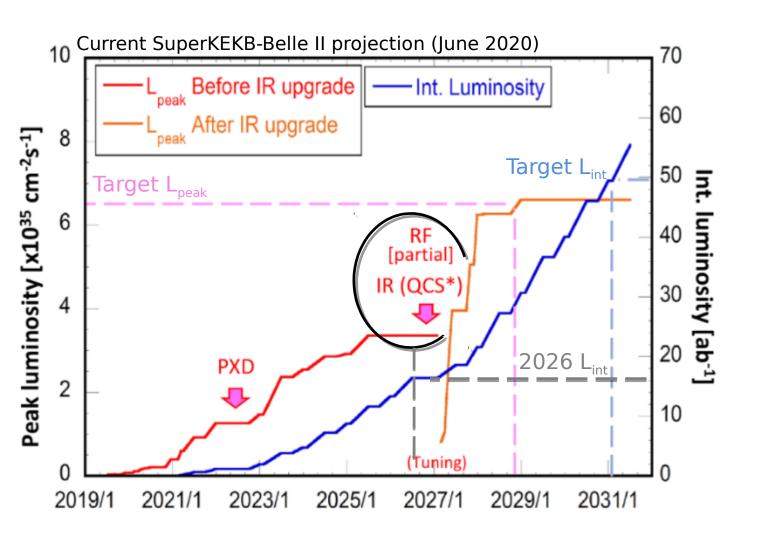


- PXD = DEPFET sensors
 - Very low material budget 0.2 % X_0 / layer
 - Small first layer radius = 1.4 cm
 - Long integration time 20 μs



A decade of operation → Upgrades?





Short term ~ 2026

- Long shutdown for QCS upgrade
 - Needed before next jump in luminosity

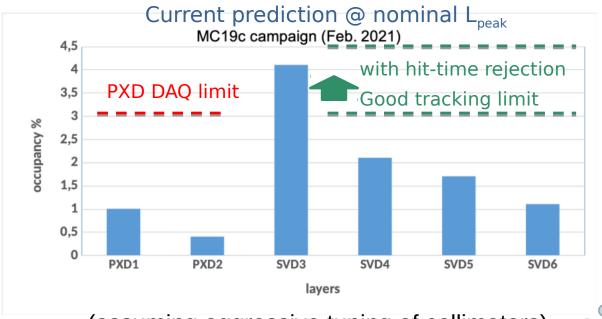


- Opportunity for Belle II sub-det. upgrades
 - Let's investigate possibilities...
 - short time → with currently ~available technology
- Longer term > 2030
 - Further increase of peak luminosity
 - Beam polarization?

Current VXD & nominal luminosity



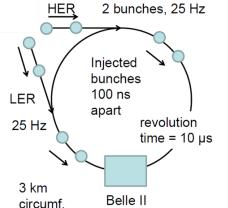
- Beam-induced background extrapolations
 - A long way to reach Data/MC ratio ~ O(1)



- (assuming aggressive tuning of collimators)
- Optimistic case with large uncertainties
 - Drastic change of beam optics for max L_{peak}
 - $β_v$ * today 800 μm / nominal 300 μm
 - Continuous injection effect not predicted

⇒ Belle II VXD Open workshop July 2019

- Tracking / vertexing
 - Track pattern recognition with SVD hits only required in // to tracking in Central Drift Chamber
 - Then extrapolation to match PXD hits
 - Also used for reduction of PXD output bandwidth
 - Final pointing resolution somewhat limited by beam-pipe thickness
 - 0.8 % X_0 ← partially required against synchrotron rad.





Requirements for short-term VXD upgrade



- exing & 10 dius range 14 135 mm

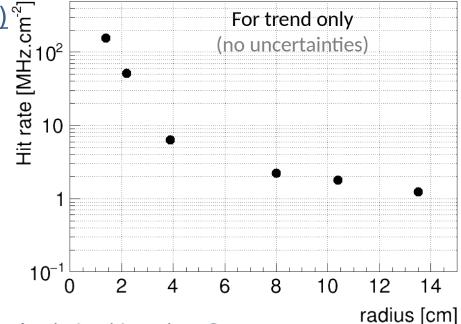
 single point resolution ≤10-15 μm

 Robust against environment for inner layer (r=1.4 cm)

 ""+-rate ~ 120 MHz.cm-2

 10 Mrad / year

 10 Mrad / year Vertexing & Tracking performances at least as good as current VXD
- Total material budget < (2x 0.2 + 4x 0.7) % X₀
- Based on current extrapolation with safety factor (x5) bear In mind large uncertainties (previous slide)
- Possibly **improve** performances
 - Impact parameter resolution
 - Tracking efficiency ($p_T < 100 \text{ MeV}$) & Fake rate
 - Faster High Level Trigger
 - Simplified track pattern recognition



Timing if pixelated tracker? rough estimate $\rightarrow T_{int} \lesssim 100 \text{ ns}$

Proposals for upgrades of Belle II

Received expression of interest (EOI) documents related to vertex and CDC <u>upgrade.</u>

EOI	Upgrade ideas scope and technology	Time scale
RMBA	Improved diamond readout electronics. Integration with SKB abort system	< 2026
DEPFETs	Adiabatcally improved replacement of existing system	2026
DMAPS	Fully pixelated Depleted CMOS tracker, replacing the current VXD. Evolution from ALICE ITS developed for ATLAS ITK.	2026
SOI-DUTIP	Fully pixelated system replacing the current VXD based on Dual Timer Pixel concept on SOI	2026
Thin Strips	Thin and fine-pitch double-sided silicon strip detector system replacing the current SVD and potentially the inner part of the CDC	2026
CDC	Replacement of the readout electronics (ASIC, FPGA) to improve radiation tolerance and x-talk	< 2026

Effort built up to answer within ~1 year



Which technology fit requirements?

Which technology can allow install in ~2026?



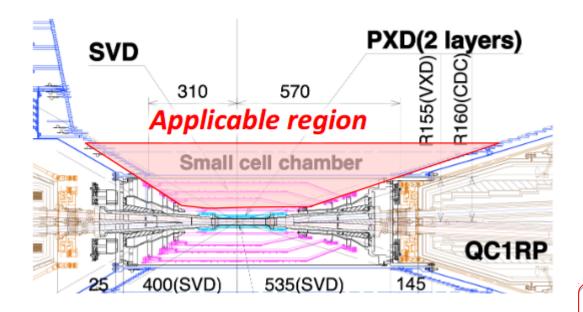
Thin and fine-pitch DSSD





Main R&D targets

- Handling higher hit-rate / SVD
 - 10 MHz/cm² (radii>3 cm)
- Improved resolution σ_z & decrease material budget
- Extensible to small cell chamber of CDC
- Trigger capabilities (L1 trigger)



	Sensor dim.	Thickness	Pitch P- side	Pitch N-side			
nt	40x125 mm ² 60x125 mm ²	300-320 μm	50-75 μm	160-240 μm			
,	(with intermediate strip						

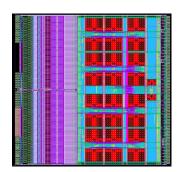
Upgrade 51

Curre

51.2x57.6 mm ²	140 μm	50 μm	75 μm

Solutions

- Double-Sided Sensors prototyped by Micron
- Front-End ASIC = SNAP128A under dvpmt
 - Based on SliT chip for g-2 (J-PARC experiment)
 - 180 nm CMOS process



- ENC = 650 e-
- Total power 2.8 mW/chan.
- 127 MHz output
- $\sigma_t \sim 8 \text{ ns}$
- 2k-depth memory
 → latency ~16 μs

⇒ First Sensor+FEE in 2021

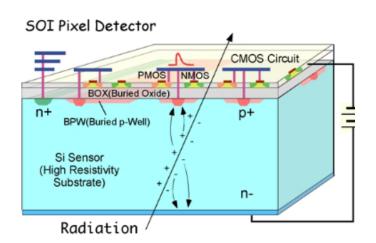
DuTiP - SOI pixel sensors





Main R&D targets

- 7 layer tracker
- Binary detector
- Low material budget
 - Monolothic technolgy
- Handling high-rate
 - Time-stamping < 100 ns
 - Global-shutter style



Dual Timer Pixel concept

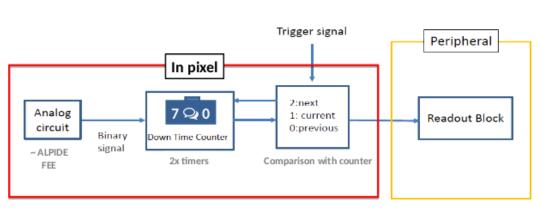
- 16 MHz clock for TIMER
- 2x 60 ns "integration" window
- Trigger latency 8 μs
- Occupancy << 0.1 %

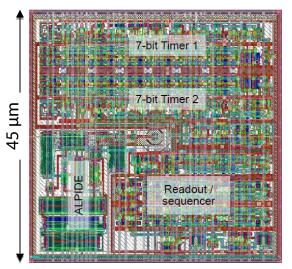


Pixel layout

SOI Implementation

- 0.2 μm LAPIS
- Full depletion
- Pixel pitch 45x45 μm²
- Sensitive thickness 50-75 μm





⇒ Initial prototype DuTIP 1 expected in March 2021

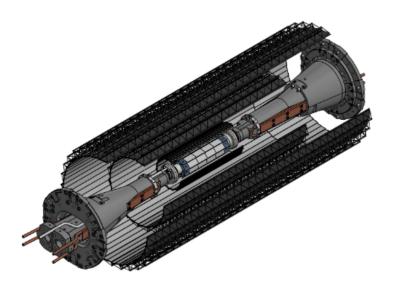
DMAPS - VTX

@ Bonn, CPPM, CERN, IRFU



Main R&D targets

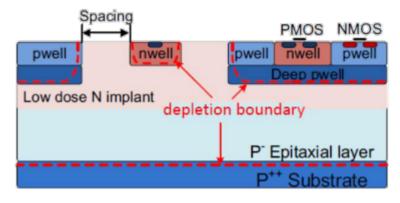
- 5 (7) layer tracker
- Monolithic and low power
- Small and fast pixels in all layers
- Rad. hard: TID 100Mrad & 10¹⁴ n_{eq} cm⁻² NIEL



- 0.1% X₀ inner and 0.3-0.5% X₀ outer layers
- Simplified services, all layer for tracking on HLT

Depleted monolithic active CMOS pixels

- Evolution of TJ-Monopix and Mimosis chip families
 - TJ Monopix 2 matrix as workhorse
 - Column drain architecture ok for Belle II
 - R&D for Belle II EoC needed
- Small pixels: 30x30μm²
- Fast: 25ns integration time (100ns time window sufficient)
- Occupancy << 0.1 %

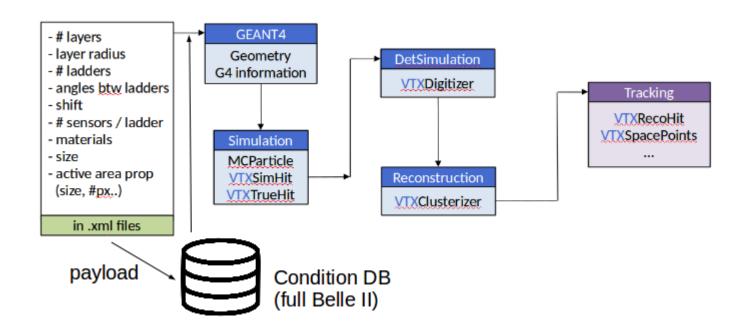


⇒ TJ-Monopix 2 being tested now.
1st Belle II dedicated chip (Obelix) in 2022

Full simulation of vertex upgrade in Belle II



- Replace PXD & SVD with generic pixel layers and connect to tracking
 - Implemented in Belle II software as new sub-detector (VTX) of Belle II
 - Part of Geant4 detector simulation with realistic backgrounds
 - Part of overall event reconstruction => physics benchmarking

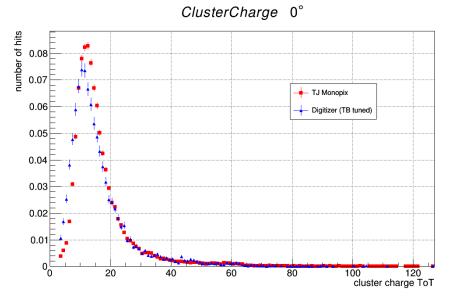


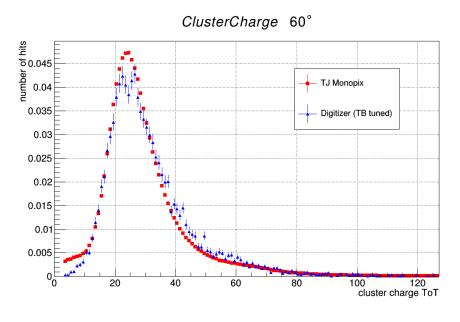
Simulated pixel response



Context = new vertex det. with all VXD fully pixelated = VTX

- Realistic pixel sensor model
 - Digitizer assuming
 - fully depleted thin layer 30 μm
 - Pixel 33x33 μm² with 7bits Time over Threshold
 - Tuned with Monopix-1 beam data
 - JINST 14 (2019) C06006
 - Pitch 40x40 μm²
 - ToT 6 bits





Monopix-1 data from **Bonn group** Test-beam at DESY with 5 GeV e-

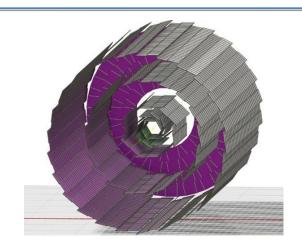
Results by T.Fillinger (Strasbourg), B.S. (Göttingen), C.Wessel (Bonn)

Simulated tracking performances



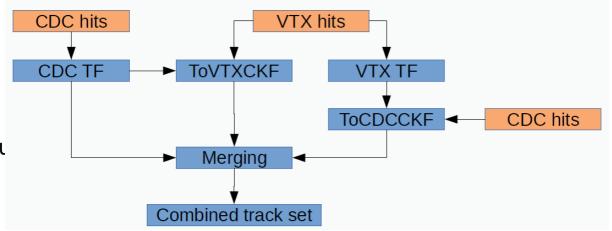
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<u>Geometry</u>

- Taken from fast simulation
- 5 or 7 barrel layers with/without 2 forward disks
- Crude layer description but with targeted material but
 - \rightarrow per layer: 0.1 % X₀ for radii <4 cm then 0.3 % X₀



<u>Full tracking chain</u>

 VTX standalone CDC standalone

then combined

High Level Trigger All VTX layers included in pattern-reco. \Rightarrow

Results by T.Fillinger (Strasbourg), B.S. (Göttingen), C.Wessel (Bonn)

beneficial to

Simulated tracking performances



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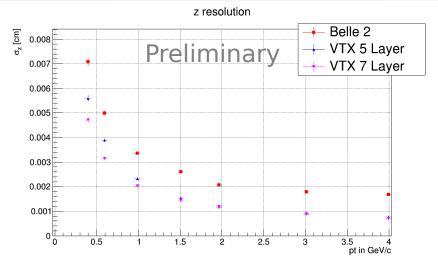


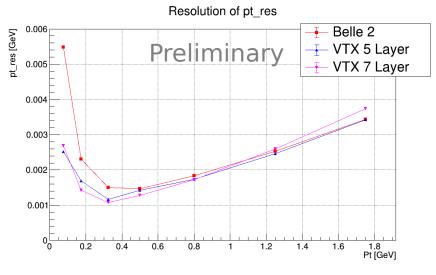
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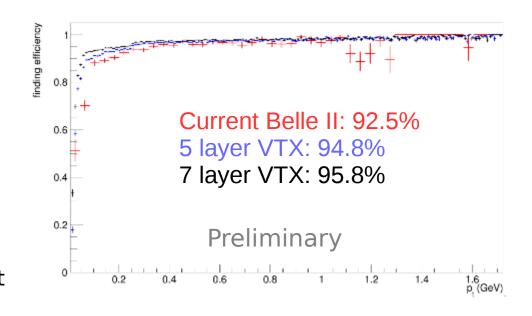


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Summary & Outlook



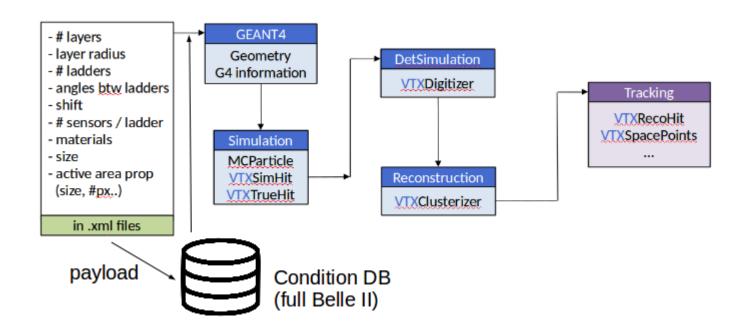
- There is an opportunity for an upgraded vertex detector (VXD) in Belle II
 - Shor-term target QCS upgrade ~ 2026
 - Main requirement = additional robustness / hit-rate & radiation environment
 - Also opportunity to enhance vertexing & tracking performances
 - ⇒ Large fraction of Belle II dataset will be collected after upgrade in 2026
- Present work status
 - Demonstrate feasibility of EOIs → test prototypes of submitted chips
 - Full simulation for fully pixelated VXD <u>option</u> → physics benchmarking
- Upgrade goals revolve on low material, low power, fast pixels to find signal tracks in large backgrounds
 - Common grounds with LC community

⇒ It is time to join, R&D contributors outside Belle II welcomed!

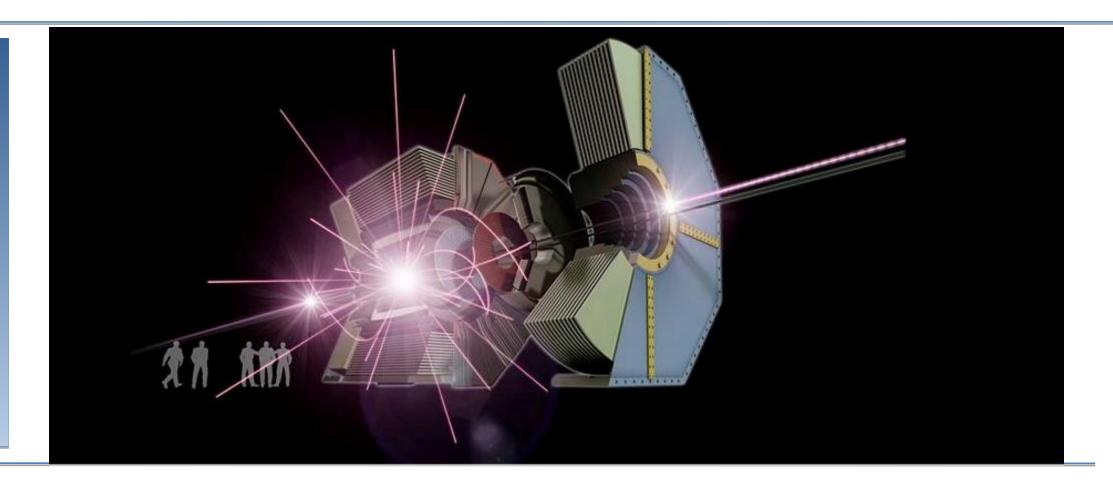
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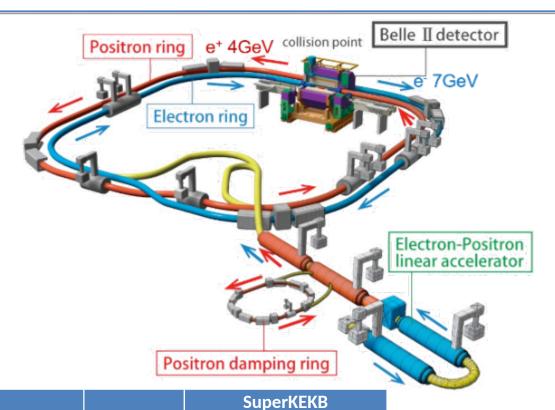


SUPPLEMENTARY SLIDES

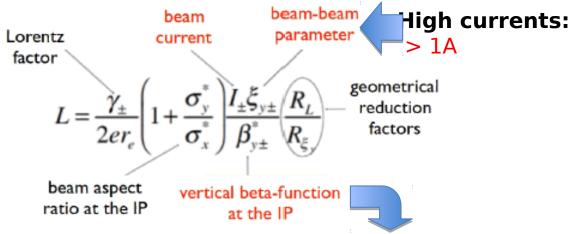


SuperKEKB collider





Recipe to high luminosity

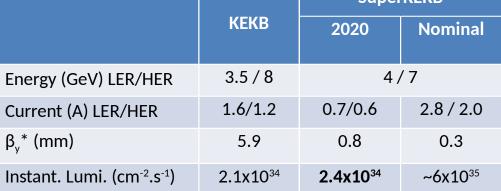


Nano-scale beam size:

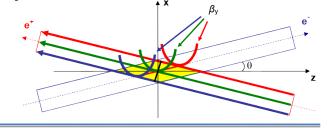
 $\sigma_x \times \sigma_y \sim 10 \mu m \times 60 nm$ $\beta_y * << 1 mm$

& specific beam crossing features

Crossing angle (83 mrad) + crab waist
(80%)

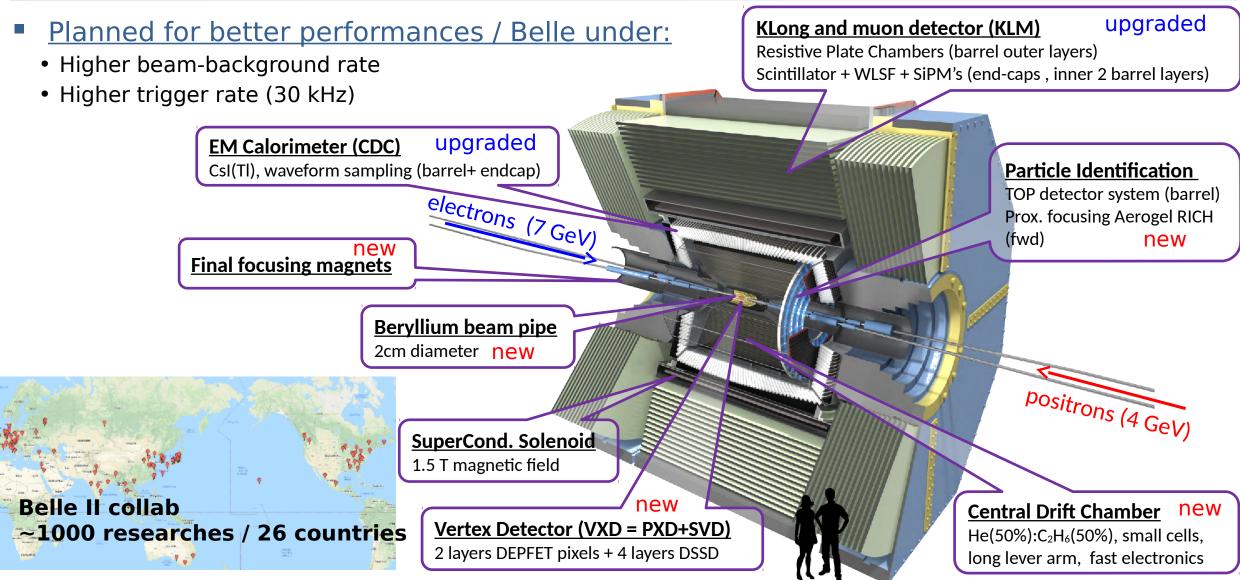


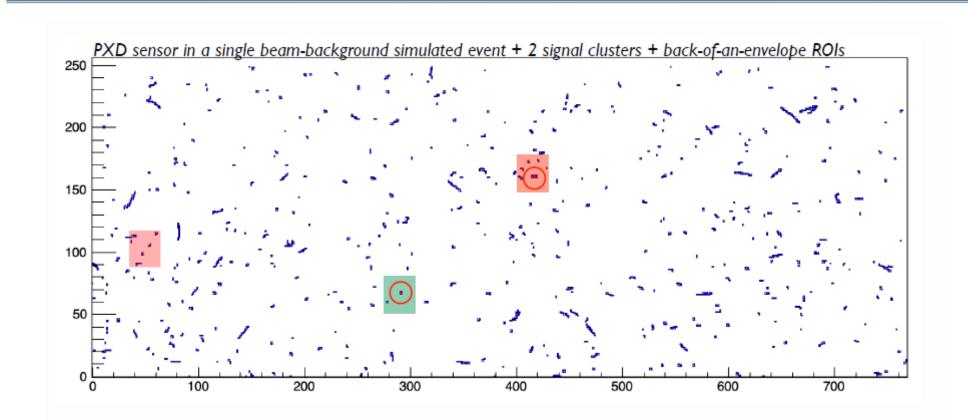
Cost = severe induced beam background



Belle II detector







 ◆ A PXD sensor frame + the ROIs from the HLT + nominal expected background

From Eugenio Paoloni, July 2019

CMOS pixel sensor options

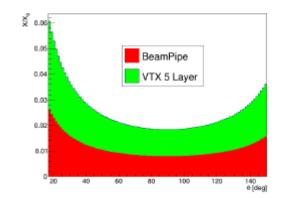
⇒ Various R&D on-going outside Belle II

Sensor available 2020	MIMOSIS-1 (CBM-MVD)	Belle II requirements "First guess"	MONOPIX-2 (ATLAS-ITK)	ATLASPix3 (ATLAS-ITK)			
Time precision (ns)	5000	50 to 100	25	25			
Pixel pitch (μm²)	30x27	30x30 to 40x40	33x33	150x50			
TID (Mrad)	5	100	100				
Power (mW/cm²)	~50	< 100 to 200	~150	~140			
Trigger delay (μs)	No trigger	5 → 1 0	lor	ng			
	In test IPHC		Submitted Bonn, CERN, CPPM	Tested Barcelona, CPPM, Gene Heidelberg, KIT, Liverpo			
180 nm HR-CMOS process → ~full depletion ← 180 nm HV-CMOS process							
Periphery In pixel Image: Image:							

Full pixelated VXD: Geometry details

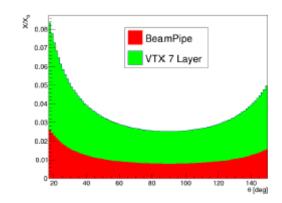
VTX with 5 pixelated layers

5 layers	1	2	3	4	5
Radius (cm)	1.4	2.2	3.9	8.9	14.0
# ladders	6	10	8	18	26
Sensor type	Α	Α	A'	A'	A'
# Sensor rows along z direction	1	1	2	4	6

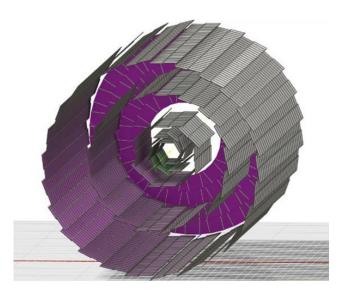


VTX with 7 pixelated layers

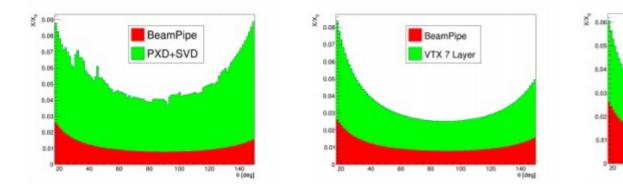
7 layers	1	2	3	4	5	6	7
Radius (cm)	1.4	2.2	3.5	6.0	9.0	11.5	13.5
# ladders	6	10	14	12	18	22	26
Sensor type	Α	Α	Α	A'	A'	A'	A'
# Sensor rows along z direction	1	1	2	3	4	5	6

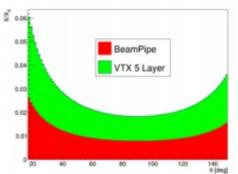


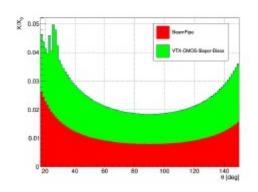
5 layers + 2 disks



Material budget full pixelated VXD







Tower Jazz 180 nm time response simulations

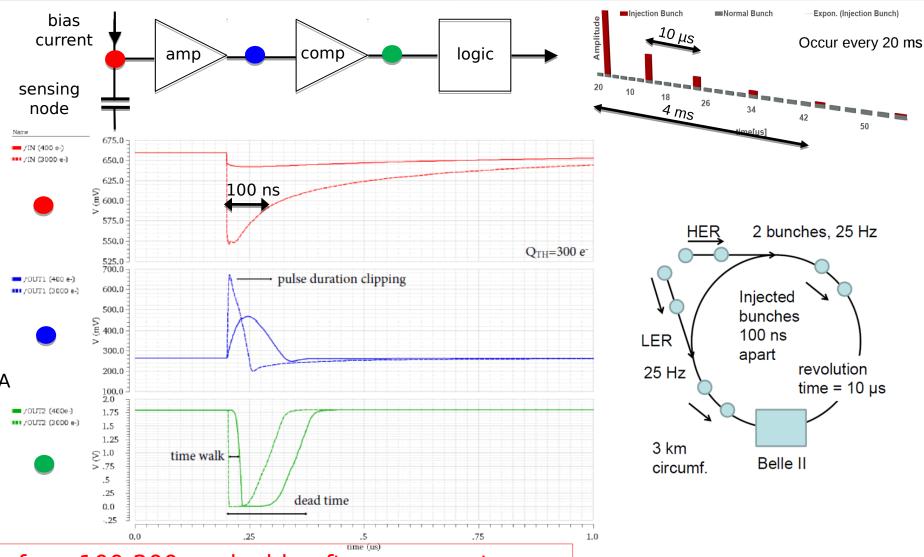
Front-end structure in-pixel

Simulated behavior (MALTA case)

 From I. Berdalovich, JINST 13 (2018) C01023

 Short recovery time for node requires I_{bias}~500 nA → 0.9 µW/pixel

 ALPIDE with μs timing reaches 0.040 μW/pixel



 \Rightarrow Suggest gating injection for \sim 100-200 ns doable after comparator

DEPFET pixel sensors Belle II DEPFET collaboration Data Drain CU



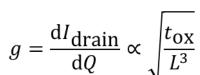
Current Belle II - PXD

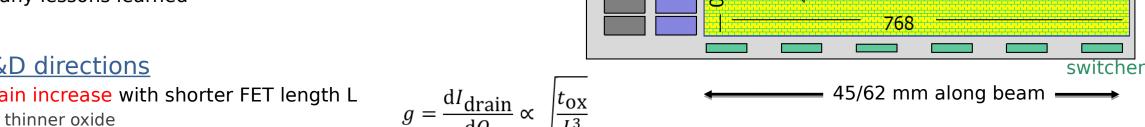
- First use of the technology in HEP experiment
- Many lessons learned



- Gain increase with shorter FET length L
 - → thinner oxide
 - → higher signal → improved rad. tolerance

$$g = \frac{\mathrm{d}I_{\mathrm{drain}}}{\mathrm{d}Q} \propto \sqrt{\frac{t_{\mathrm{ox}}}{L^3}}$$

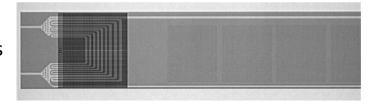




- Rotating read-out direction + switcher intergration
 - Speed x3
 - Pixel size along beam x1/2



- Require advanced processed
- Speed x2
- All-silicon module improvements
 - Microchannel cooling
 - Thinner drivers



250 1536

Drain Current Digitizer

Within reach

- T_{int} : 20 \rightarrow 10 μ s
- Improved σ_z
- Mat. Budget 0.21 → 0.15 % X₀

switche

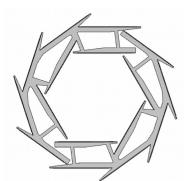
Integration concept

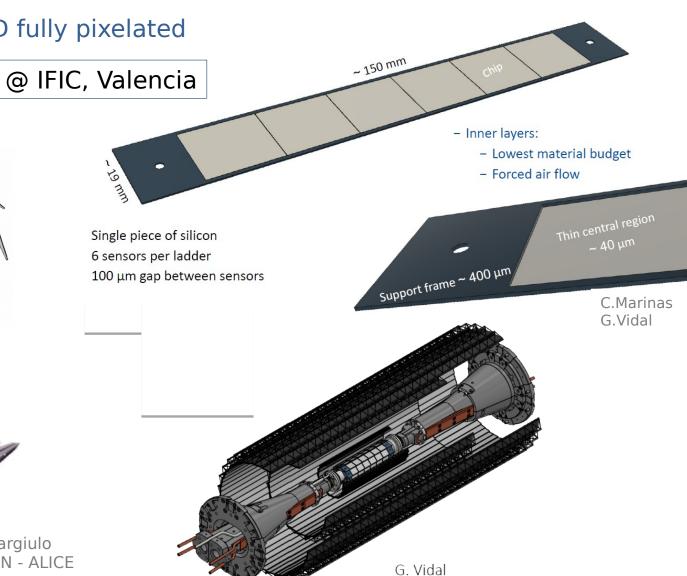


Context = new geometry with all VXD fully pixelated

Inner layers = full silicon module

- 2 to 3 layers, radius < 4 cm
- Target 0.1 % X_0 / layer





- Outer layers ~ ALICE.
 - 3 to 4 layers, radius 4-14
 - Target 0.3 % X₀ / layer

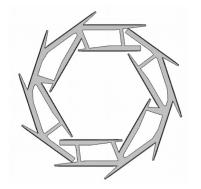


Integration concept



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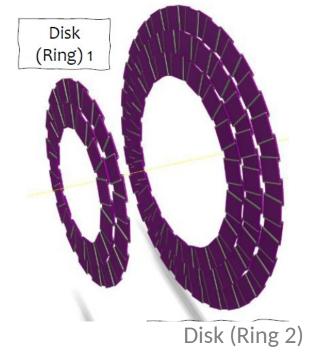
- Outer layers ~ ALICE-ITS la concept
 - 3 to 4 layers, radius 4-14 cm
 - Target 0.3 % X₀ / layer

Forward disks

- 2 disks at z = 16.5 & 25.6 cm
- Target 0.3 % X₀ / layer



F.Bosi M.Massa



C.Gargiulo **CERN - ALICE**