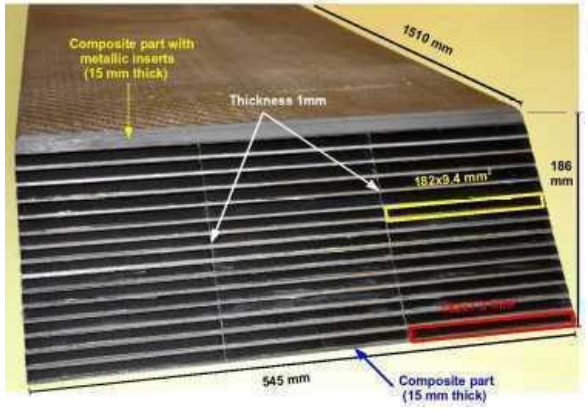
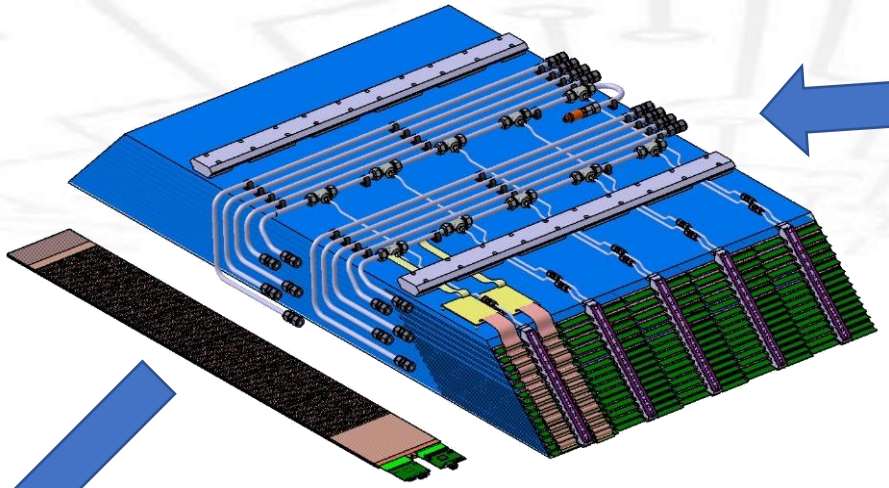
New front end board for ILD Si-W ECAL

Jérôme NANNI

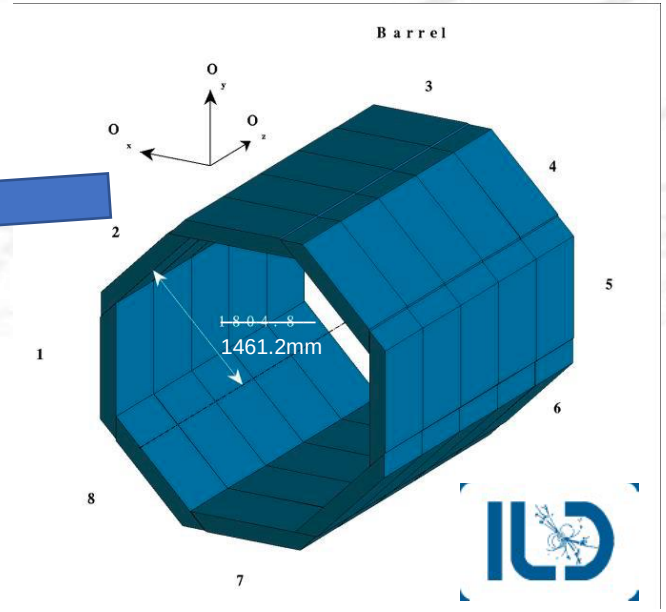
Introduction



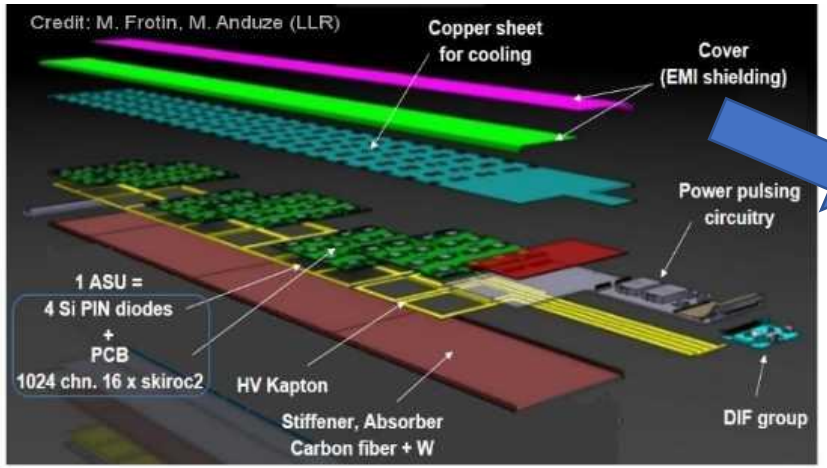
(13-15 double layers)



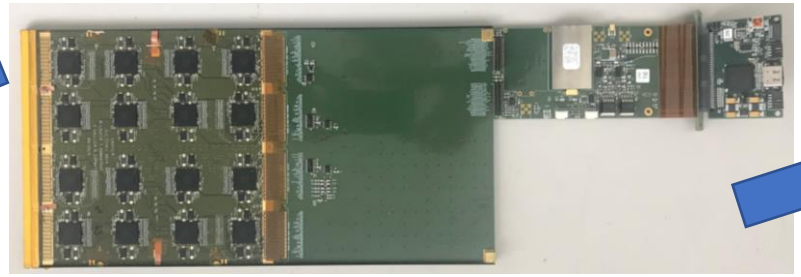
Module (5 columns x 13-15 alveoli)
Double long slab per alveolus



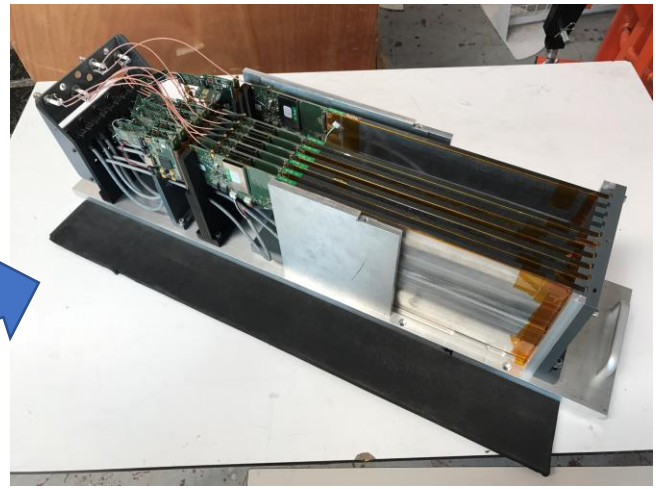
ILD & SiW-ECAL barrel
(8x5 modules)



Assembly of long SLAB (8-12 boards)



Short SLAB (4 x 6'' wafers)



SiW-ECAL prototype (8 layers)

Electrical long SLAB

2017-2018:

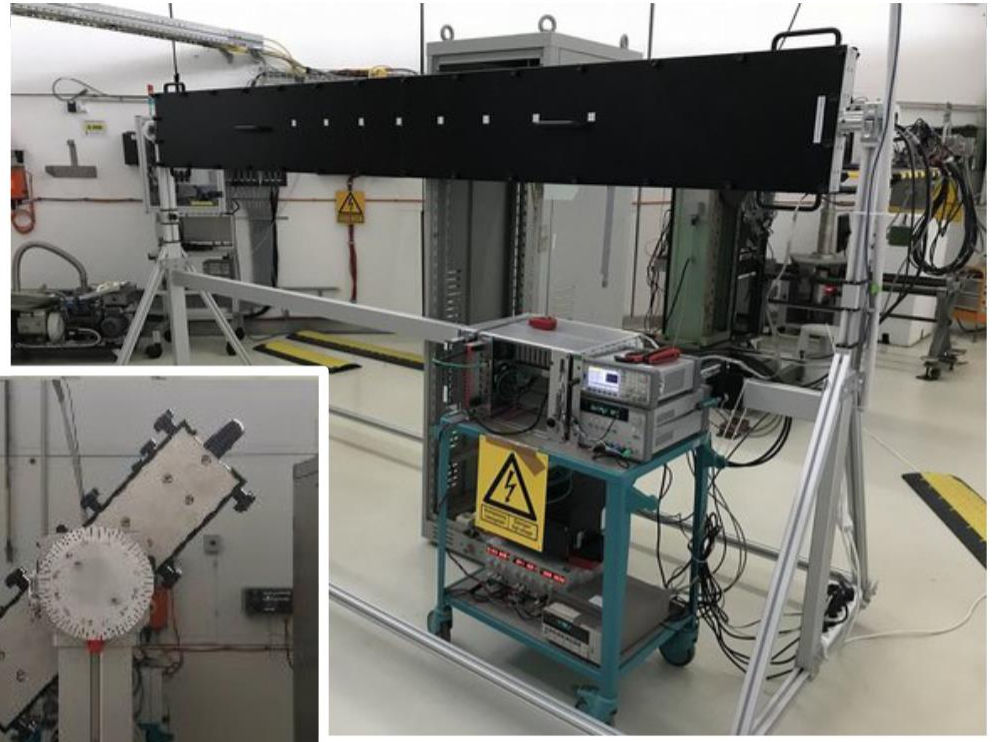
- Design and assembly (8 boards chained)
- Test beam @DESY
- Results (see presentation @ LCWS 2018)

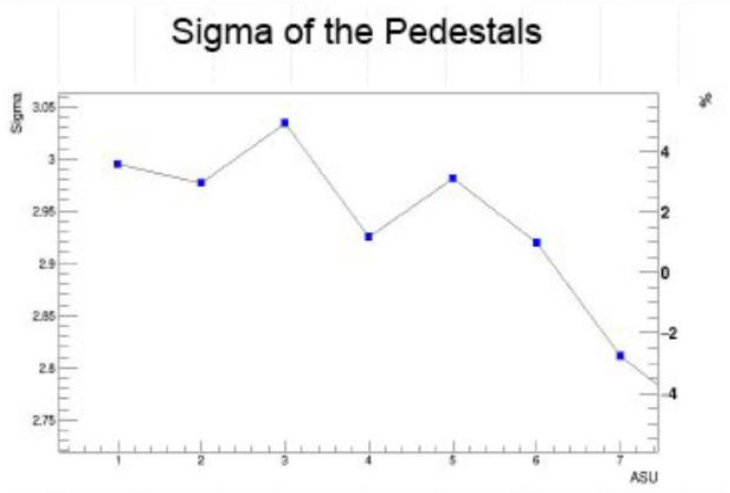
2019:

- Continue measure and analysis to confirm TB observations
- Voltage drop cross with bandgap distribution

2020 :

- Start design of the new front end board





Benefit / default of electrical long slab

Important voltage drop (5%)

Need extra electronics to configure more than 4 boards

Need too many manipulations to move or replace board

Mini wafers not adapted to observe cumulative effect

Show feasibility of electrical long slab

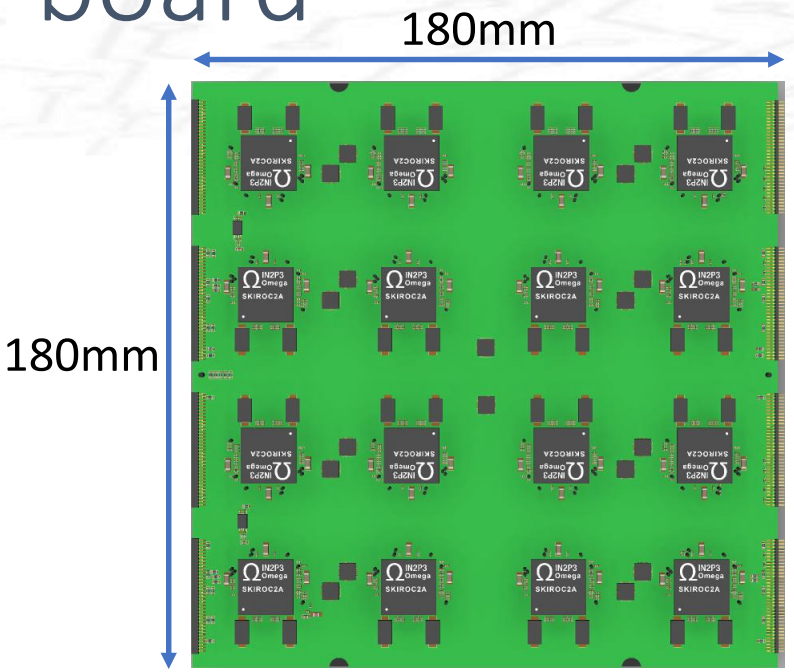
Measure MIP on each board (with mini wafer for costs reductions)

For final project, we need new board & new mechanics

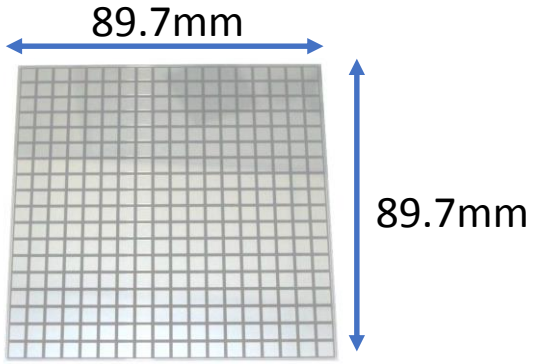
→ Move to physics long SLAB (fully equipped of Si wafers

Properties of the new front end board

- 16 chips Omega SK2A to read pixels
- 2 power supply AVDD and DVDD
  - Generate local analog power per chip
  - Generate local digital power per partition
- 1024 pixel on bottom side to glue 4 x 6’’ Si wafer
- Drive high voltage up to 350V for 750µm wafer
- Configure 10 boards chained
- Send data from 2 partitions of 80 chips
- Keep or increase performances (ex: S/N of 20)
- Precision on flatness, dimensions, … ±25µm
- High precision wafer placement (100µm between wafer)

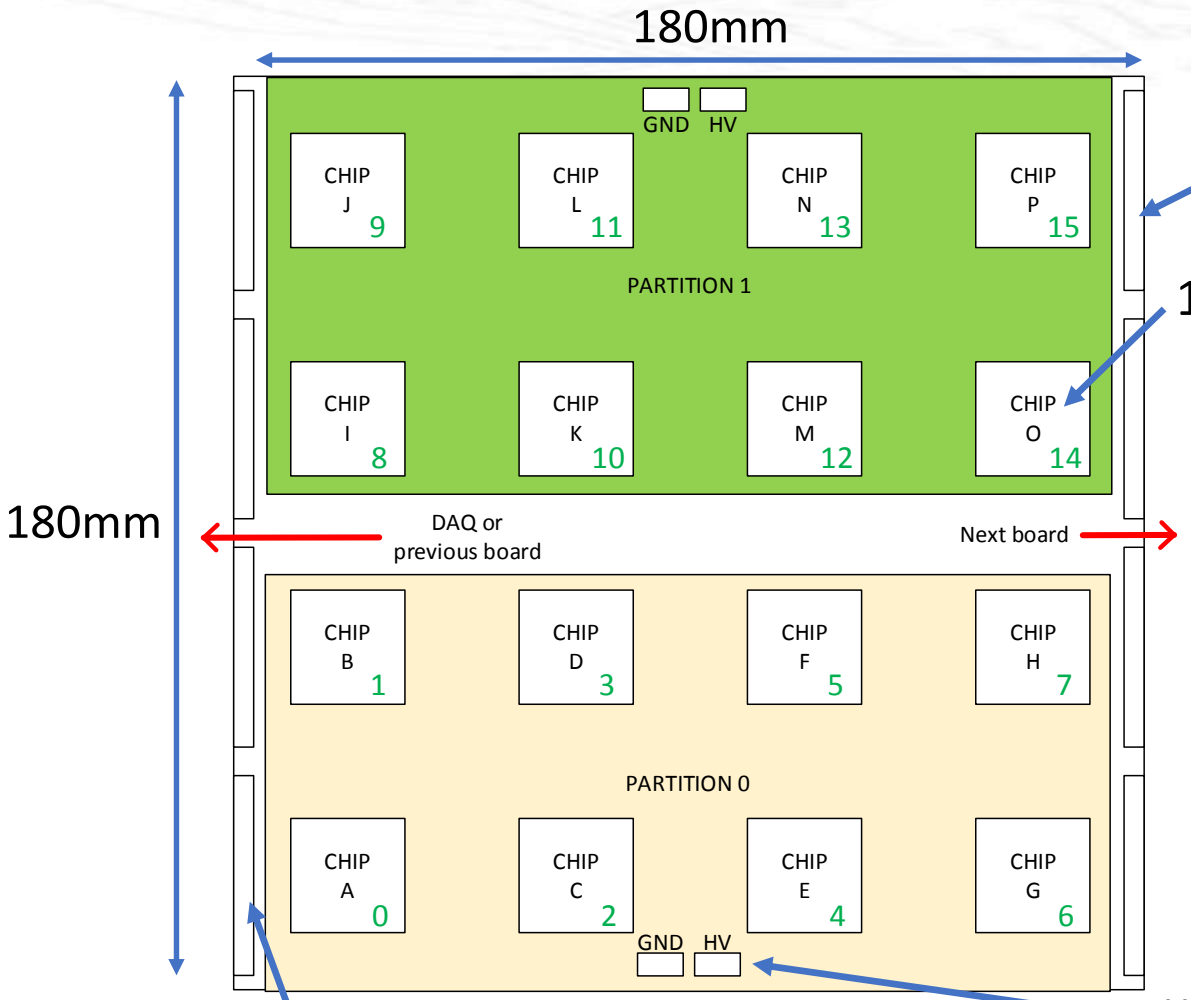


3D view from Cadence Allegro



6’’ wafer (16x16 pixels)

Board synoptic



4x 35 pins female connector

Gradconn BB02-WF352-K03-000000

16 chips Omega SK2A

2 partitions for slowcontrol and data flow.

→ Could be link or bypass with 0Ω resistor

→ Test mode for 1 chip only per partition

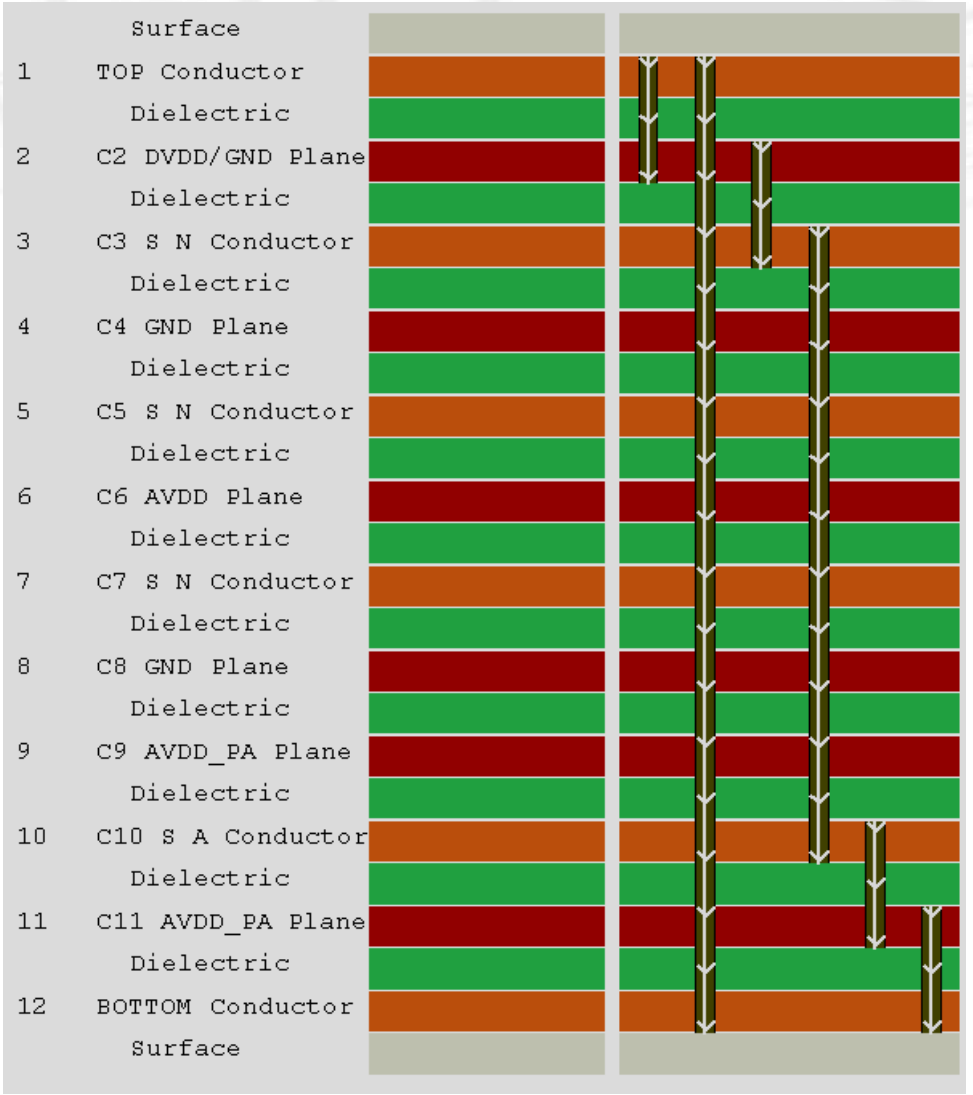
4x 35 pins male connector

Antelec AM1C100352GCMSH1BA

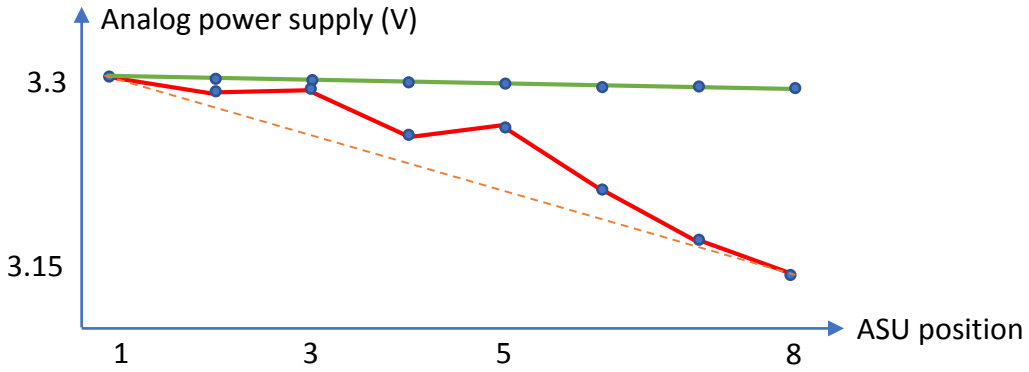
High voltage pad for wafer with kapton connection

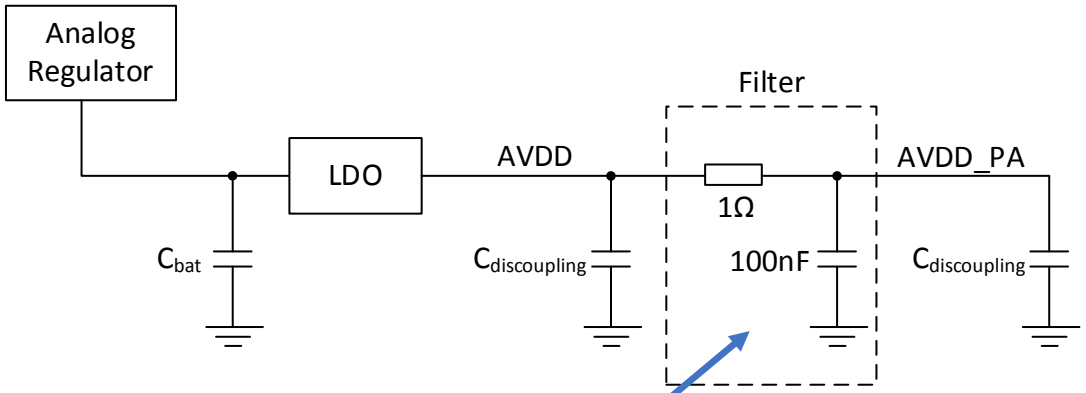
Stack-up board

- Keep layer for power
  - 2 x GND
  - 2 x AVDD_PA
  - 1 x AVDD
  - 1 x DVDD
- Minimize crosstalk
- Keep shielding mush as possible
  - AVDD_PA for preamplifier signals
  - GND for analog and digital signals
- Move away digital from preamplifier line
- Adaptation lines
  - 50Ω for single ended
  - 100Ω for ddifferential lines



Power distribution





Add filter to generate local preamplifier power supply

In the electrical long SLAB, 8 boards are chained. Regulator upstream produce analog 3.3V for all chips of all boards.

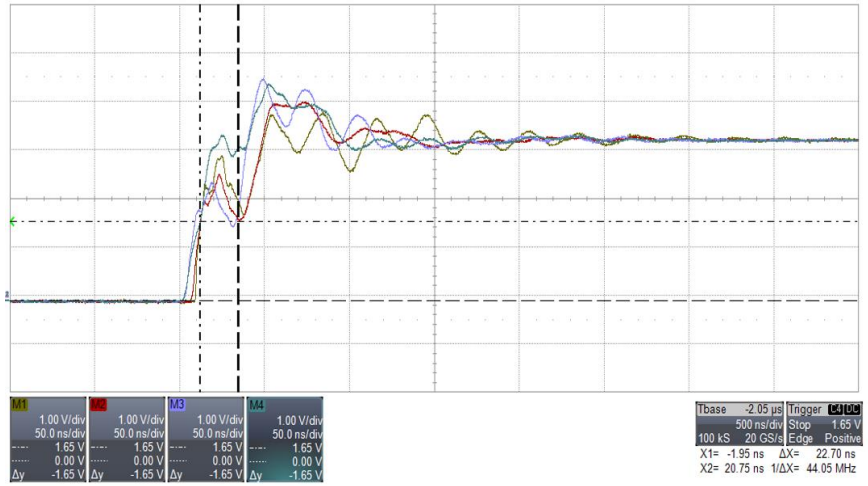
Due to resistivity of layer per board on analog 3.3V, we measure voltage drop along the long SLAB coupled with bandgap distribution.

→ We decide to generate local power supply with LDO (Low Drop Out) to cancel voltage drop.

Configuration lines (1/2)

In the electrical long SLAB, we have some difficulties to configure more than 4 boards. Configuration clock line is not design for variable number of boards chained.

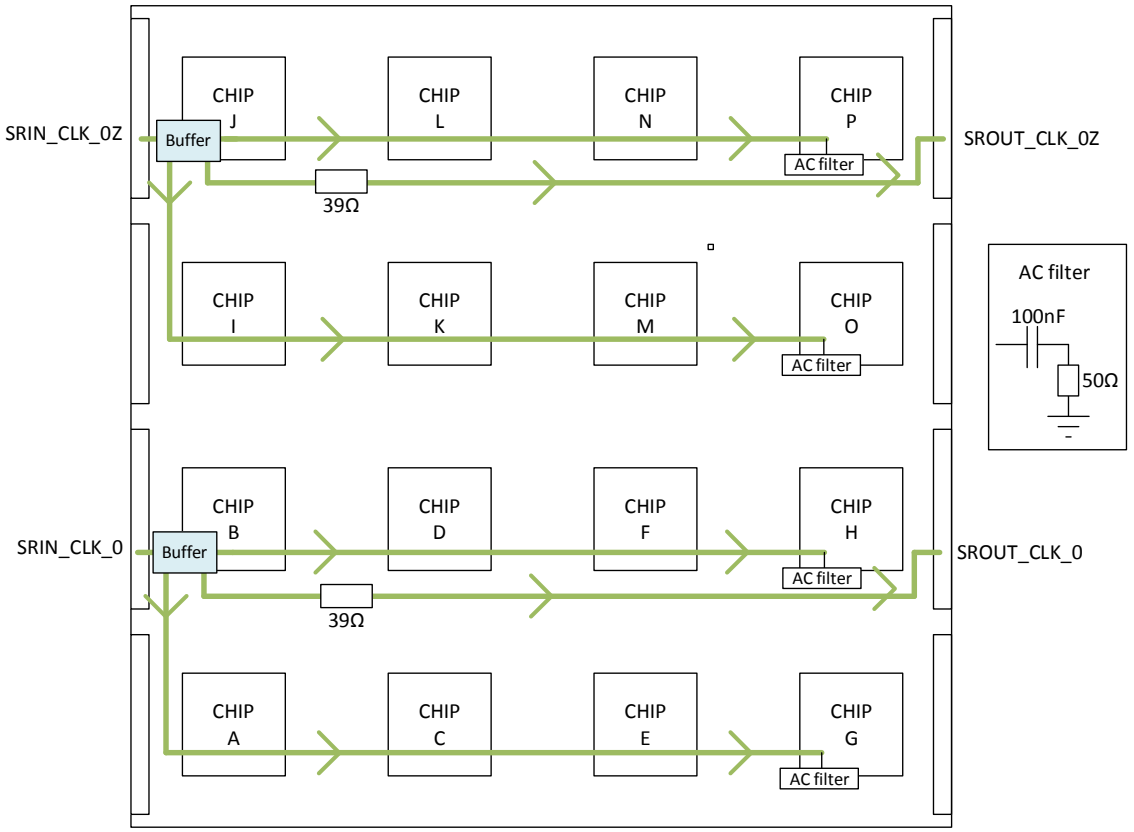
→ Only 1 buffer upstream drive all readout chips, not adapted for variable wire length.



→ Need long studies to find solution with hardware

- Make simulations with Sigrity
- Place filter to shift the reflection effect on the configuration clock

Configuration lines (2/2)



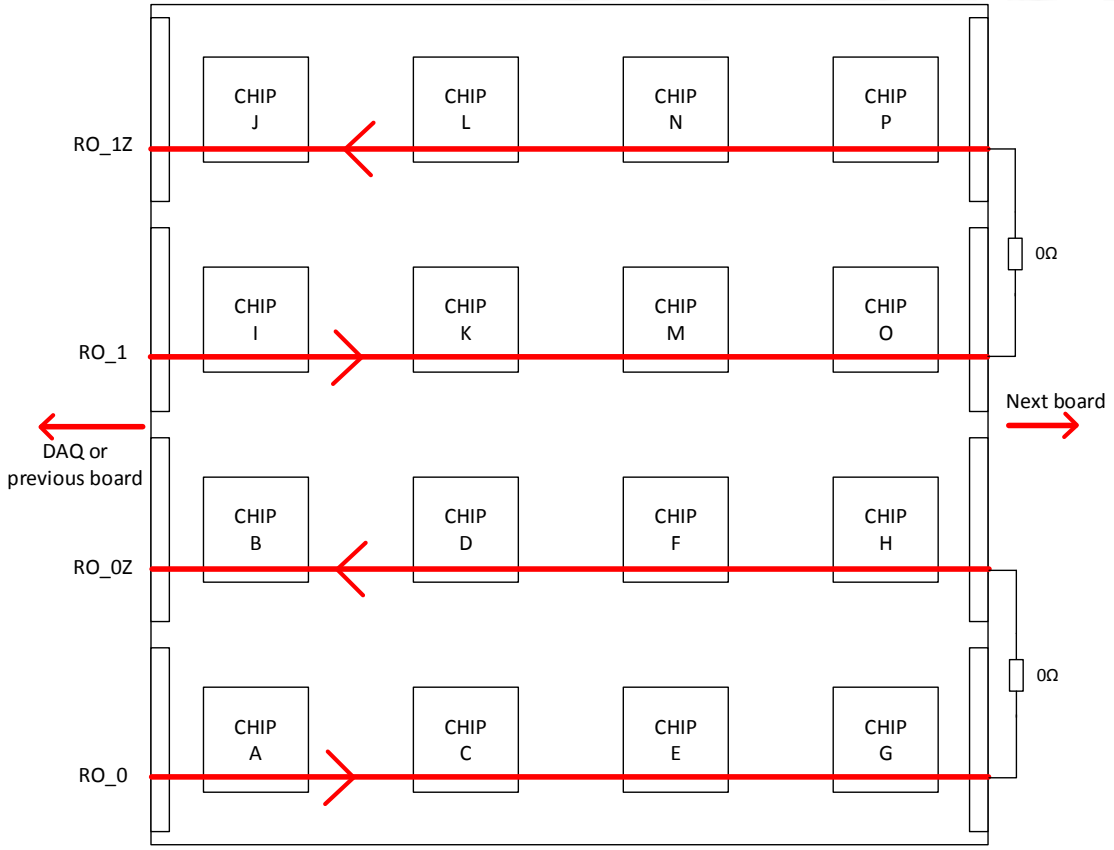
Need system to reduce length of clock line and load capacitors.

→ Add buffer or logic gates, dedicated per local partition and for next board

→ Add AC filter to reduce reflection effect on each partition.

→ Configuration clock is drawing to limit stub and reflection

Data lines



Each chip is chained in coil per partition.

Omega SK2A chips are not able to drive signal on 180 cm (10 boards).

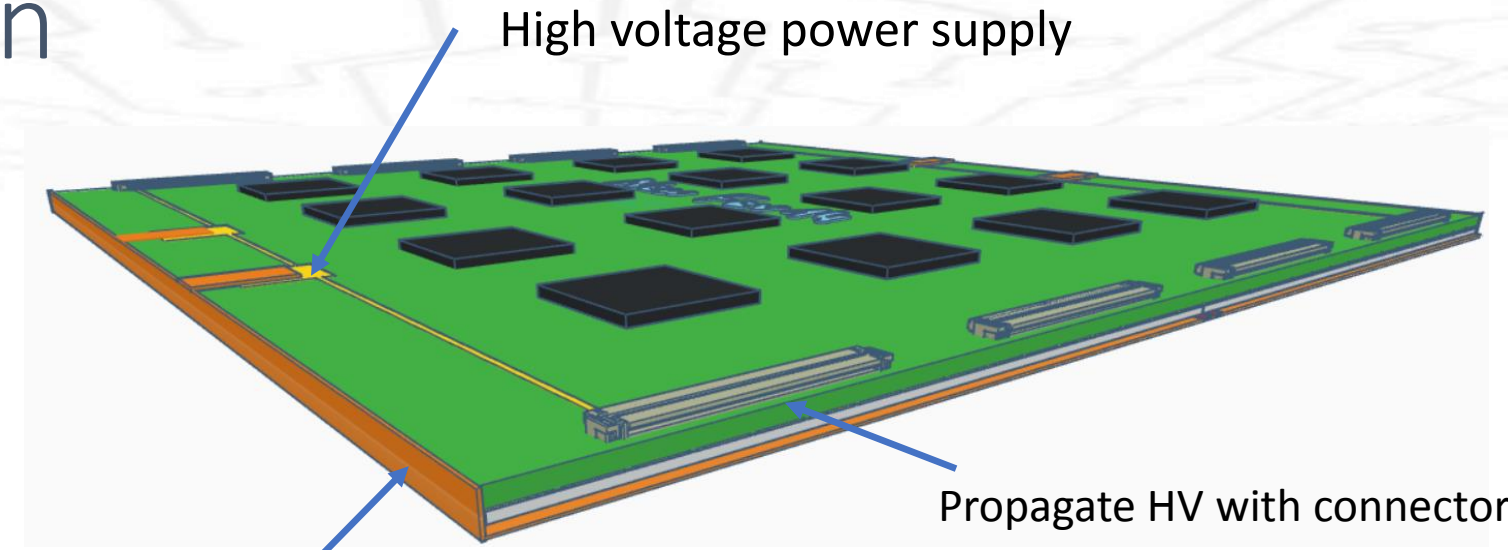
Possibility to bypass chip if necessary with slowcontrol or shunt resistors.

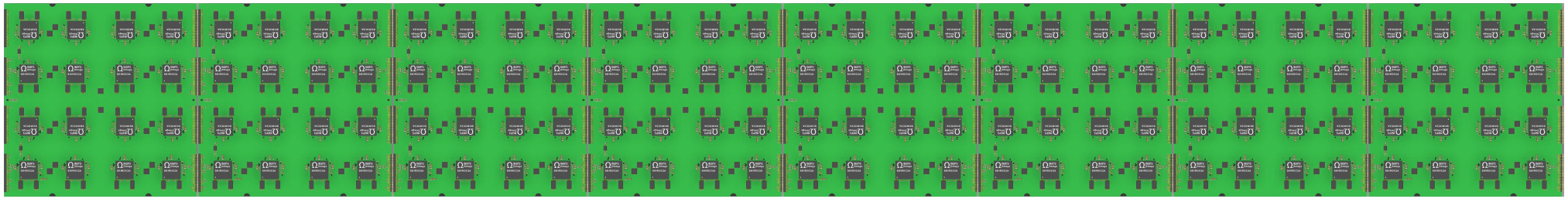
→ The last chip of each partition must be the closest of DAQ.

→ Board is divided in 2 partitions to reduce readout time

Mechanics solution

- Kapton is enlarge to protect 2 sides of the system during insertion or slice in the support.
- High voltage is driven by the board instead of the kapton for assembly, maintenance and costs reductions.

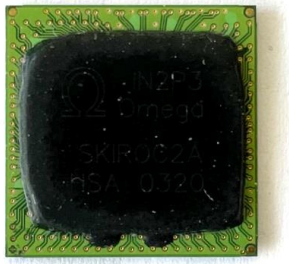




New packaging for SKIROC2A chips

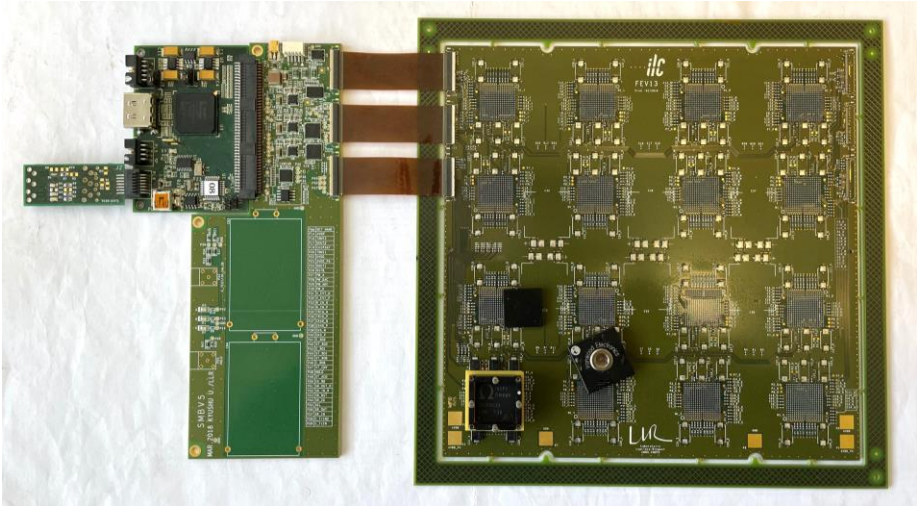
- Previous company Novapack stop BGA activities
- Very difficult to find a company for BGA encapsulation.
- Test a new company Aptasic

  → No conclusive results
- Contact with a new Chinese company (recommend by Omega)
  - Package BGA size: 17mm x 17 mm
  - Thickness: 1,2mm



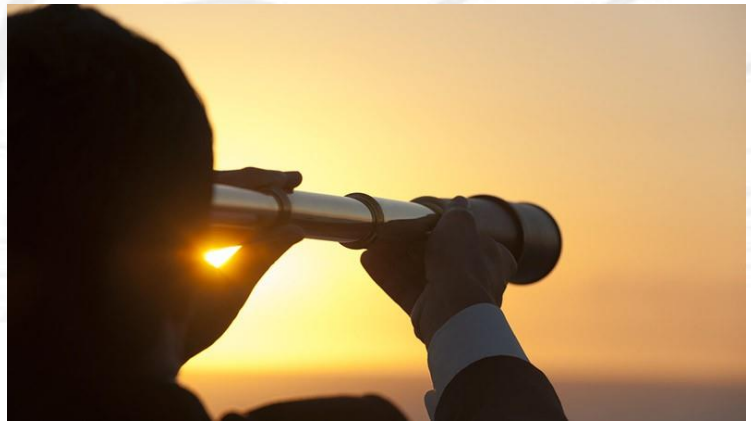
Aptasic solution

Awaited solution



Upgrade bench of unique chip

Conclusion/planning



- Design of new front end board
    - Reduce voltage drop on power supply
    - Change high voltage distribution through the board
    - Add solutions to simplify manipulation and protect wafers

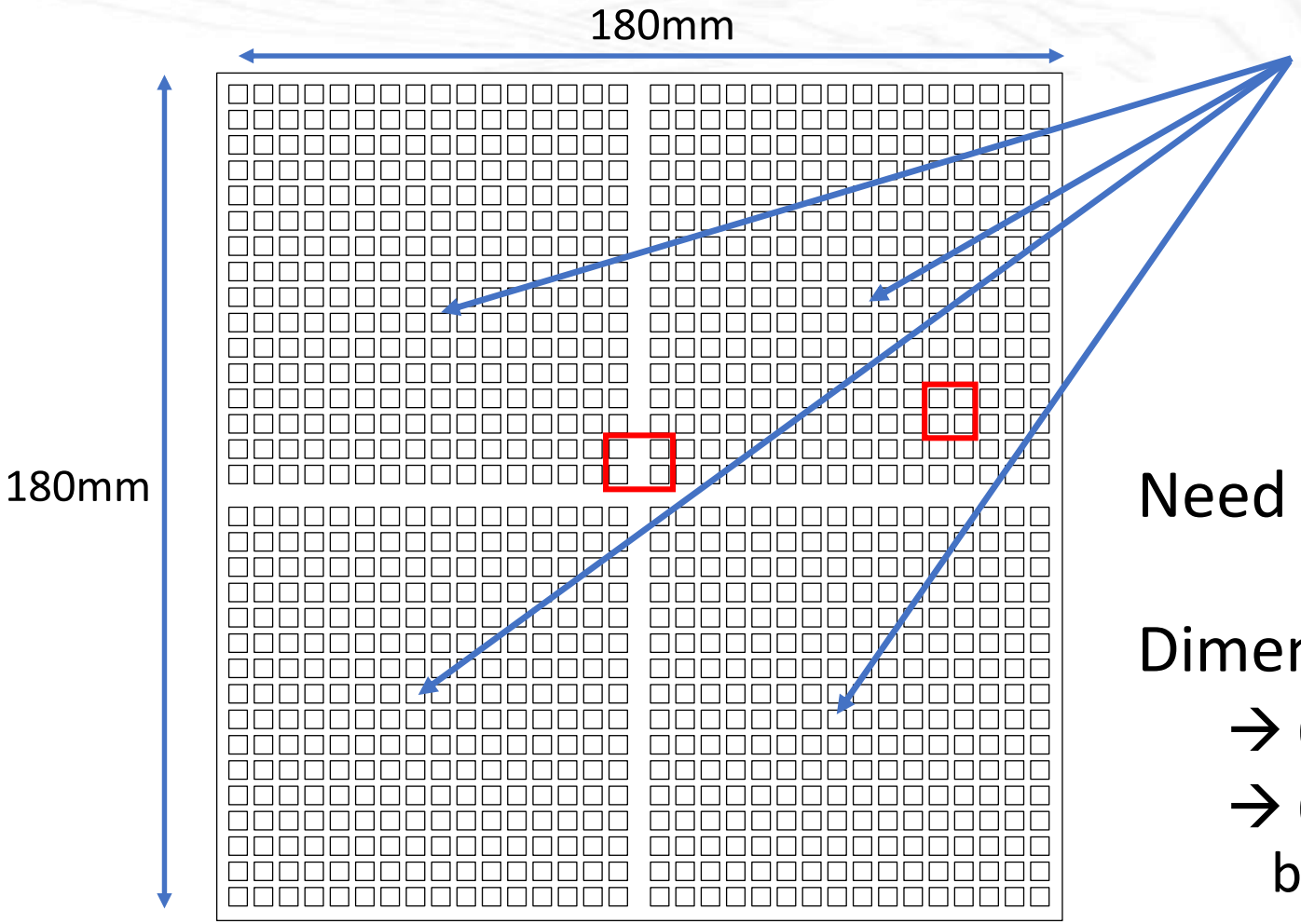
- May: launch packaging of SKIROC2A
- June: production of 15 new front end boards
- September: 1st test + 2021
- 4th quarter: beam test @ DESY (COVID ?)
- 2022: start long slab assembly

→ Be ready in 2023, with new long slab design for ILD schedule

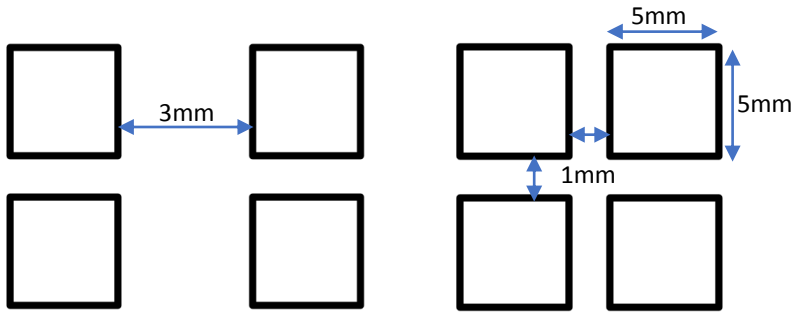

Any
Questions

BACKUP SLIDES

Board synoptic (bottom)



4 matrix 16x16 pixels for 6” wafers



Need high precision to place wafers.

Dimensions of wafers: 89.7mm x 89.7mm

→ 0.1mm gap between wafers

→ 0.25mm gap between wafer and edge of board.

Stack-up board

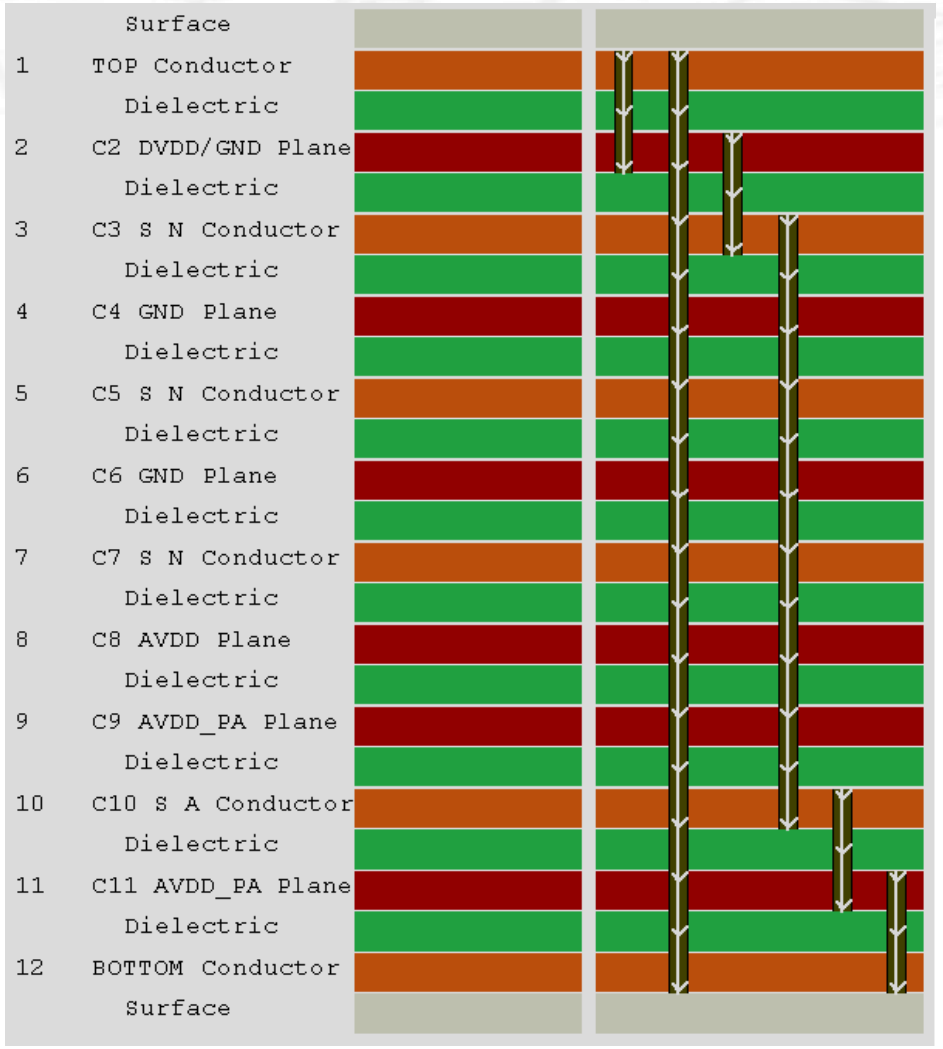
Digital layer for clock 5MHz and 40MHz, differential signals and slow control

Digital layer partition 1

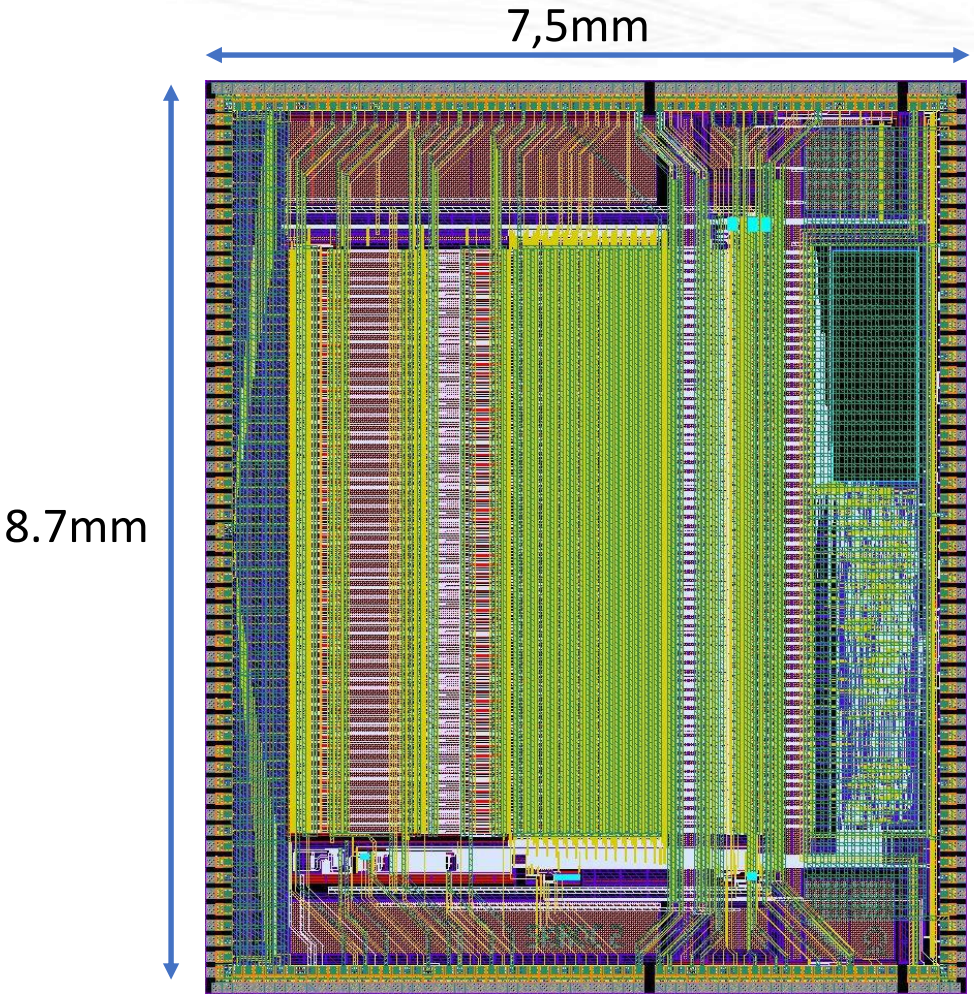
Digital layer partition 2

Analog power layer

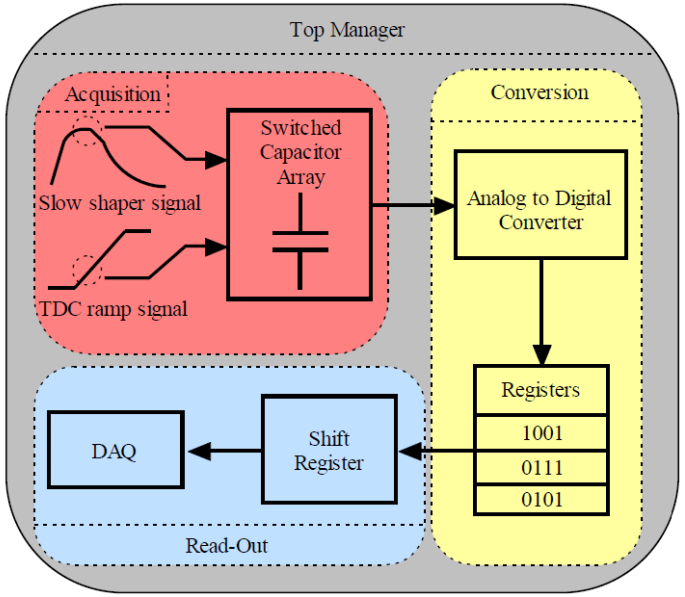
2 AVDD_PA layers to shield signal from Si wafer.

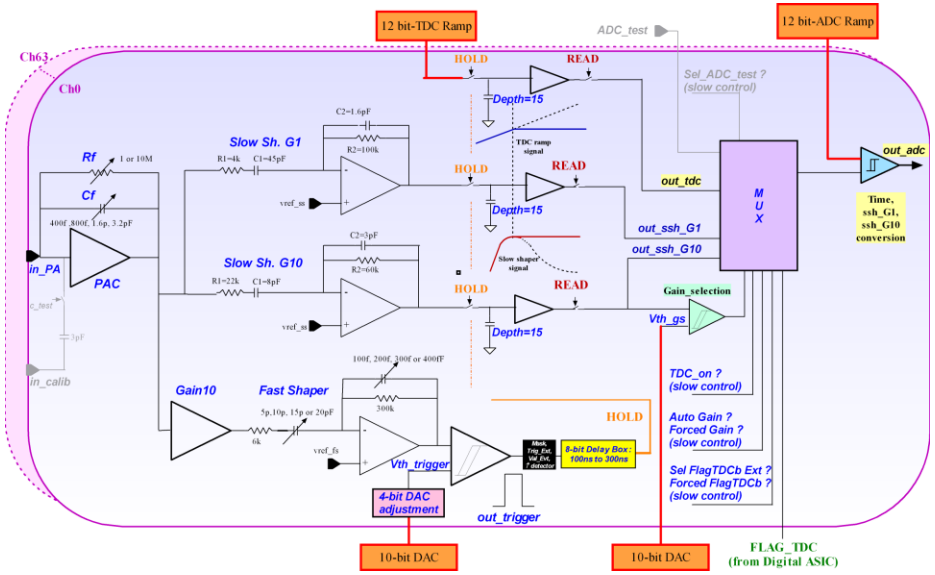


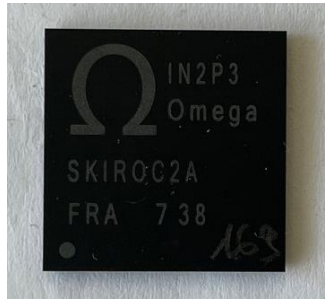
Readout chip Omega SKIROC 2A



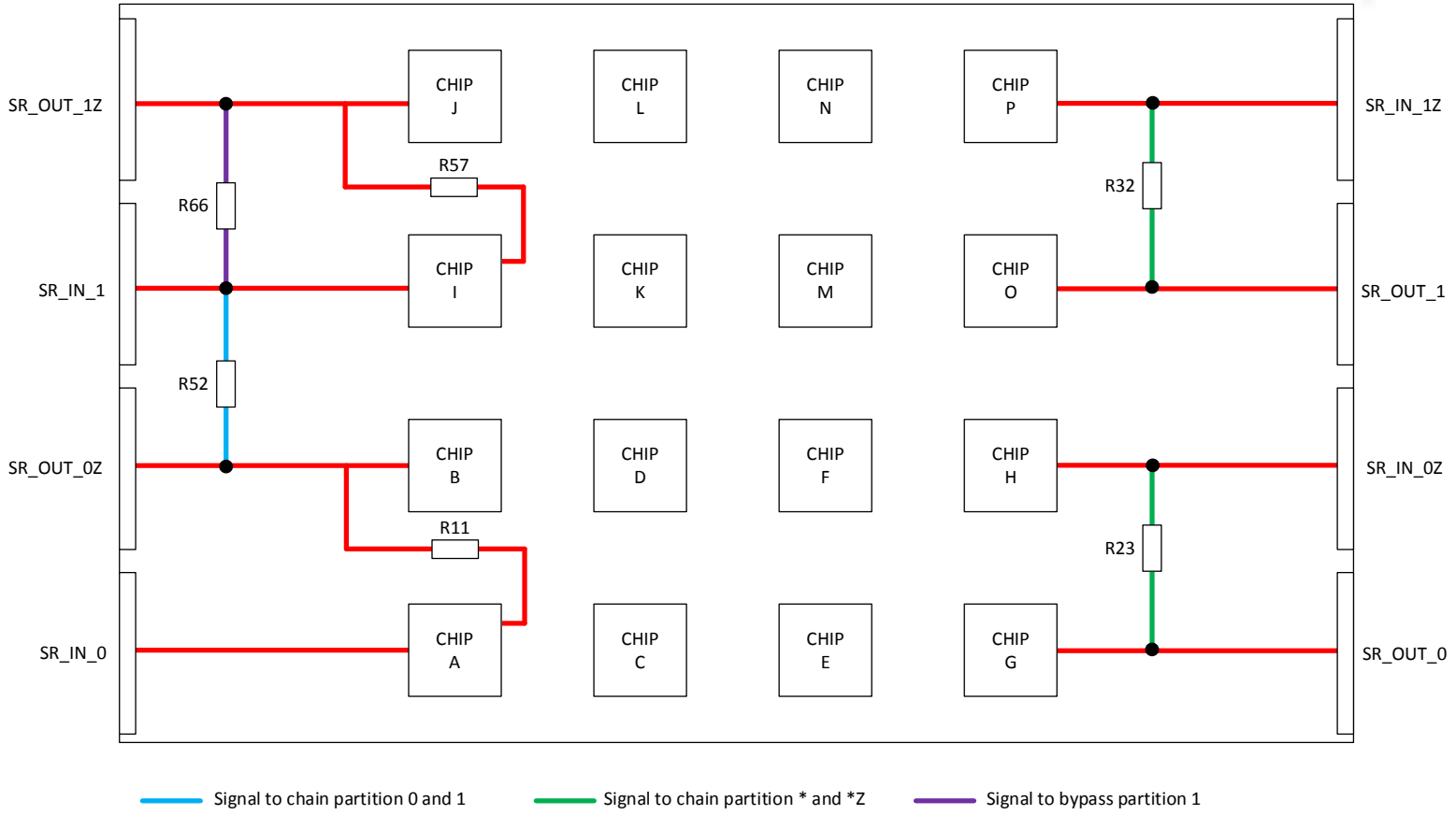
Chip 64 channels
Technology AMS 0,35µm
Large dynamic: 2fC up to 10pC
Very low noise: 0.4fC
Analog memory depth: 15
Full power pulsing







Slowcontrol options



There is some shunt resistor to:

- Chain dummy partition,
- Chain partitions,
- Shunt a complete partition
- Test single readout chip

Planning for 2021

→ 2021:

- → May: launch new packaging for SKIROC2A
- → June : production of new front-end boards
- → September: 1st functional tests
- → 4th quarter: test beam @DESY

→2022:

- → January: start long slab assembly

Planning for 2021

Today March 18

Nom	Date de début	Date de fin
Measure wafers i(V)	04/01/21	15/01/21
Packaging SKIROC 2A by NCAP	12/04/21	02/07/21
FEB conception	02/11/20	19/11/21
Cahier des charges	02/11/20	15/12/20
Schematic	16/12/20	09/02/21
Review schematic	10/02/21	16/02/21
Drawing board	17/02/21	08/06/21
Review drawing	09/06/21	15/06/21
Production of 15 boards	16/06/21	27/07/21
Metrology	28/07/21	03/08/21
Solders componants for 1+4 boards	04/08/21	24/08/21
Fonctionnal tests	25/08/21	22/09/21
Tests with wafers (not glued)	23/09/21	13/10/21
Gluing wafers on 1+4 boards	14/10/21	22/10/21
Calibration + cosmic tests	25/10/21	19/11/21
Beam tests	22/11/21	03/12/21
Solder componants for 5 boards	14/10/21	27/10/21
Gluing wafers on 2 boards	06/12/21	14/12/21
Study mechanical support for long slab	01/03/21	05/11/21
Mechanical production	08/11/21	11/03/22
HV kapton study and production	01/03/21	13/08/21
Long SLAB assembly v2	06/12/21	25/03/22
Assemble 2 boards	06/12/21	06/12/21
Measure & analysis	07/12/21	20/12/21
Assemble 3 boards	21/12/21	21/12/21
Measure & analysis	22/12/21	04/01/22
Assemble 4 boards	05/01/22	05/01/22
Measure & analysis	06/01/22	19/01/22
Assemble 5 boards	20/01/22	20/01/22
Measure & analysis	21/01/22	03/02/22
Assemble 6 boards	04/02/22	04/02/22
Measure & analysis	07/02/22	18/02/22
Assemble 7 boards	21/02/22	21/02/22
Measure & analysis	22/02/22	07/03/22
Assemble 8 boards	08/03/22	08/03/22
Measure & analysis	09/03/22	22/03/22
Calibration / tests / source	06/12/21	25/03/22