CALICE AHCAL

Ongoing hardware developments

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Hardware developments for AHCAL

- Technical protoype built and running since 2018
  - 38 active layers, 72x72cm²
  - 608 Readout ASICs (Spiroc2E - Omega)
  - ~22’000 channels!

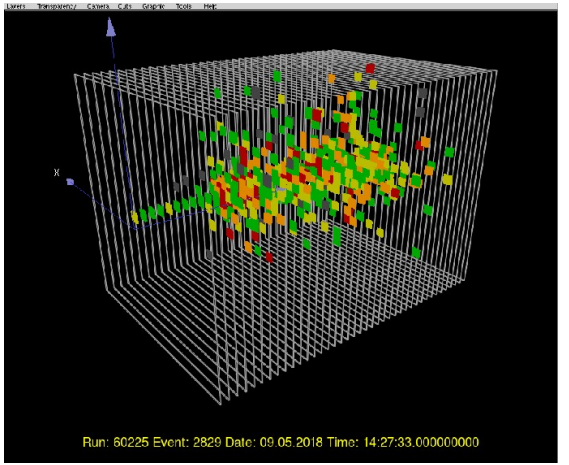
    → Analysis talk L. Emberger on Thursday

- Building the technical prototype

  … already a large fraction of automation

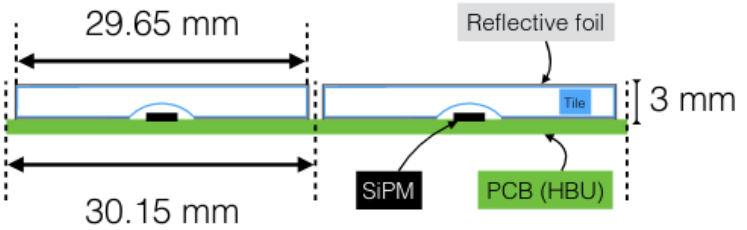
  but a full 8M channel AHCAL needs more!

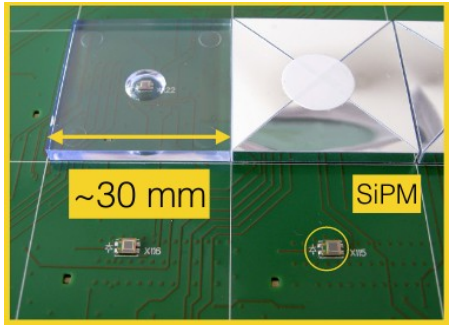
  … ongoing Hardware developments
- Simplification of Module manufacturing & complexity
- Optimized readout ASICs
- Common components within calorimetry systems (ECAL)



AHCAL Scintillator tile design

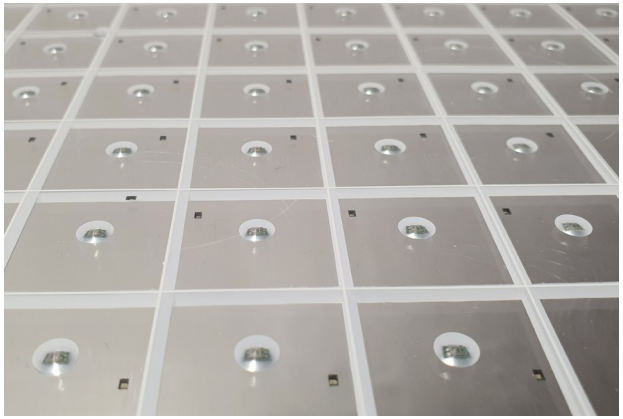
- Surface-mount tile-on-SiPM design
- Baseline design for AHCAL tech. Prototype:
  - Individual production & wrapping of scintillator tiles
    Automatized machine for tile wrapping
  - SiPM sensor & tiles placed on module PCB
    by SMD assembly machines
  - Already great simplification from physics prototype!





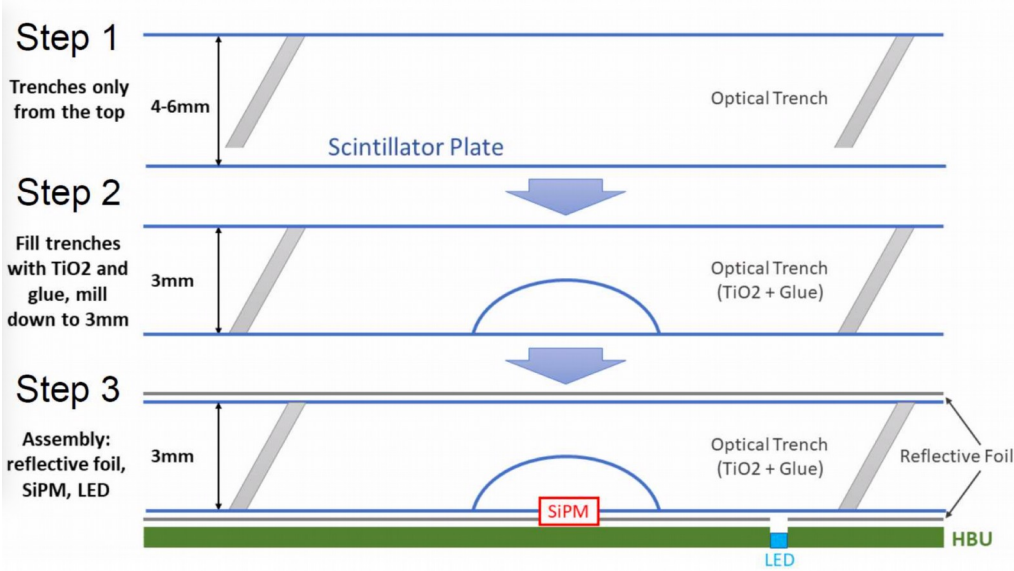
- Full AHCAL has about 8M tiles!
- **Further reduce complexity for mass production**
  - Possible solution: “Megatile” modules
  - One scintillator plate per HBU module (144 channels / tiles)
  - Reduced number of components, Mechanical constraints & Dead area

Megatiles



- Tile matrix from single plate
- Optical isolation by machined & filled Trenches
- Key production steps
  - Mill Trenches from top side
  - Fill with Mixture Epoxy + Ti02
  - Dimple from bottom & Main surfaces

→ Optimize Uniformity, Light yield & Crosstalk



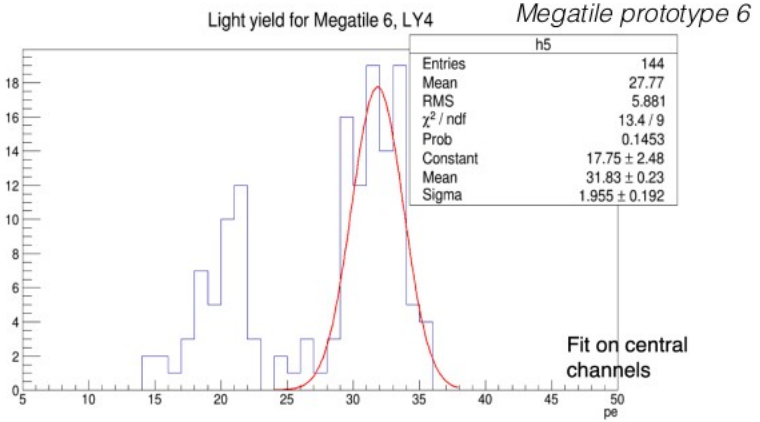
Megatiles - Performance

- Optical performance studied

  Simulations, Cosmics & at DESY test beam
- Design and machining procedures optimized
  - Various designs investigated
  - Trench design & Filling material

- Excellent light yield for central channels
  - Comparable to Individually wrapped Tiles

- More challenging compared to individually wrapped tiles:
  - Optical isolation to neighbors & at edges



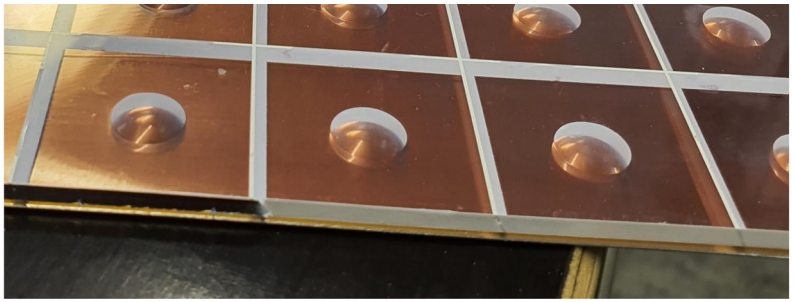
Megatiles - Uniformity

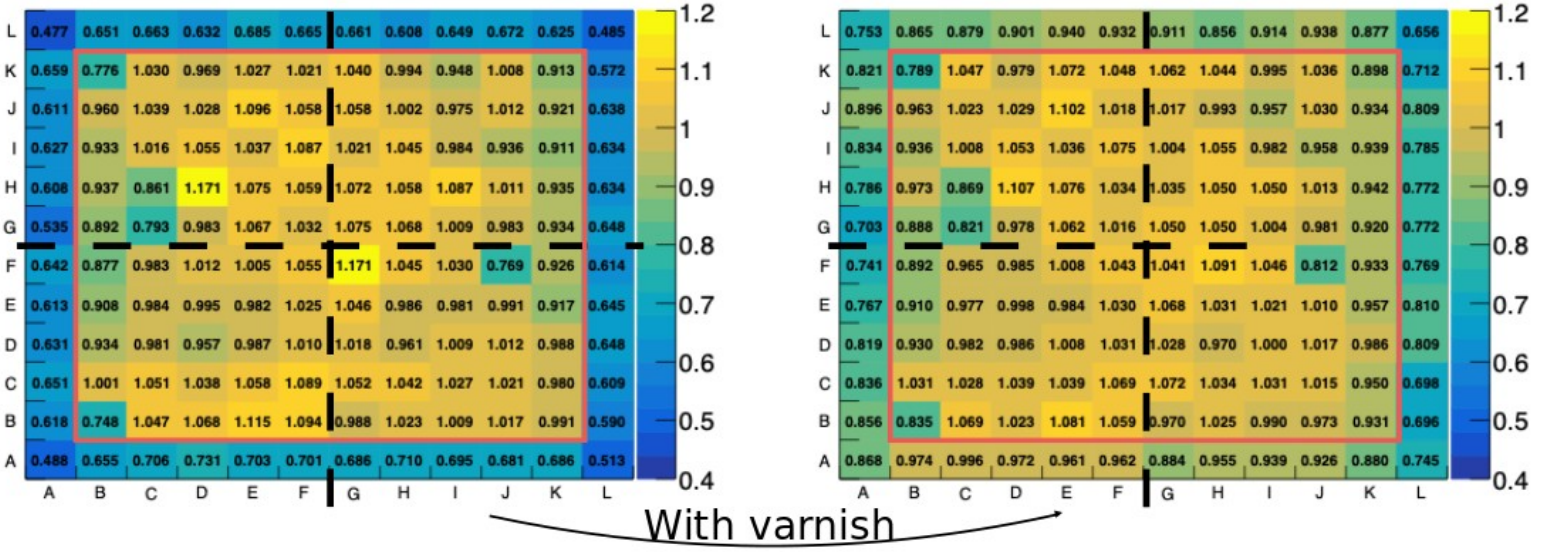
Edge tiles:

- No trench with reflecting TiO2, reduces LY

- Surface treating of tile matrix edges (“spray paint”)

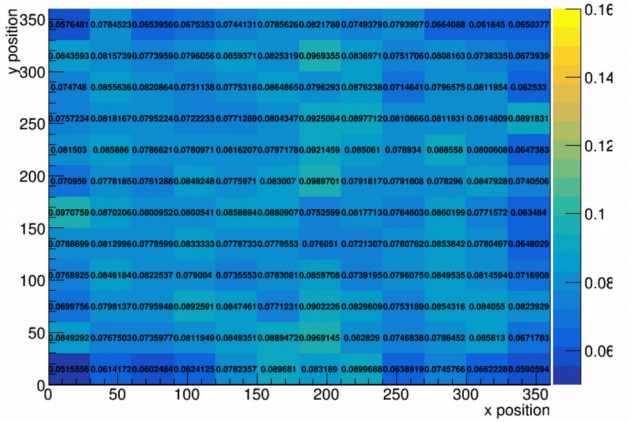
→ Greatly improved Uniformity

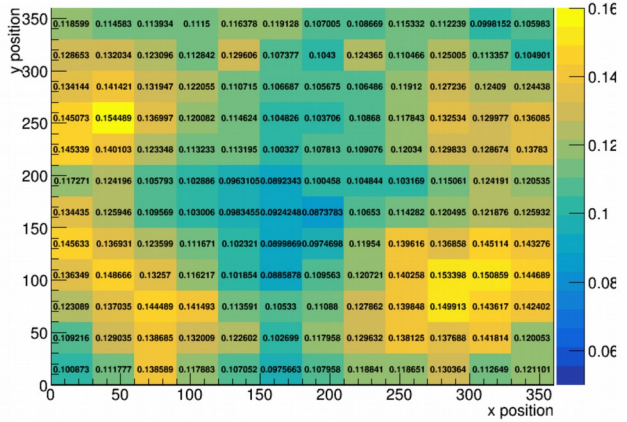


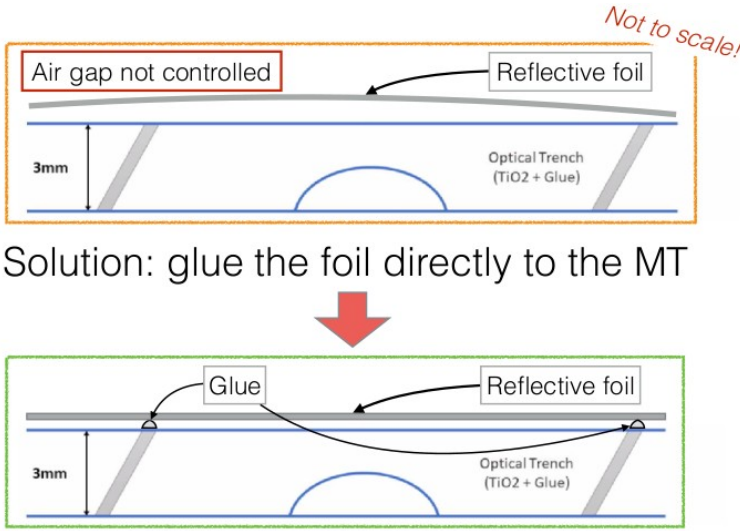


Megatiles - Optical crosstalk

- Optical Crosstalk between channels
  - Higher than AHCAL baseline, but acceptable
- Testbeam results:
  - Higher than expected from cosmics measurements
  - Understood: Caused by uneven Air gap (Scintillator surface – Reflective foil)
  - Flattened in cosmic setup orientation (additional weight)
  - New study in beam pending (delayed due to pandemic)



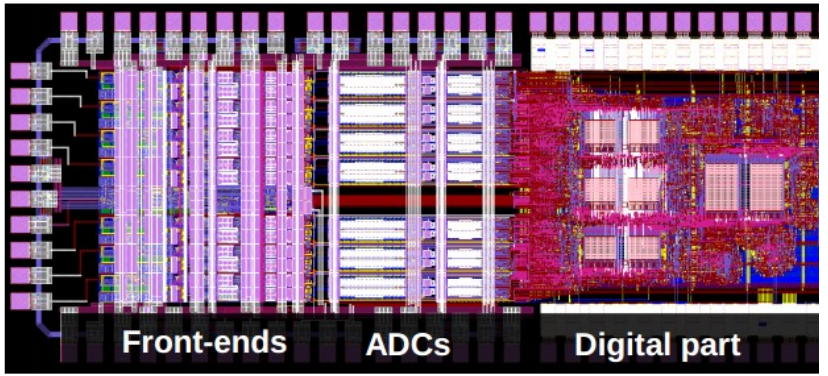




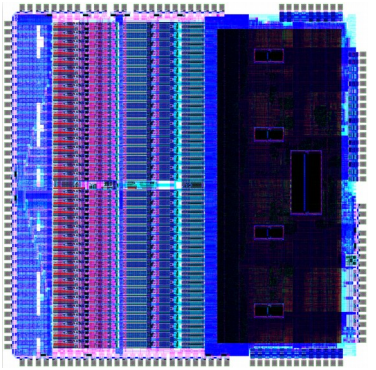
Alternative readout ASIC - KLauS

- AHCAL requires a highly **specialized readout ASIC**
  - Low noise charge measurement
  - Time measurement (~1ns requirement)
  - Low power, Power pulsing capable
    (~25uW @ 0.5% duty cycle)

7-channel KLauS4 prototype (2016)

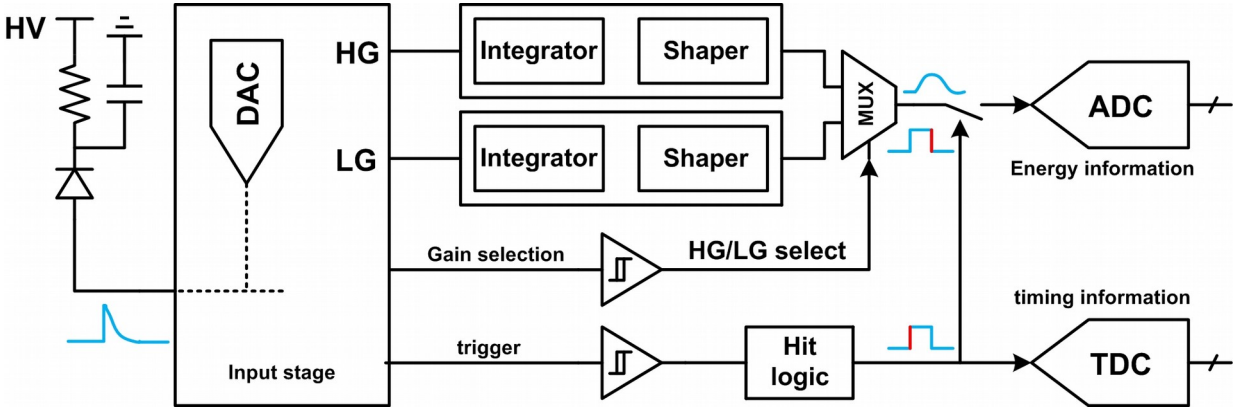


- **KlauS ASIC** developed at Heidelberg University
- **Target low gain SiPMs** (10µm pixel, ~1mm² area. Charge range 15fC – 150pC)
- SiPM readout solution for CALICE AHCAL & ScECAL
- KLauS6 with 36 channels – Development close to final
- Analog front-end + ADC + TDC + Digital circuits
- Versatile ASIC for different beam (time)-structures & Sensors



KLauS6 (5x5 mm²)

KLauS Channel



- Input stage → Buffer & distribute signal current, SiPM bias voltage tuning (~2V range)
- 2 charge measurement branches → Calibration & full SiPM dynamic range
- 2 comparators blocks → Timestamp & ADC start, charge range selection (auto-gain)
- Integrated per-channel SAR ADC for charge measurement
- PLL based TDC for time stamp recording
  - In KLauS6: ~195ps bins , ~3.3ms dynamic range (@nominal 40MHz clock input)
- Allows very flexible run conditions

  – no analog memories, no separate digitization and readout phases required → Continuous running

KlauS ASIC - Charge measurement

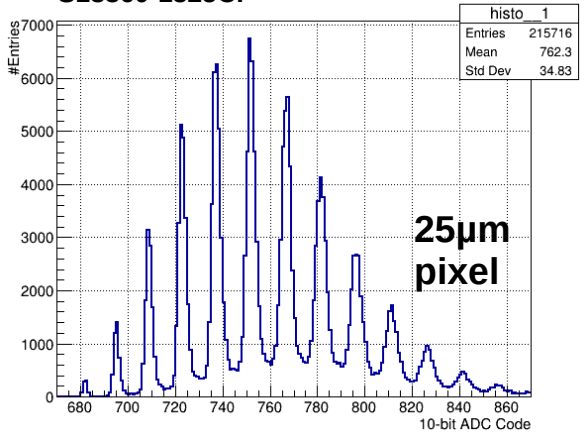
SPS with different MPPCs

- Spectra recorded in self-triggered mode
- Pulsed LED
- Nominal SiPM bias
- No problem to operate with 3x3mm² SiPMs or larger pixels

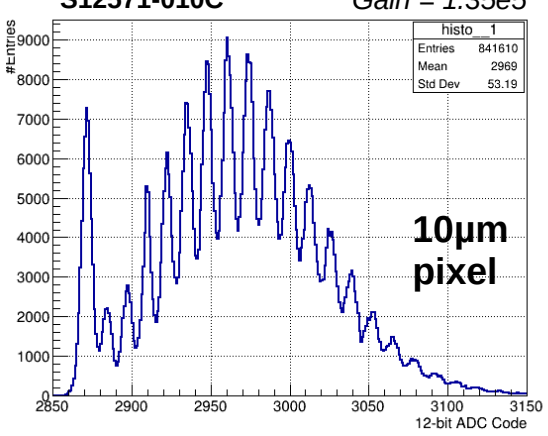
Charge spectra with electrons @ DESY

- AHCAL standard tile (30x30x3 mm³)
- Self triggered operation
- Automatic range selection enabled

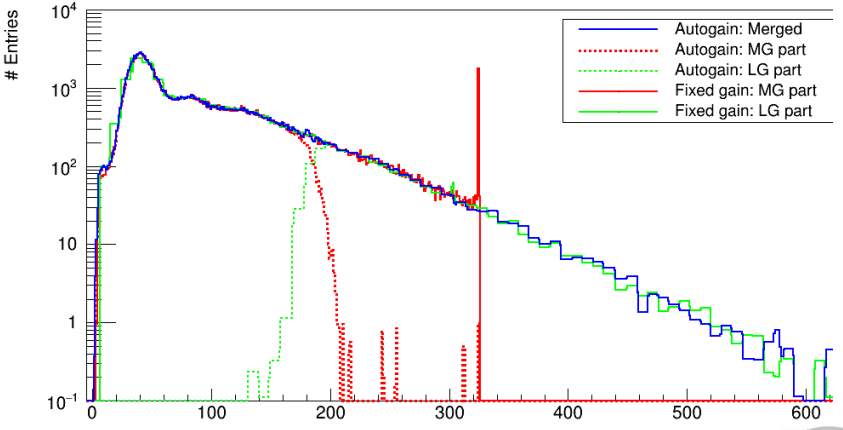
Hamamatsu S13360-1325CP



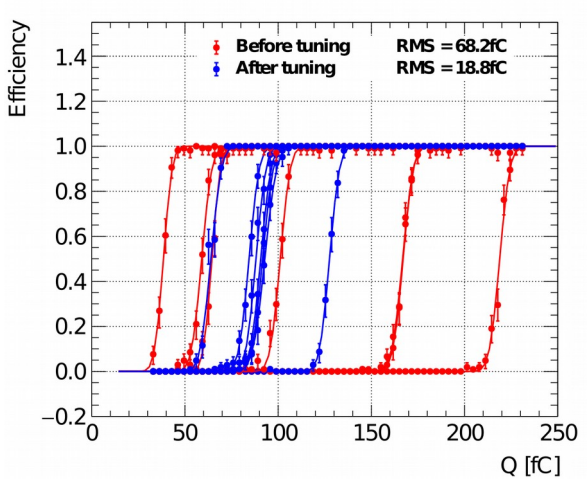
Hamamatsu S12571-010C *Gain = 1.35e5*

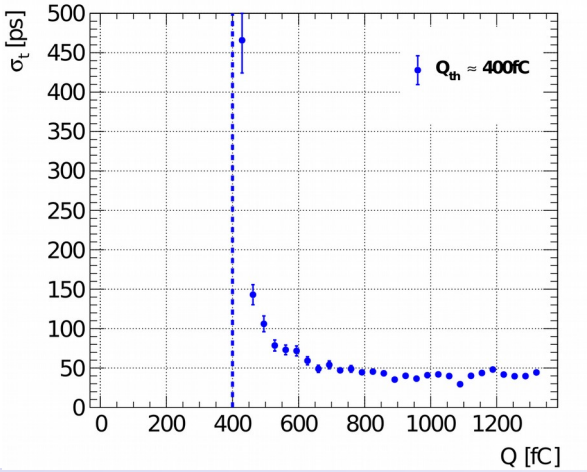


Electrons at DESY: Auto-gain mode & Individual contributions



KlauS ASIC - Hit timestamps





Comparator:
Leading edge current discrimination
Used for **Time-stamp & hold** for ADC peak sampling

Two DACs to adjust **threshold**:
- Global 6 bit DAC: … Coarse setting
- 5 bit DAC per channel: … Fine-tuning

Electronic **jitter**
- Measured with oscilloscope
- At 400fC threshold: approaching σ < 50 ps
- Contributions from KLauS TDC binning ~60ps

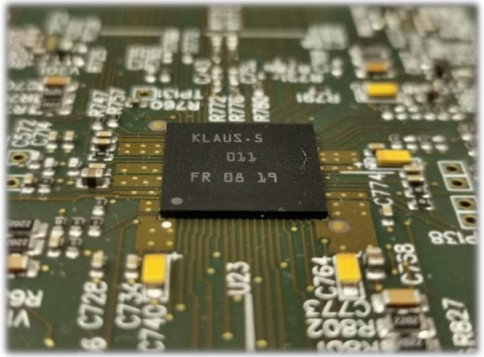
Main “real” contribution is photon statistics

- Design goal (< 1ns) verified in first Testbeam campaign

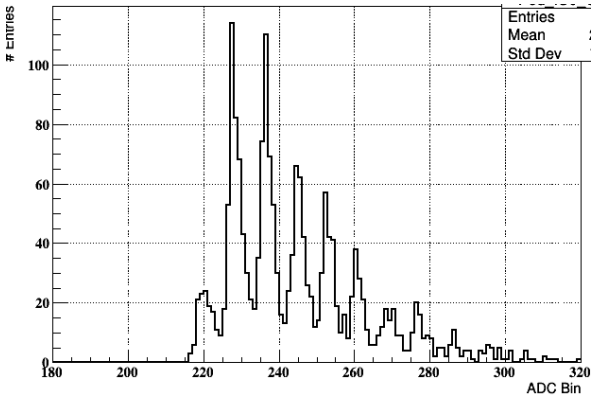
- Plan to study timing in detail with full modules, megatiles, ...

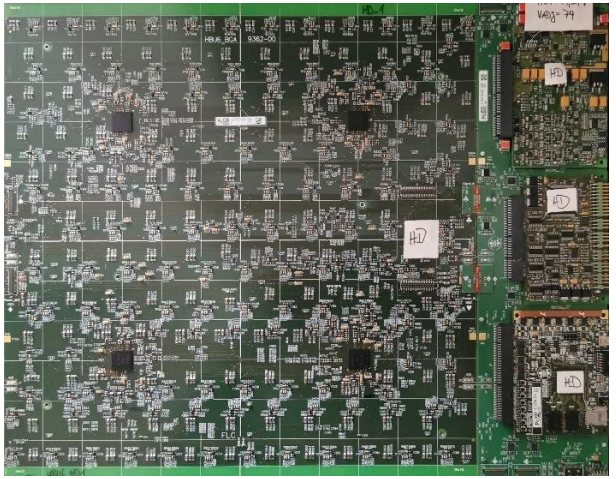
HBU with KlauS ASIC

- KlauS in BGA package is available
- Allows integration in HCAL Base Unit (HBU)
  - Base AHCAL module PCB
  - 4 readout ASICs, 144 channels
  - KlauS variant of HBU developed by DESY + HD
  - DAQ & Software adopted for single-board operation



- HBU-K DAQ development and testing in progress
  - Basic functionality shown
  - Integration to full CALICE DAQ in progress





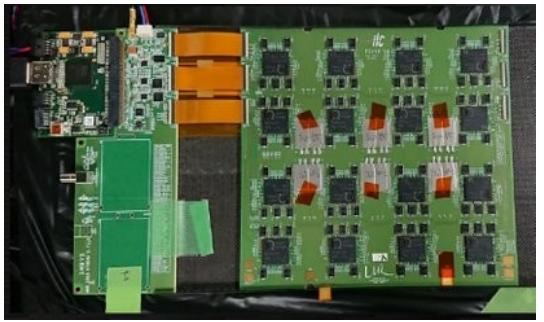
- Test beam campaigns at DESY
  - Common running with multiple layers
  - Planned for April
  - Later this year: timing with HBU & KLauS6

Development of common interfaces

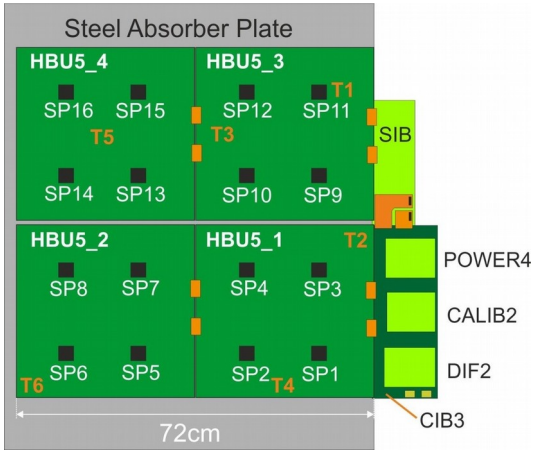
Plan to streamline CALICE detector components

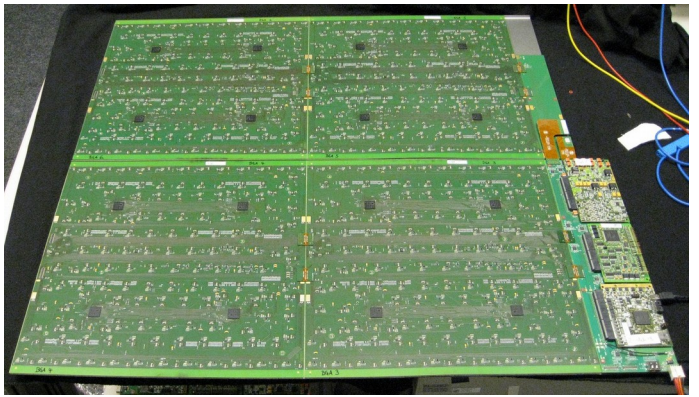
- Detector cooling
- DAQ interface cards & Data concentrators
  - Adapt to SiW-ECAL cards
- Common ground and partially specifications, but…
- Different conditions & additional requirements
  - AHCAL: LED system for calibration
  - Layer sizes
    → Signal distribution
  - Channel density
    → Cooling solution

ECAL cards with ASU



AHCAL DAQ cards in tech. prototype





Summary

- AHCAL is a proven technology
  - Hardware development can build on working prototype detectors
  - A “full AHCAL” still not out of the box

- Emphasis on
  - Simplification of manufacturing
  - Generalization of readout electronics
  - Streamlining of common detector components within CALICE