The Semi-Digital Hadronic Calorimeter (SDHCAL)

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On behalf of the CALICE Collaboration

CIEMAT

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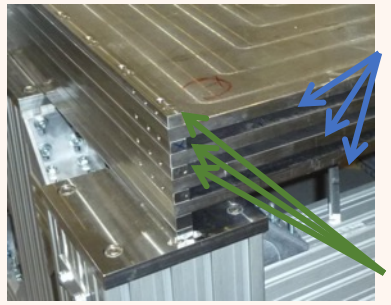
SDHCAL – Main characteristics

Sampling calorimeter: ***Absorber: Stainless Steel + Detector: Glass Resistive plate Chambers***

Absorber: **Stainless steel**

Absorber **plates up to ~3x1 m²** .
Surface **planarity < 1mm** ,
Thickness 15mm, tolerance **50µm**

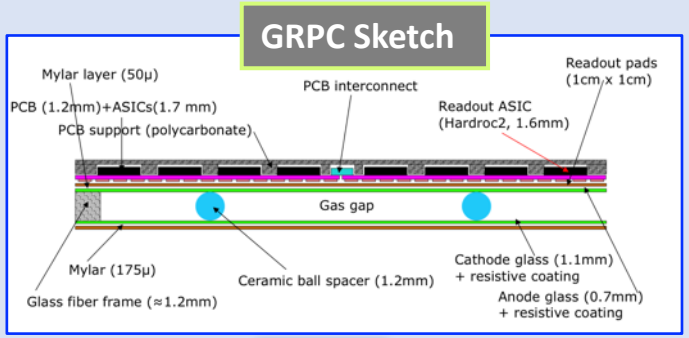


Plates (15mm) assembled together by using an intermediate **spacer** insuring the place for introducing the detectors

Detail after assembly the **first 4 absorber plates of a 1.3m³ prototype (plates ~1x1m²)**

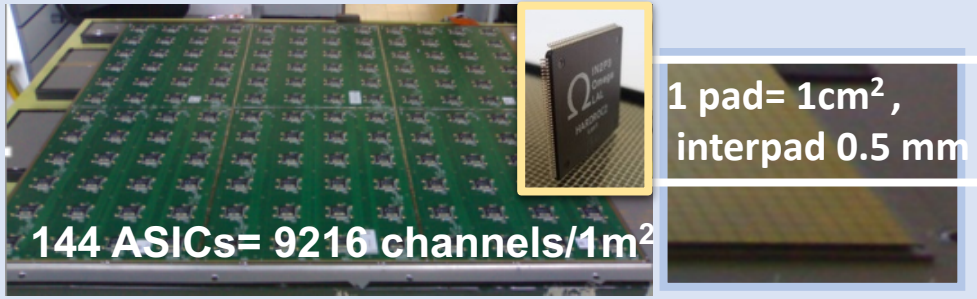
Detector: **GRPC (Glass Resistive Plate Chambers)** operating in **avalanche mode**

1x1 cm² pads. Semi-Digital Readout, 2bits **- 3 thresholds**
➔ It counts **how many** and **which pads** have a **signal larger than one of the 3 thresholds**



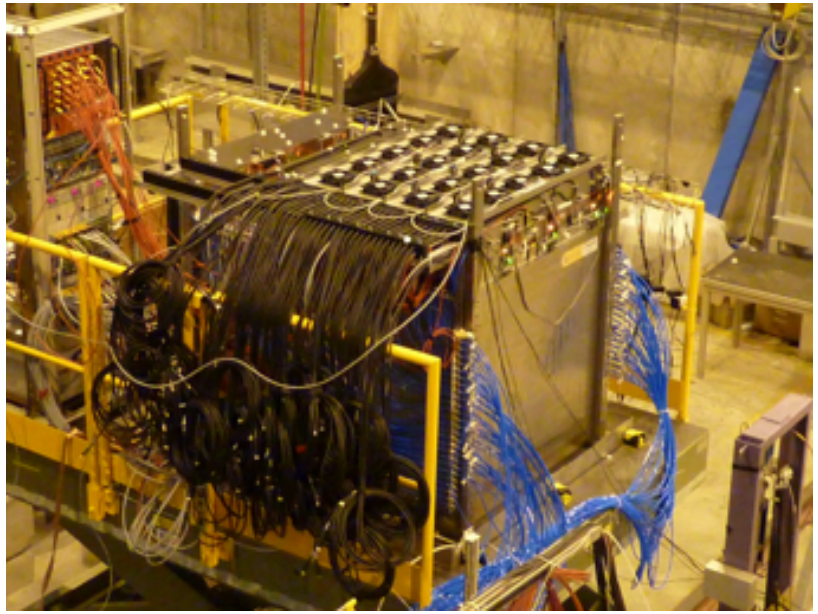
Embedded electronics:
PCB separated from the GRPC by a mylar layer (50µm).
➔ Bottom: **1x1cm2 pads**
➔ Top: **HARDROC** (**HA**dronic **R**pc **R**ead**O**ut **C**hip) & related connections

Power-pulsed electronics: In **stand-by during dead time** in between ILC Collisions or spills in beam tests

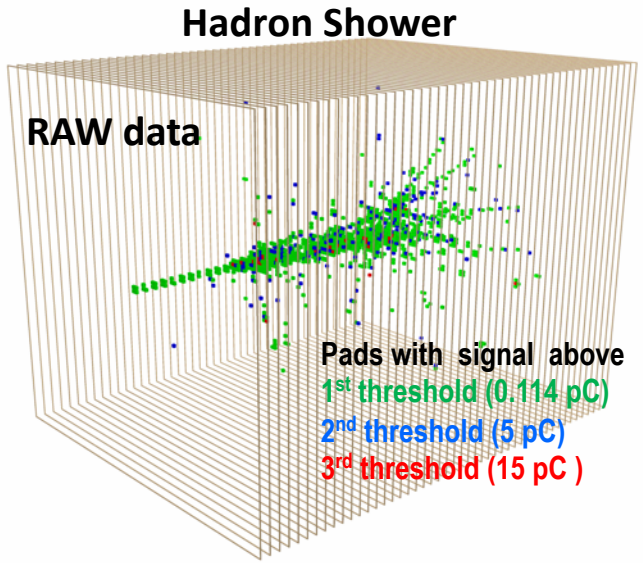


1m3 SDHCAL Prototype

SDHCAL ~1.3m^3 prototype
At Test Beam @ CERN



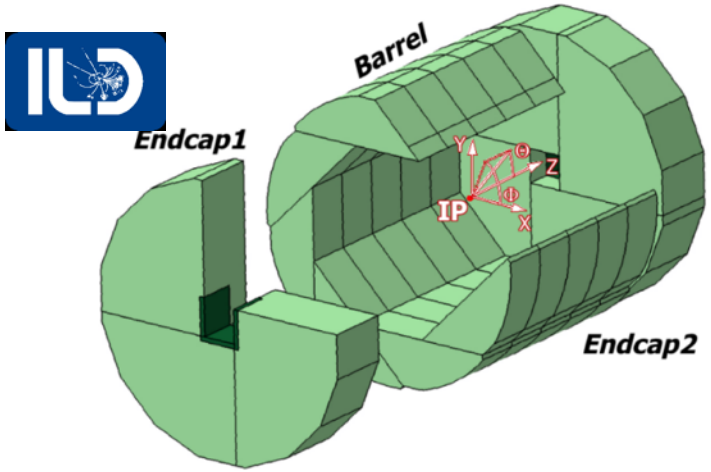
~ half million channels!!
(More than in the full calorimeter systems of the LHC experiments)

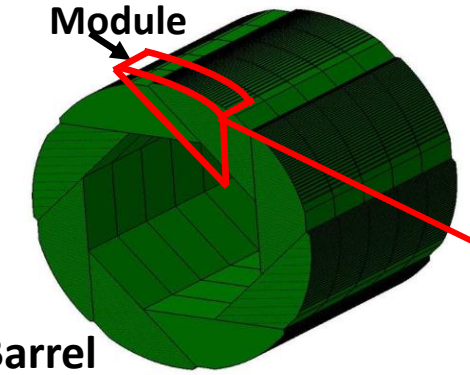


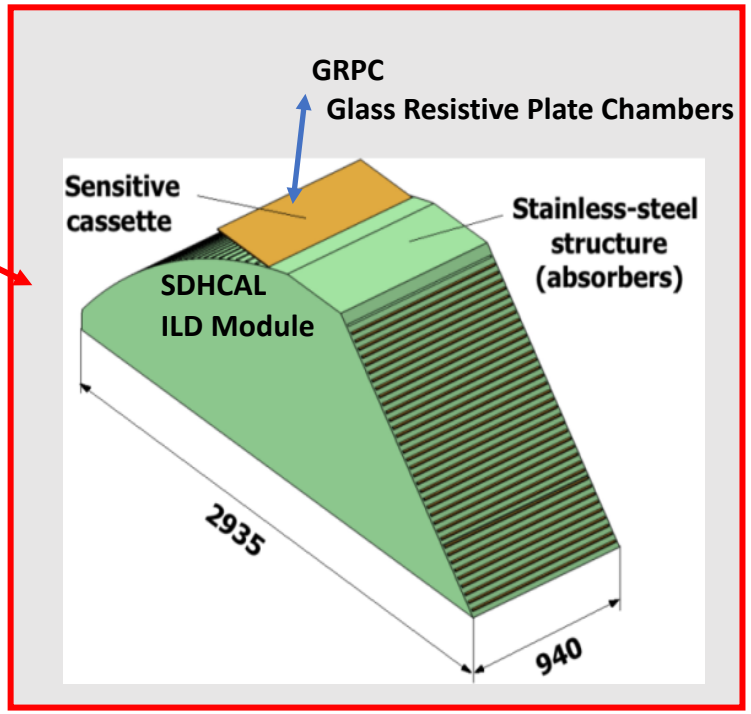
Excellent detailed view of shower development

See performance studies at Hector Garcia Cabrera's Talk at this conference: PD4/PD6 session on Thursday

The new SDHCAL prototype







The ~1m3 prototype built in the past was based on layers of plates absorbers of ~1m2

To enlarge them to the maximum size (~3x1m2) expected at ILD, implies new challenges for the detector, embedded electronics and mechanics

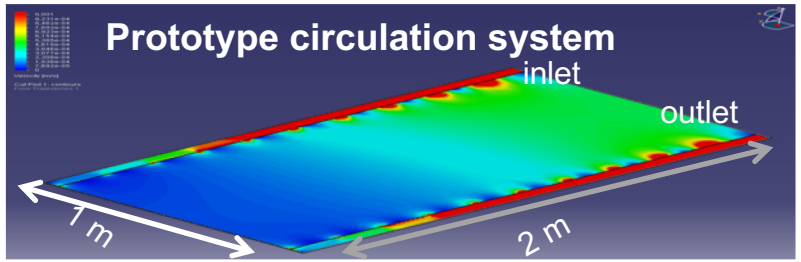
The goal

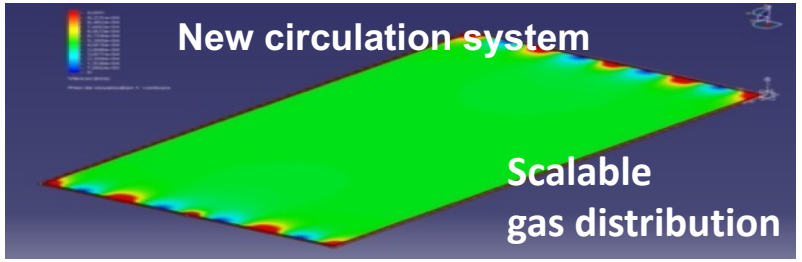
To build a ***new prototype*** ***with a mechanical structure of 4 plates of ~1x3m²*** (assembled with similar procedures to the final one) where inserting large ***RPCs equipped with a new improved electronics.***

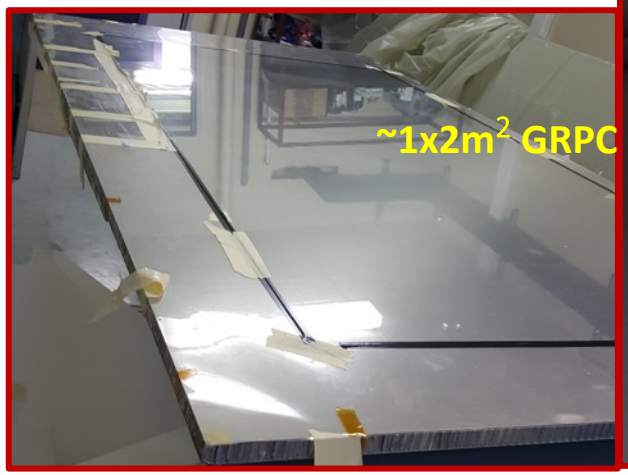
New chambers: Large GRPCs

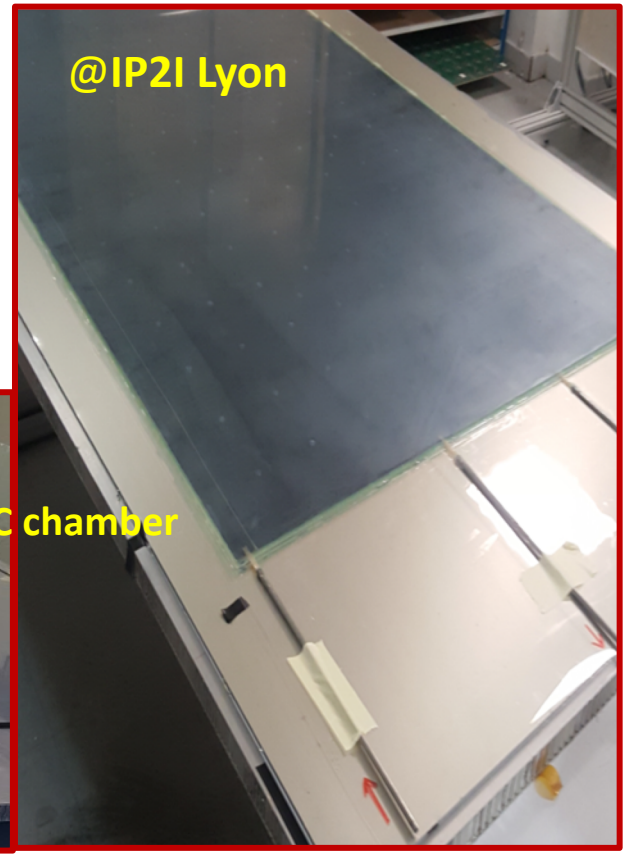
Construction and operation of large GRPC needs some improvements with respect to the $1m^2$ used at the $1m^3$ SDHCAL prototype.

Gas distribution

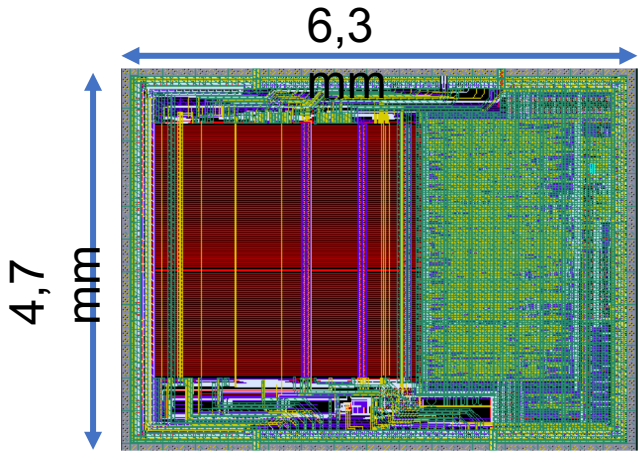








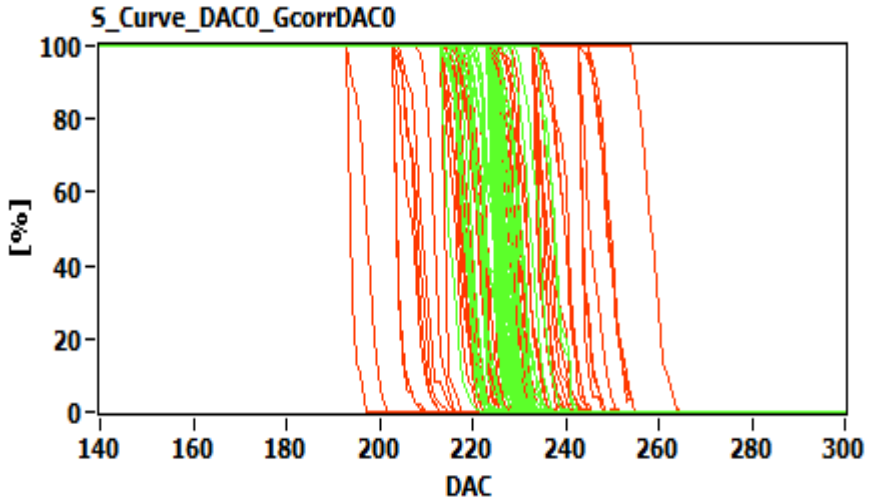
New Electronics: ASIC – HARDROC3

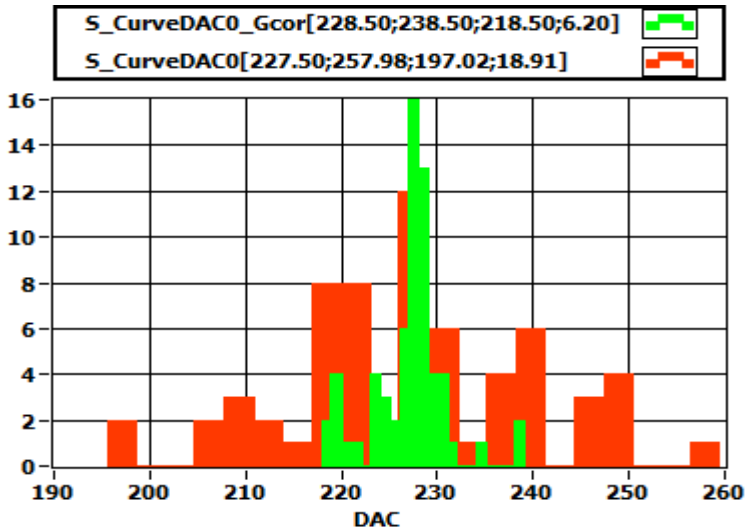


HARDROC3 (HR3) main features:

- **Independent channels**
- **Zero suppress**
- Extended dynamic range (**15 fC up to 50 pC**)
- **I2C link with triple voting for slow control parameters**
- packaging in QFP208, die size ~30 mm^2
- Consumption increase (internal PLL, I2C)

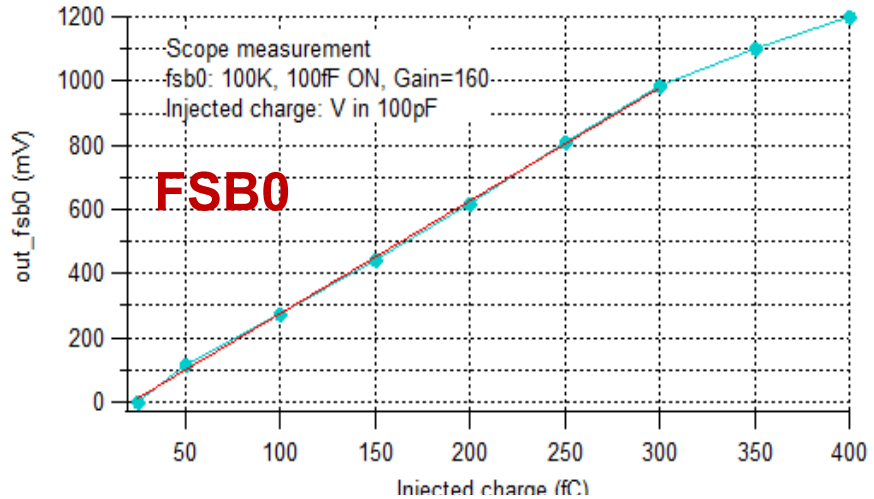
H3R TESTED : 786

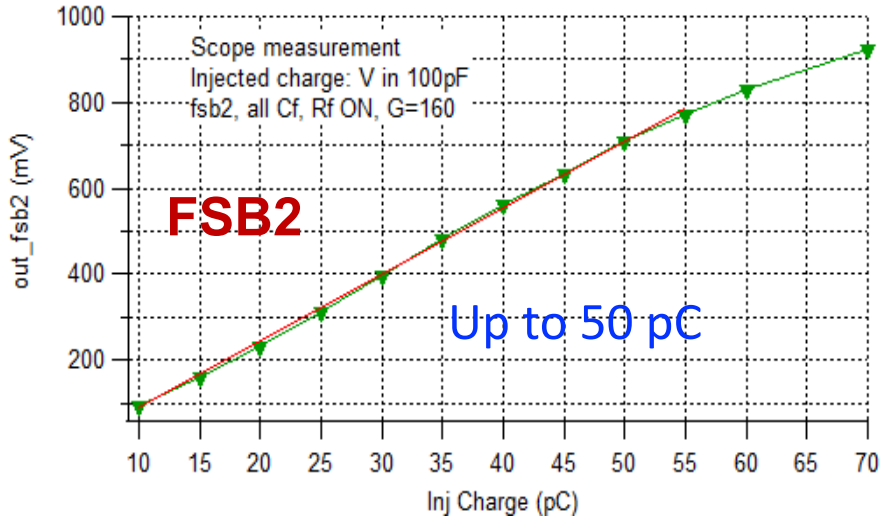


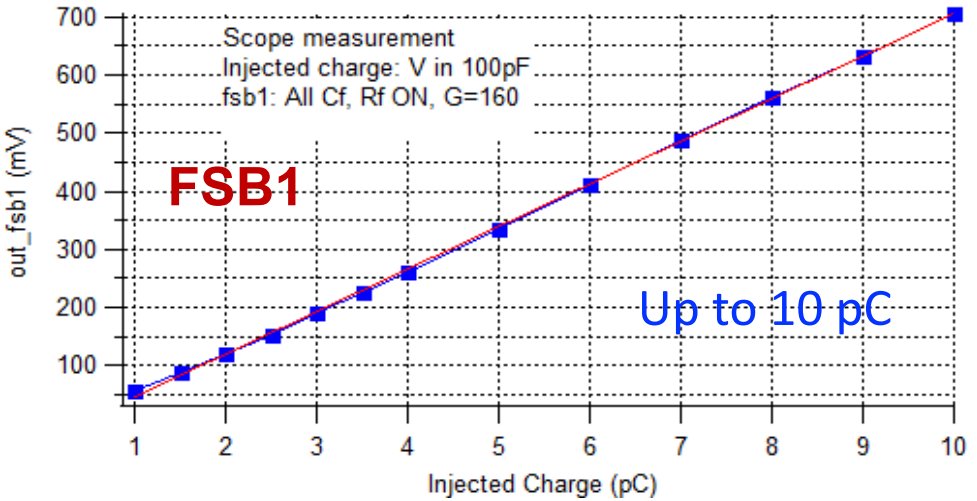


Distributions **before** and **after** equalization

New Electronics: HARDROC3 - Linearity







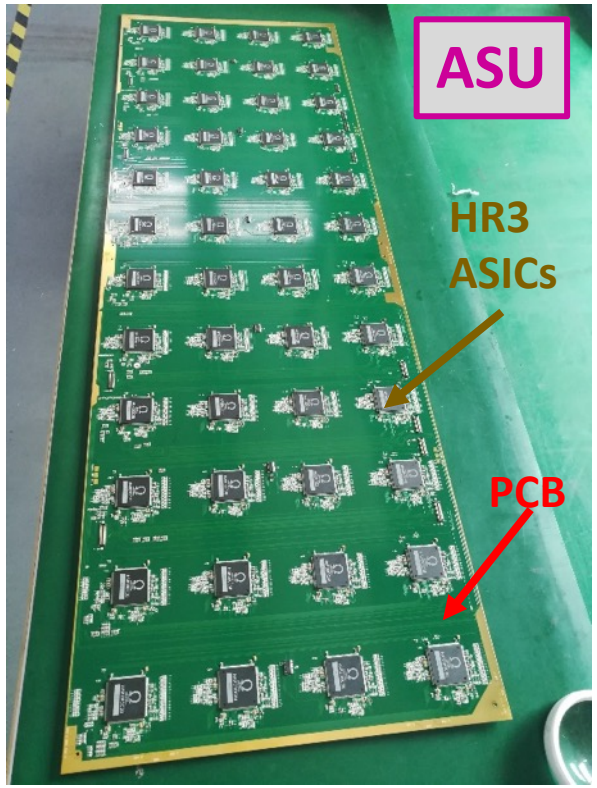
Fast shaper outputs (mV) vs Qinj (fC)

Dynamic range: 15fC - 50 pC

New Electronics: Active Sensor Unit (ASU)

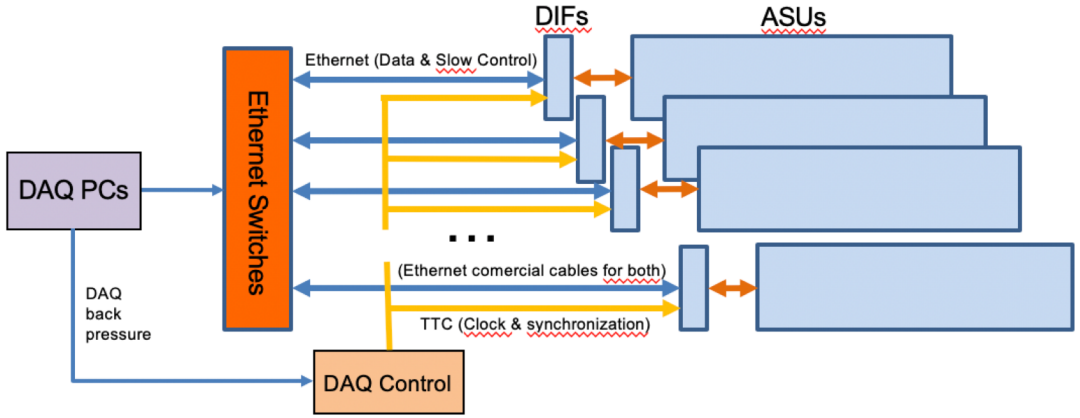
An important challenge is to build a PCB up to 1m length with good planarity to have a homogeneous contact of pads with RPCs in order to guarantee an uniform response along all the detector.

A company was found and ***1x0.33 m2 with 13 layer ASUs*** have been built.



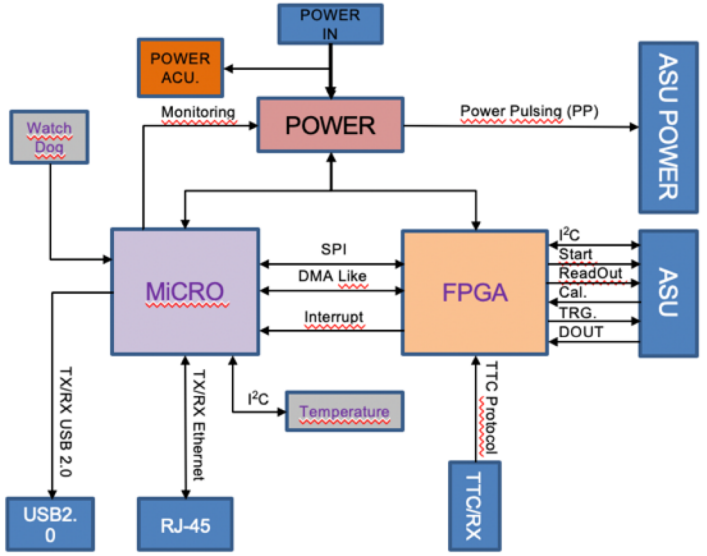
SDHCAL DAQ architecture

A ***central PC*** **collects data** from all the ***ASUs*** (containing de ***ASIC chips***) through an ***Ethernet switch*** acting in such a way **as data concentrator** and **generates the required commands for *ASU* and *DIF (Detector Interface)* configuration generating at the same time synchronization signal** required for a correct data acquisition process.

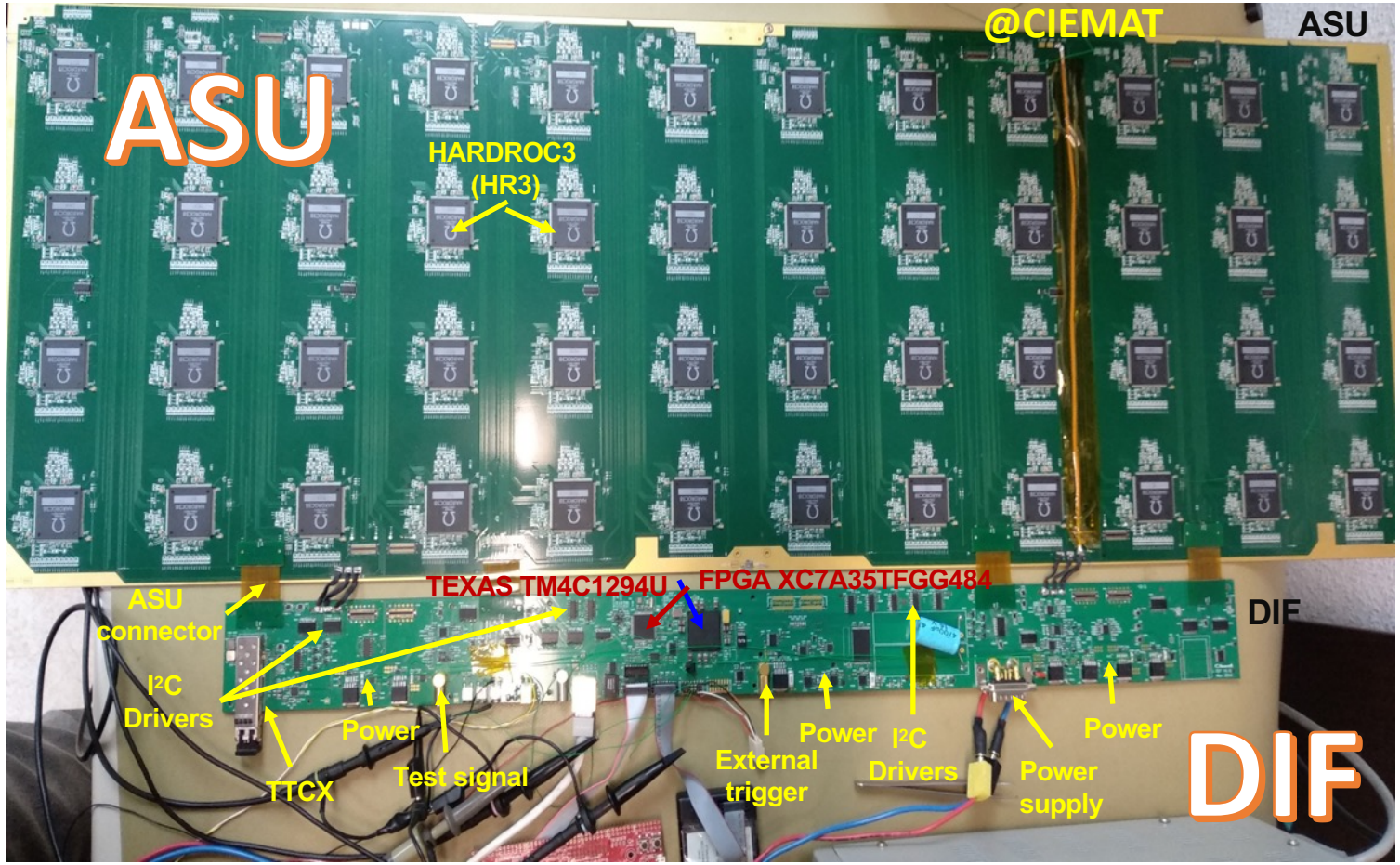


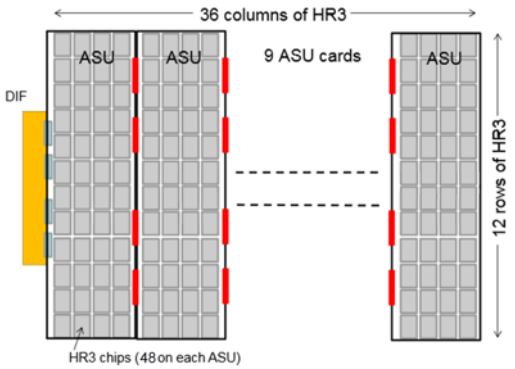
DIF architecture

- Only **one DIF per plane** (instead of **three** at 1m3 prototype)
- DIF handle up to **432 HR3 chips** (vs **48 HR2** in previous DIF)
- **Clock and synchronization** by **TTC** (already used in LHC)
- **93W Peak power supply** with super-capacitors (vs **8.6 W** in previous DIF)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- Upgrade **USB 1.1** to **USB 2.0**

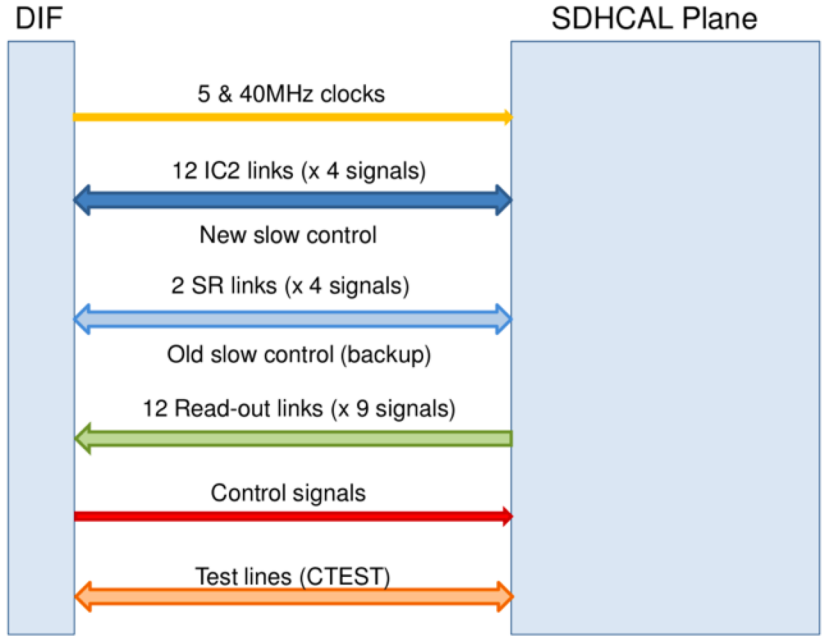


New Electronics: Detector InterFace





Number of ASUs scalable with GRPC length



Total 216 lines + Power

DIF size driven by the available space expected at ILD detector
In future it could be integrated in the ASU

Several DIF boards built and tested at Lab. Integration with DAQ ongoing

New mechanical absorber structure: Plates and Spacers

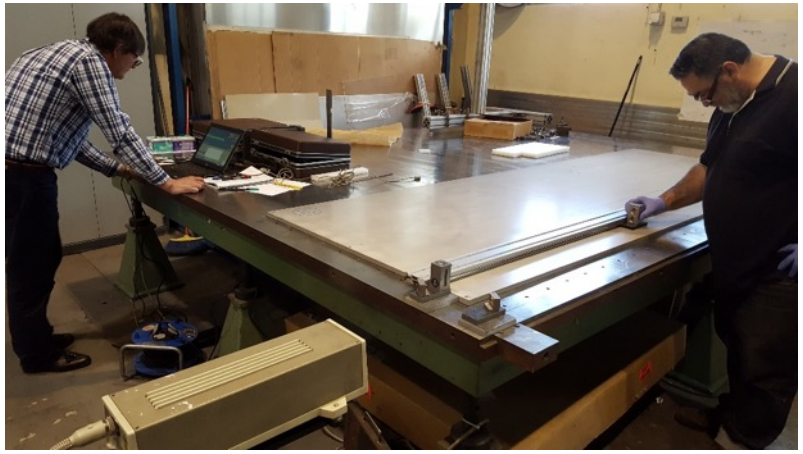
Spacers machined at the CIEMAT workshop

PLATES

At the market the best flatness available is of several mm
For the first 1 m^2 plates prototype the required plate flatness(<1mm) has been obtained **by machining the plates** but this **process is very time consuming and expensive** for the final production.
Roller leveling was envisaged as the solution

www.arku.de/

Final quality test
Performed using **laser interferometry**
(over a special table (flatness 150 micron))



Planarity

Planarity (µm)	Plate A		Plate B		Plate C	
	Side 1 up	Side 2 up	Side 1 up	Side 2 up	Side 1 up	Side 2 up
Average	469,3	852,6	511,6	596,3	983,4	1038,0

Plate D		Plate E	
Side 1 up	Side 2 up	Side 1 up	Side 2 up
458,7	546,1	610,2	521,9

Thickness

Thickness (mm)	Plate A	Plate B	Plate C	Plate D	Plate E
average	15,256	15,259	15,282	15,247	15,279
max.	15,352	15,340	15,348	15,342	15,350
min.	15,157	15,161	15,216	15,147	15,201
Δ	0,195	0,179	0,132	0,195	0,149

Initial planarity between 1 and 3mm
Final planarity inside the required tolerances

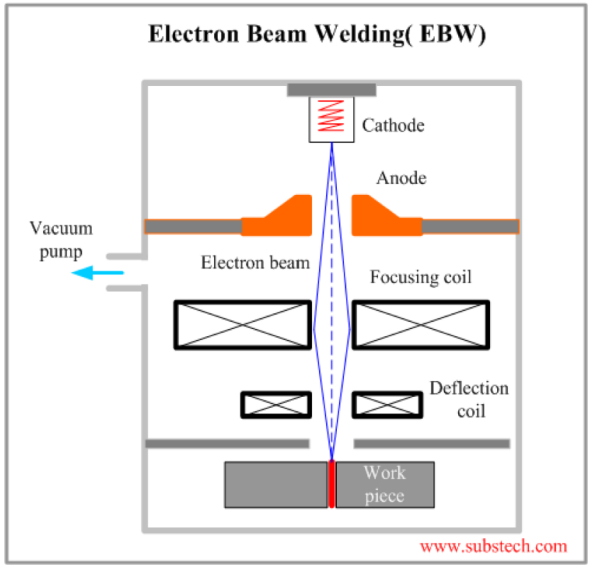
New mechanical absorber structure: EBW

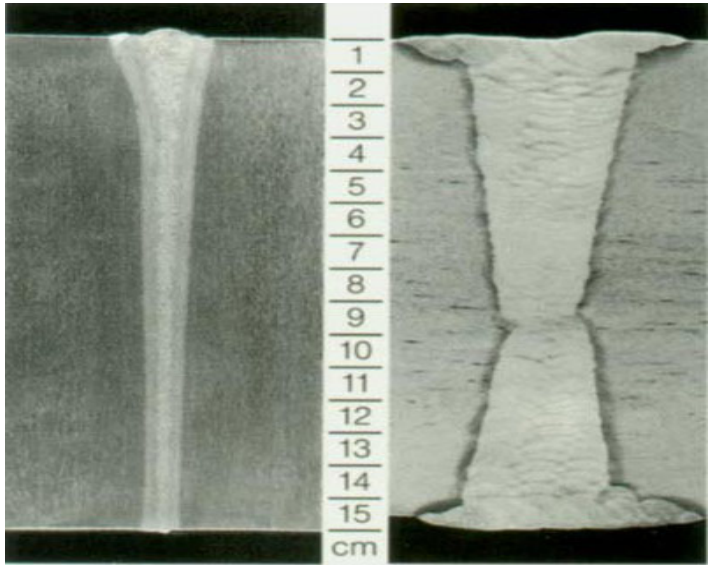
The mechanical structure for 1m3 prototype was assembled using bolts

Larger (heavier) structure
➔ Bigger bolts, **larger dead spaces**, option: Welding

Standard Welding
➔ Heating introduces **deformations**

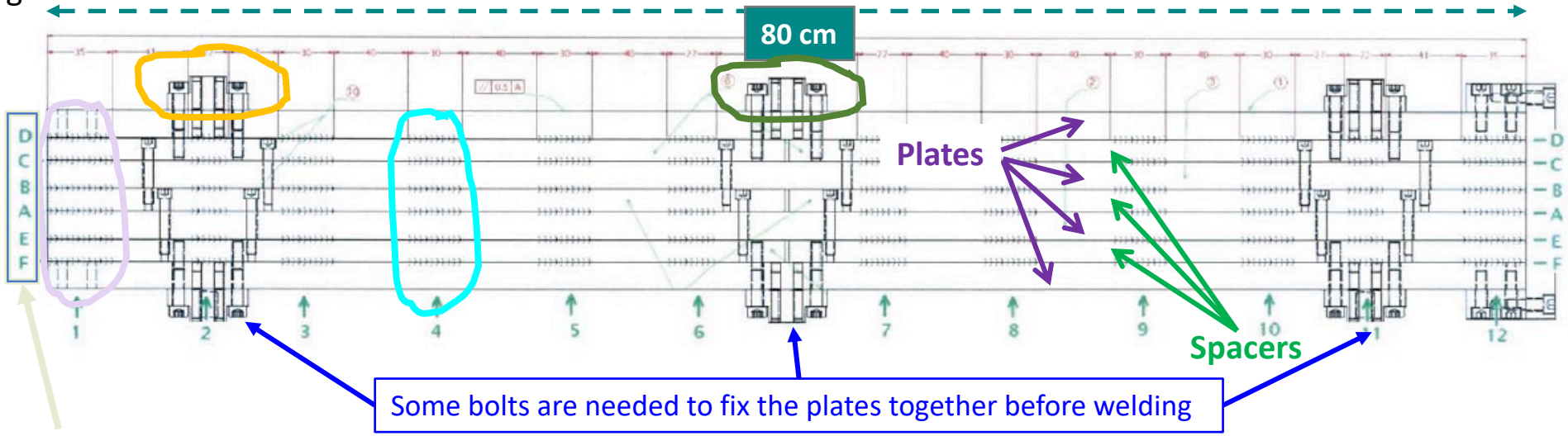
Electron Beam welding (EBW)
➔ Very **narrow**, but needs **vacuum conditions**





New mechanical absorber structure: Welding procedure

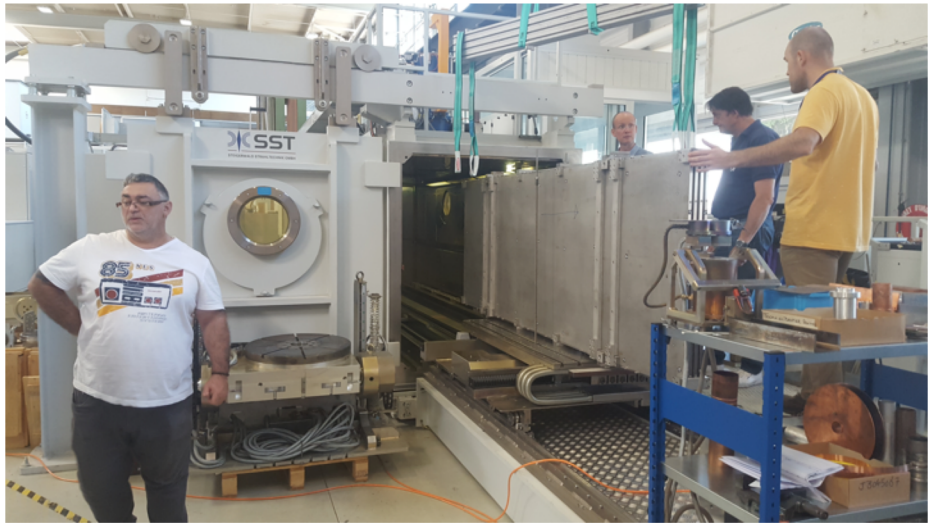
In order to optimize the procedure before welding the bigger prototype **4 smaller prototypes** of different sizes (4 plates 0.8x1m2, 4 plates 0.4x1m2) and **several special pieces** has been welded with ***different welding sequences and machine parameters*** to find the procedure producing the **lowest deformation**.



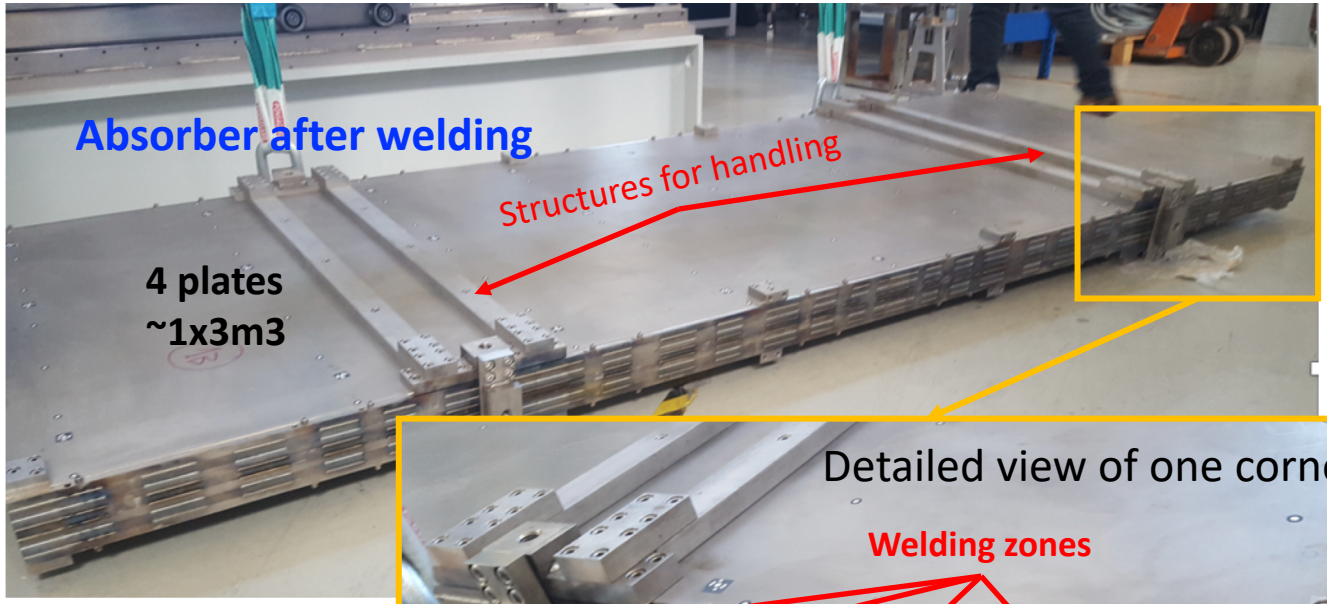
The welding is performed in a certain order not sequential, "jumping" in between the different welding point positions (horizontally and vertically).

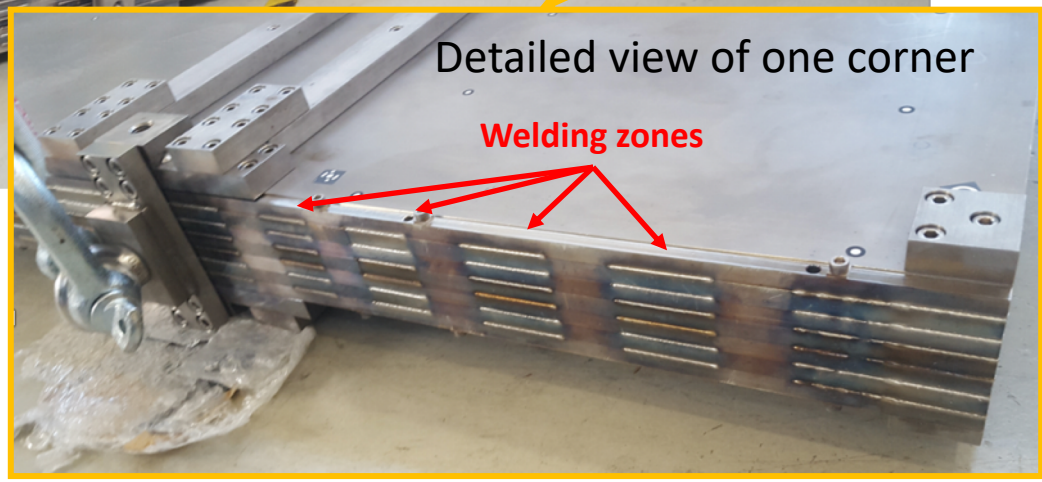
The *order in which the welding is performed* has an influence in the final deformations

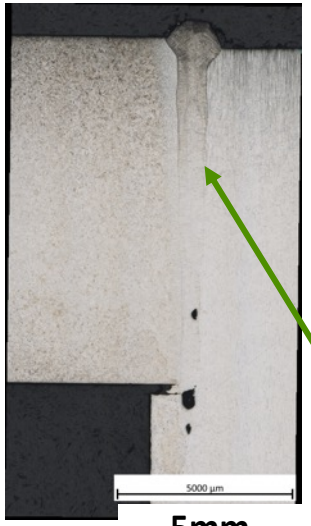
New mechanical absorber structure



Introduction of the pre-assembled absorber structure inside the EBW machine at CERN





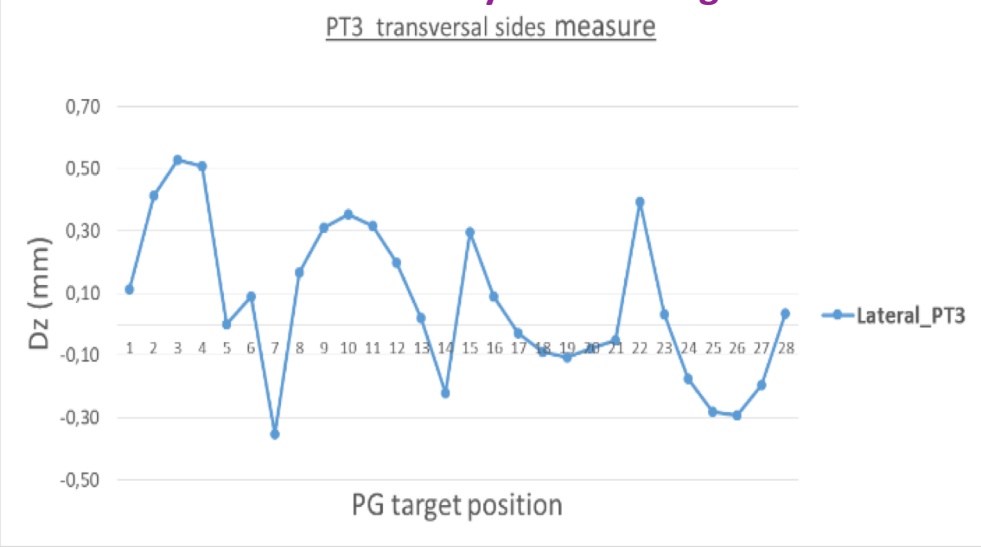


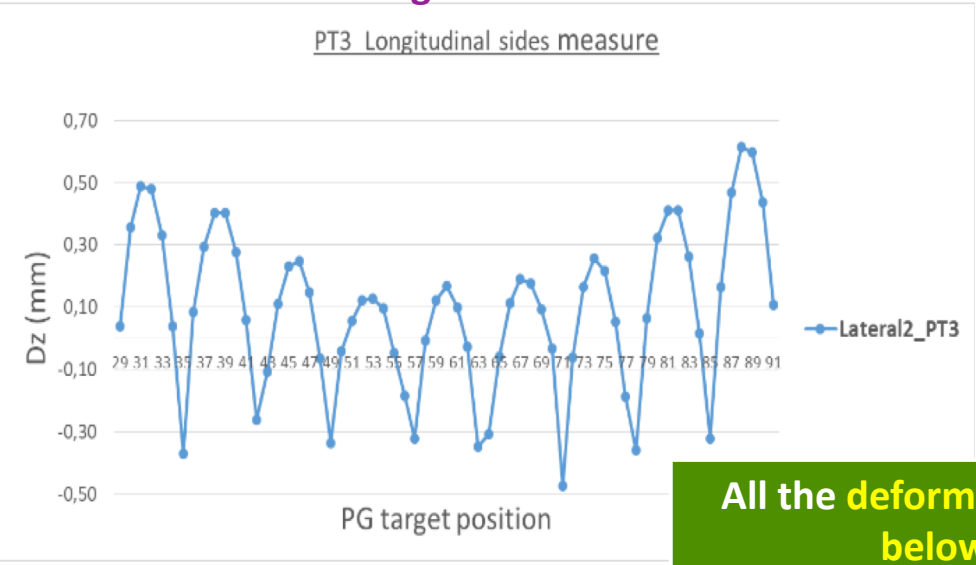
5mm

Detail of welding
(transversal cut zoomed)

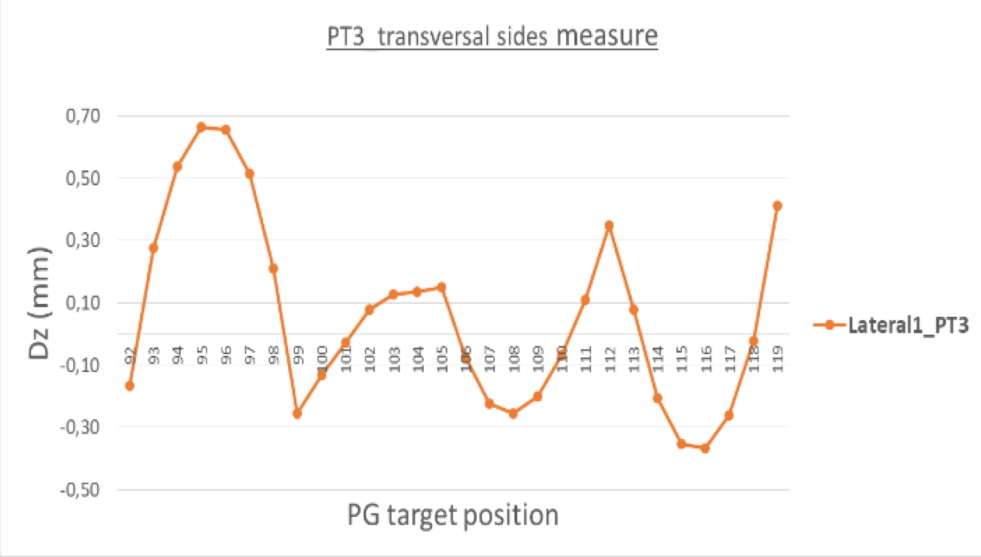
New mechanical absorber structure - Deformations

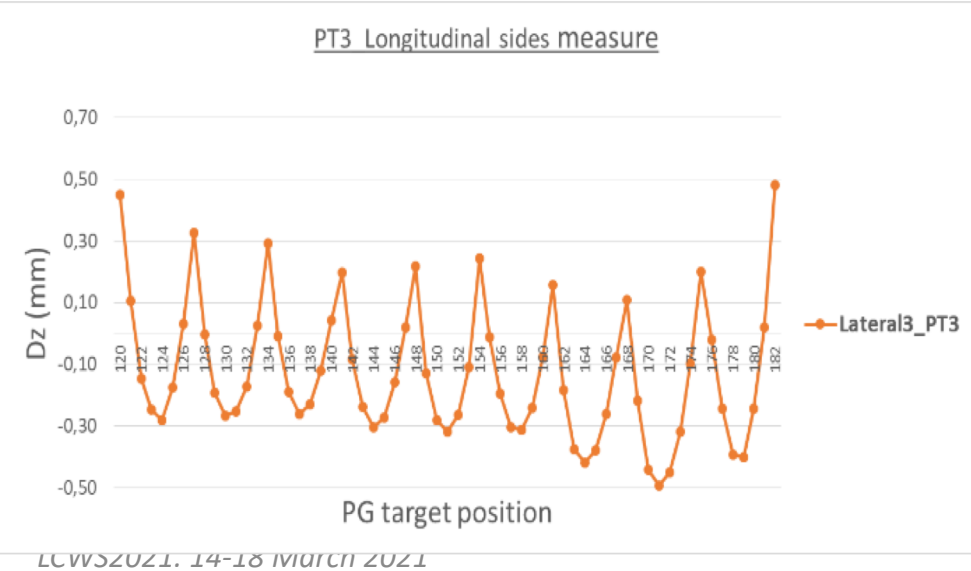
Deformations introduced by the welding in the Z-direction as a function of the target number for the demonstrator for the 4 regions





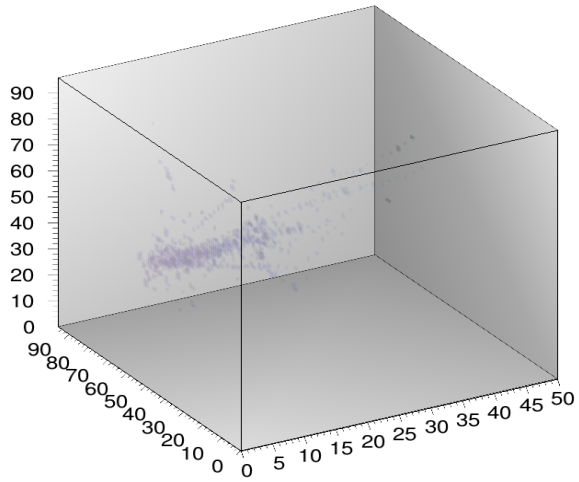
All the deformations observed are below ± 0.6 mm

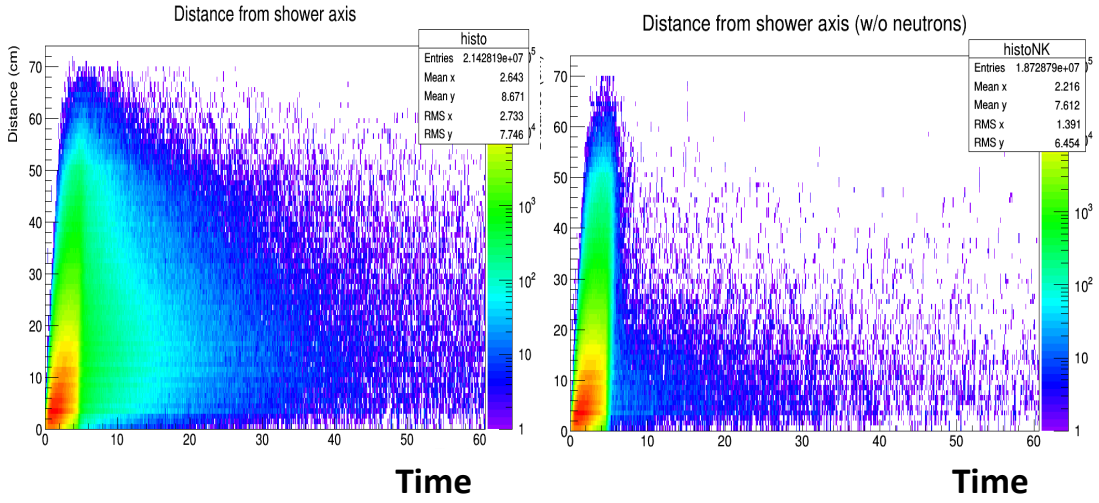




A step forward: including timing readout - motivation

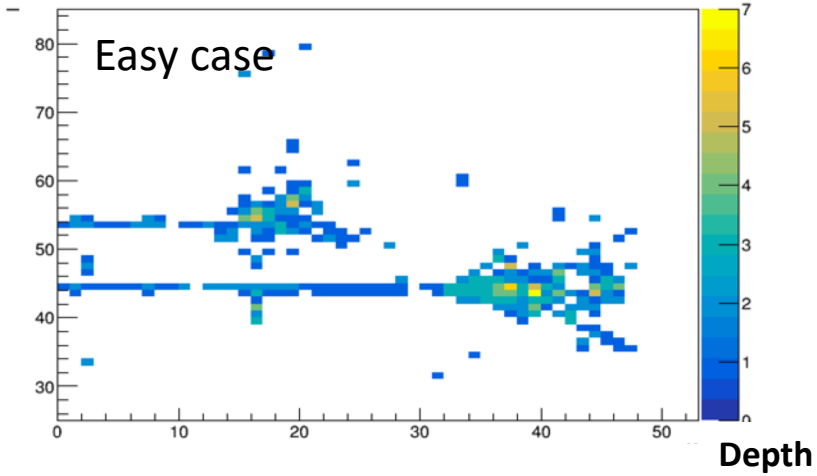
Timing could be an important factor to identify delayed neutrons and better reconstruct their energy

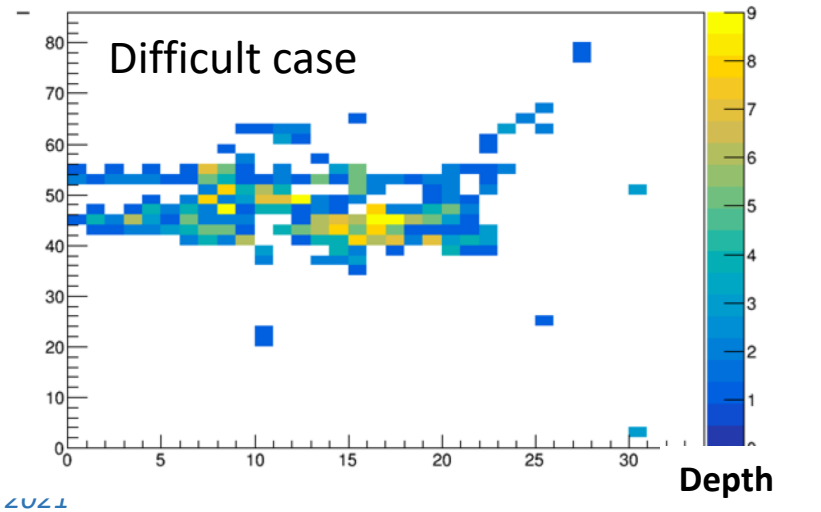




Time information can help to separate close by showers and reduce the confusion for a better PFA application.

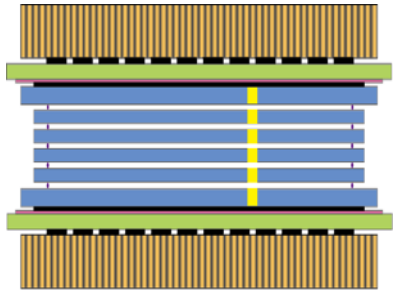
Example: pi-(20 GeV), K-(10 GeV) separated by 8 cm.

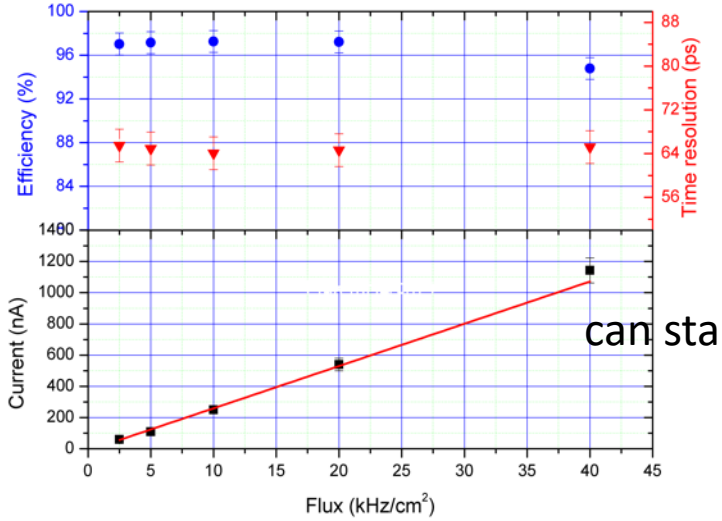




How a time resolution of tens of picoseconds could be achieved ?

❑ Multi-gap RPC are excellent fast timing detectors





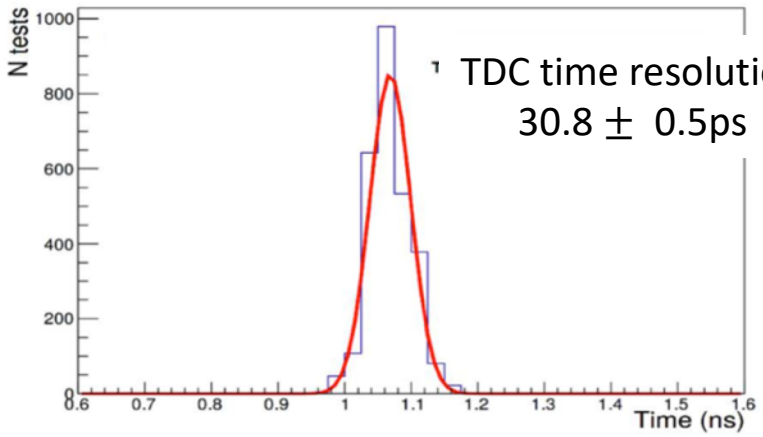
Time resolution
<100 ps
(5 gaps)

can stand for high fluxes

❑ An ASIC with a fast preamplifier, precise discriminator and excellent TDC

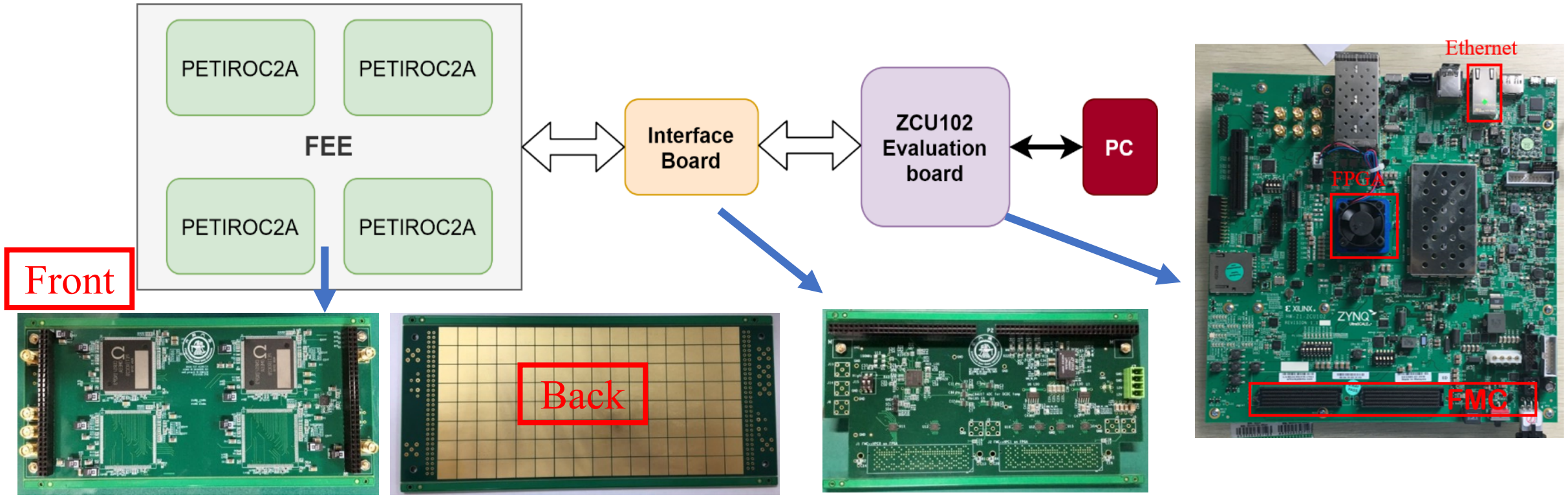
PETIROC ASIC developed for CMS muon upgrade.
32-channel,
jitter < 20 ps rms @ Q>0.3 pC

TDC (delay-line, Vernier, etc …)

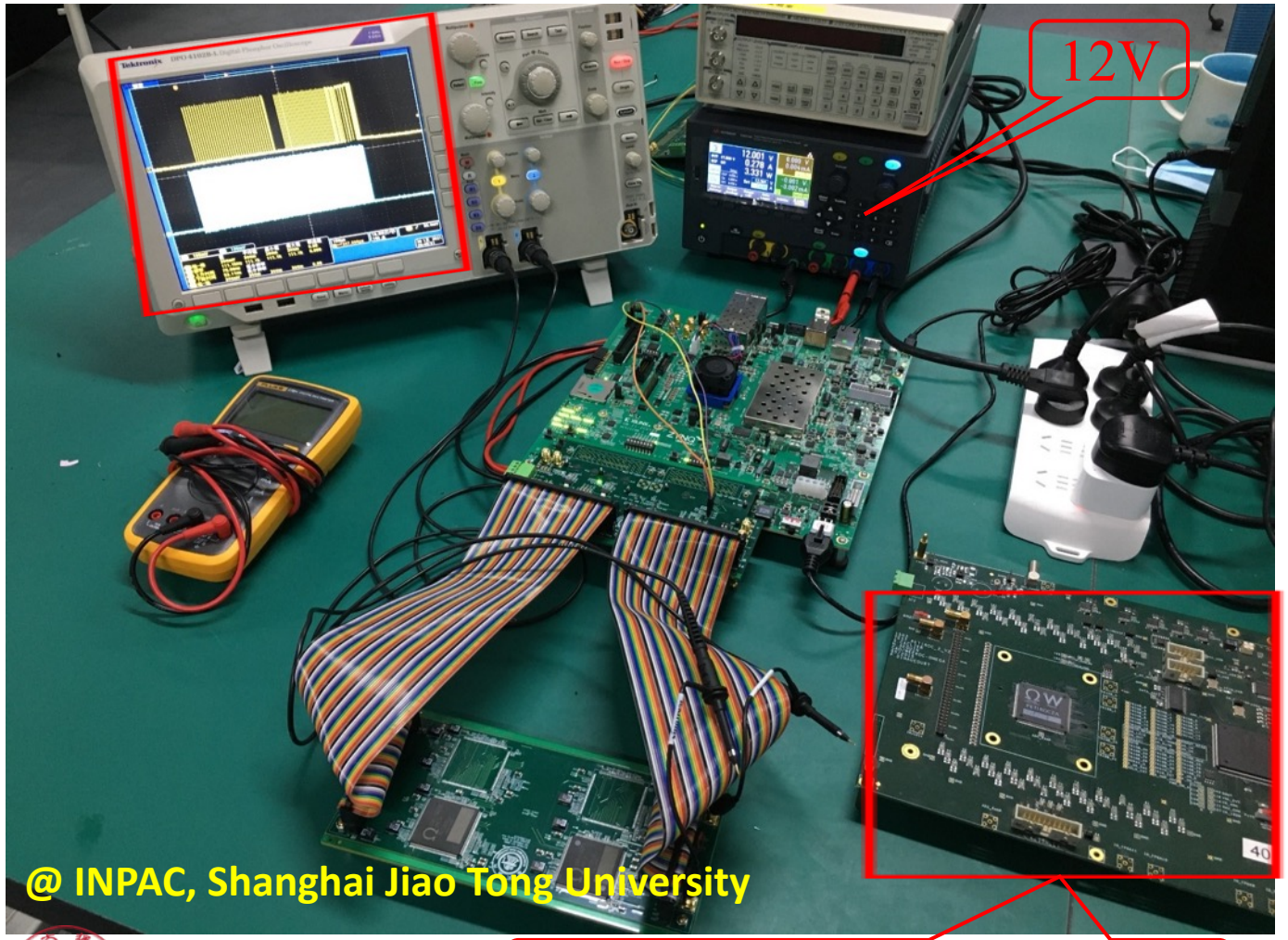


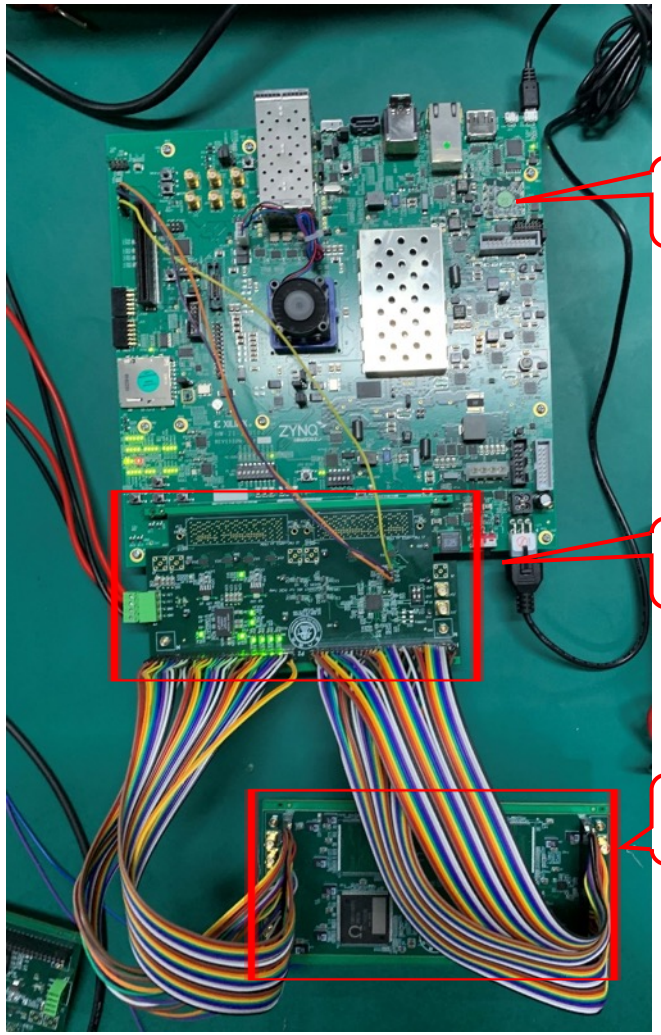
Prototype of Timing Electronics

- Front-End Electronics for MRPC readout with high timing resolution
- The system includes a front-end board (FEB), a detector interface card (DIF) and a data acquisition system(DAQ) based on ZCU102.



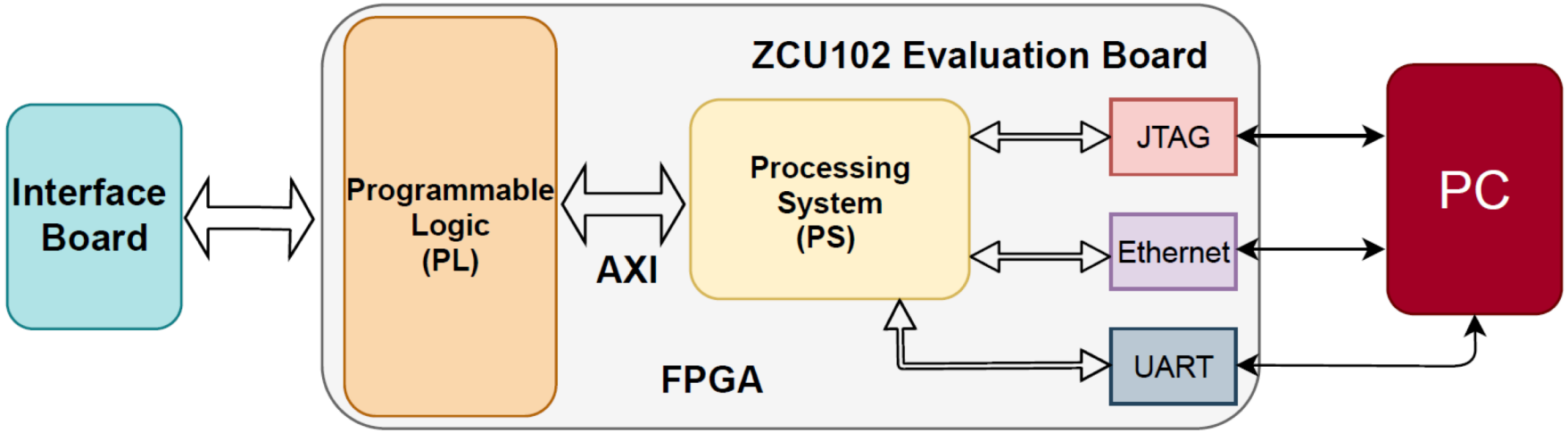
Test System and Setup





Data Acquisition System

- Petiroc2 can be successfully configured through Xilinx ZCU102 platform.
- DAQ system is based on Xilinx ZCU102 in PC side.
- ZCU102 contains Processing System(PS) and Programmable Logic(PL).
- Data transmission between PS and PL, inside of ZCU102, and then ethernet communication between ZCU102 (PS) and PC is used to transfer data.
  - Ethernet transmission between ZCU102(PS) and PC has been achieved.
  - The specific design of DAQ is still ongoing.



Summary

A new SDHCAL prototype with large GRPC, equipped with new electronics closer to the one needed for future experiments and a mechanical structure assembled with novel techniques is under development.

New developments including timing information are being evaluated. New electronic boards are under development and test


THANK YOU FOR YOUR ATTENTION!
ANY QUESTIONS?
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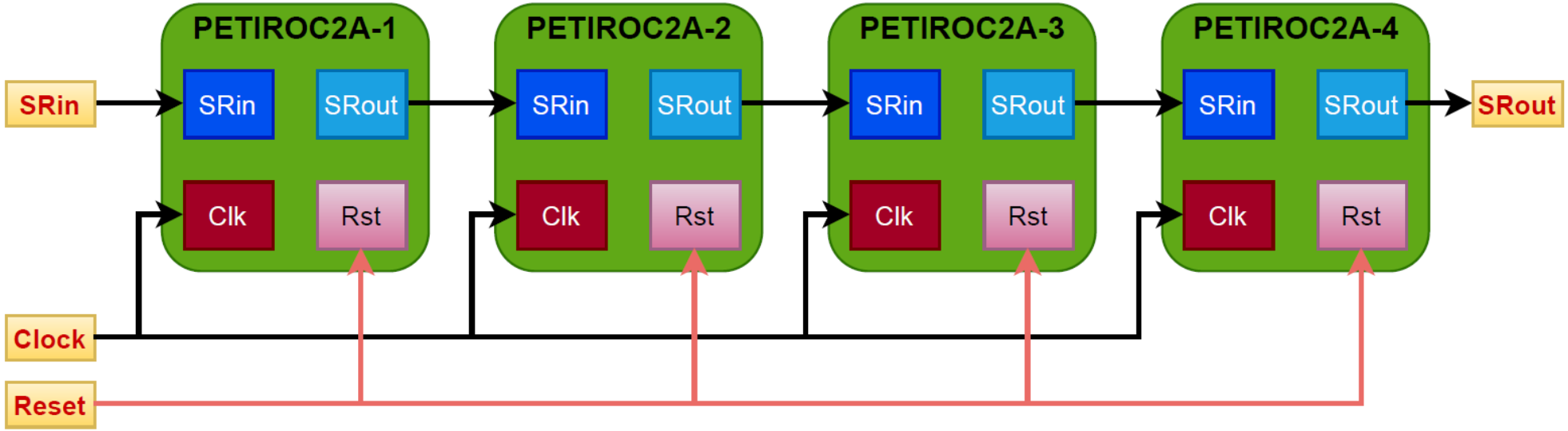
Backup

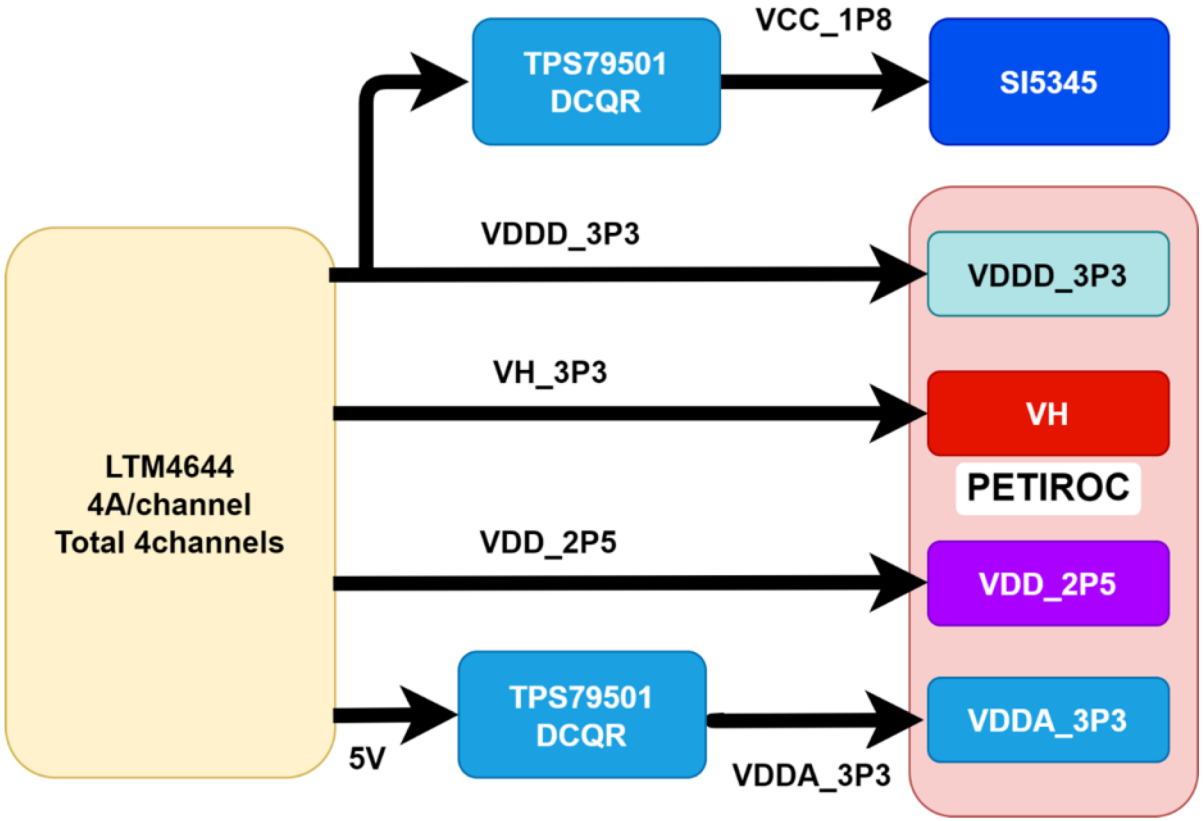
Sub-component Design and Testing

- Front-End readout Board Design
- Components: 4 Petiroc2, clock buffer, 2 headers, SMA for signal injection .
- 128 pads at the bottom, induction unit size: 1cm×1cm.
- The dimension:197mm*82mm, the blind/buried via technology.
- Configuration for petiroc2a with daisy-chain (SPI sending shift register data)

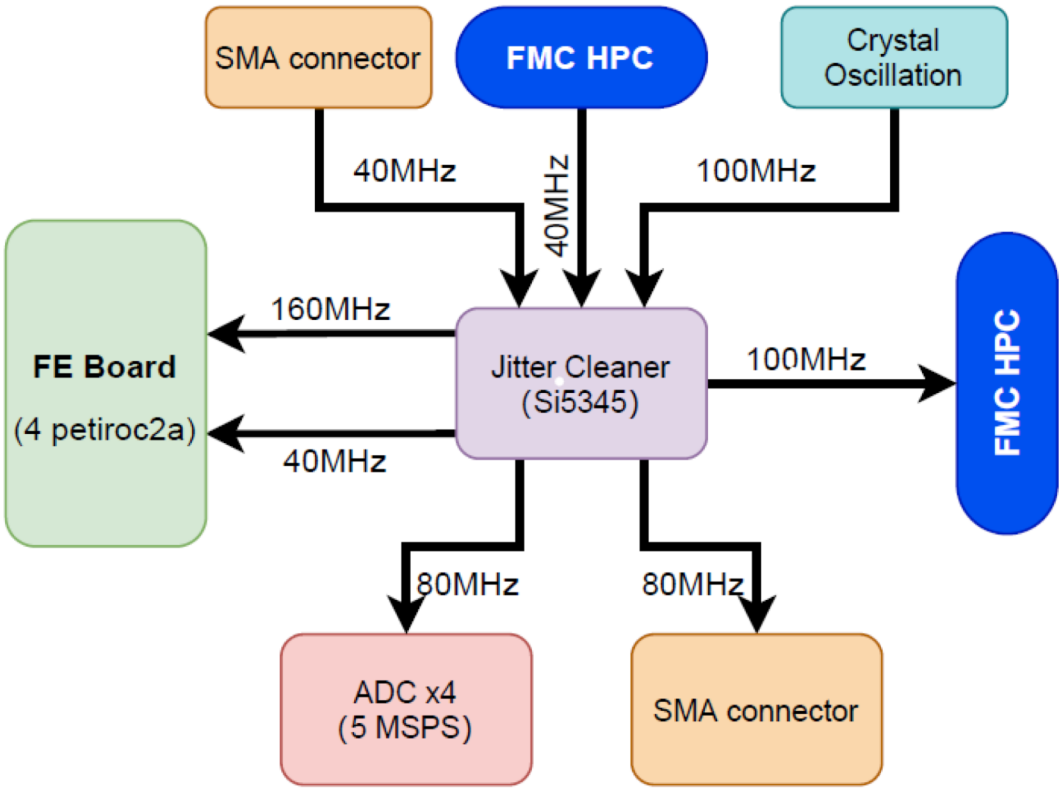


Details on DIF Design and Testing

- Detector Interface Card Design: mainly jitter cleaner and power system



Block diagram of Power Rail



Block diagram of Clock