A System-on-Chip-based Front-end Electronics Control System for the Phase-2 ATLAS Thin-Gap Chambers (TGC)

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on behalf of the TGC Electronics Group

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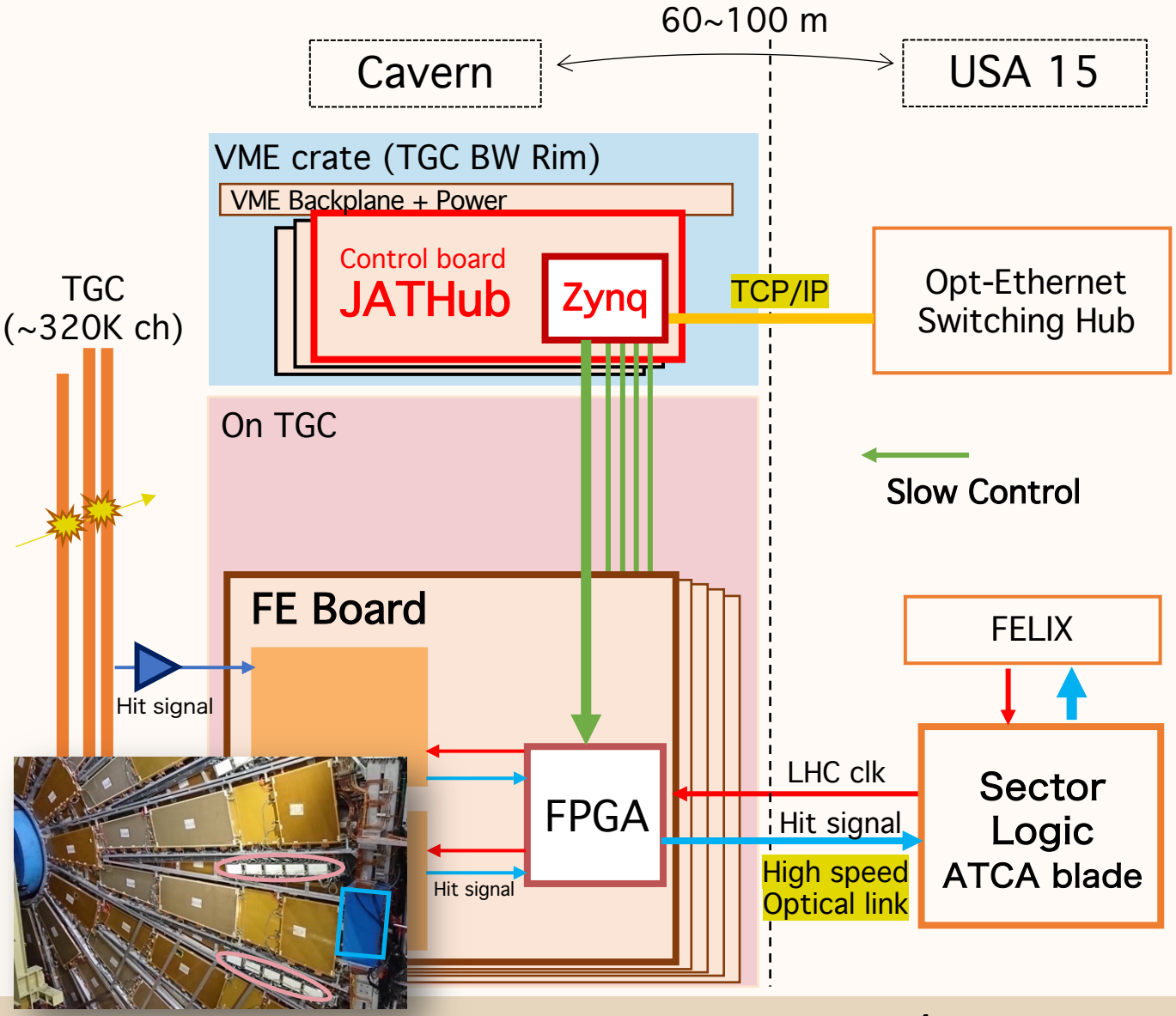
TGC Electronics System

- Front-End Board (1434 on TGC)
  - Send all hit signals to SL boards via optical links (8 Gbps/1 lane)
- Sector Logic (SL) (48 in USA15)
  - Process muon trigger in the endcap region
  - Send LHC clock(40MHz) to the FE Board
- JATHub (148 in VME crate)
  - Program front-end FPGAs
  - Improve robustness against SEU errors in the front-end FPGAs
  - Monitor the LHC clock phase within O(100 ps) distributed to the FE boards

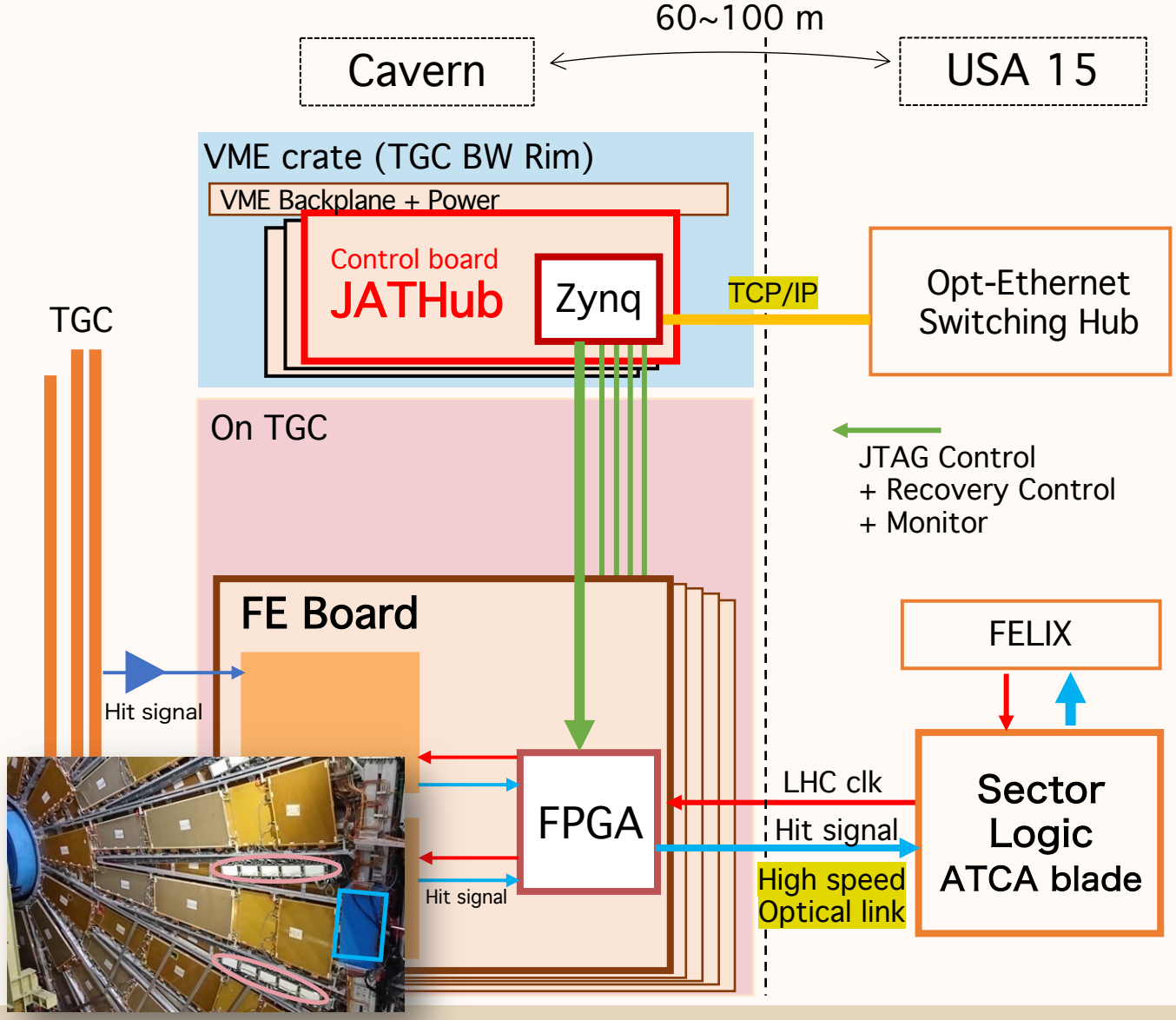


Development of the JATHub

Concept of JATHub Module Design

- FPGAs in the ATLAS cavern need to be controlled from USA15
  - Program the FPGAs by JTAG
  - Monitor LHC clock phase on FE Boards
  - Build the robust front-end system
    - Recover the function of the FPGAs, when unrecoverable SEU error occurred
    - Reset and reestablish this link, when Optical-link is unlocked

→ Control hub boards for FPGAs on the FE Board named "JTAG Assistance Hub" ("JATHub") are introduced



Design of the JATHub

- Control max. 11 FE Boards

  through two CAT6 cables for each

  - Reuse currently available signal cables
  - FE Board: 1434, JATHub: 148

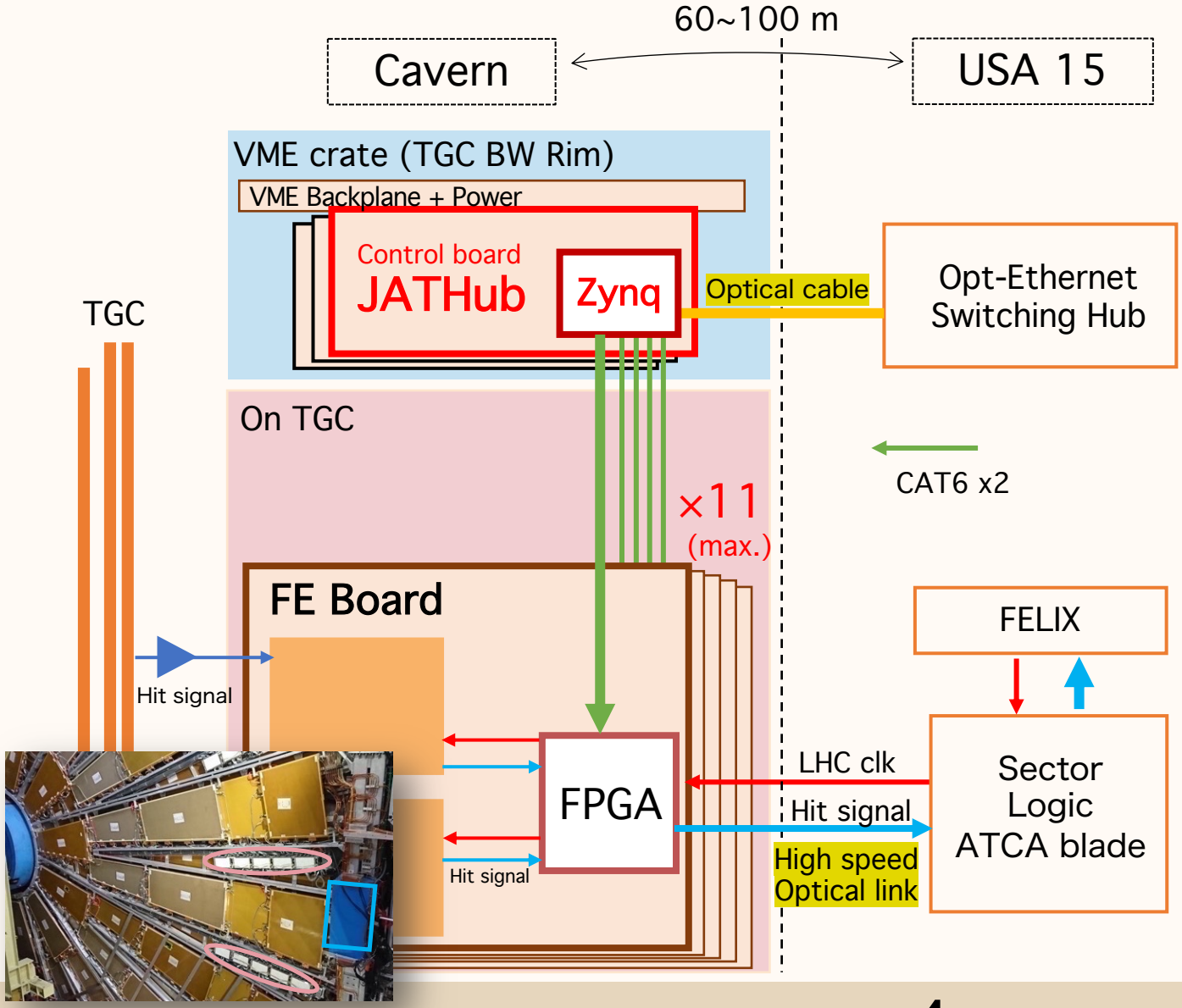
- Equipped with Zynq-7000 SoC

  as the main driver

- The boards will be housed in

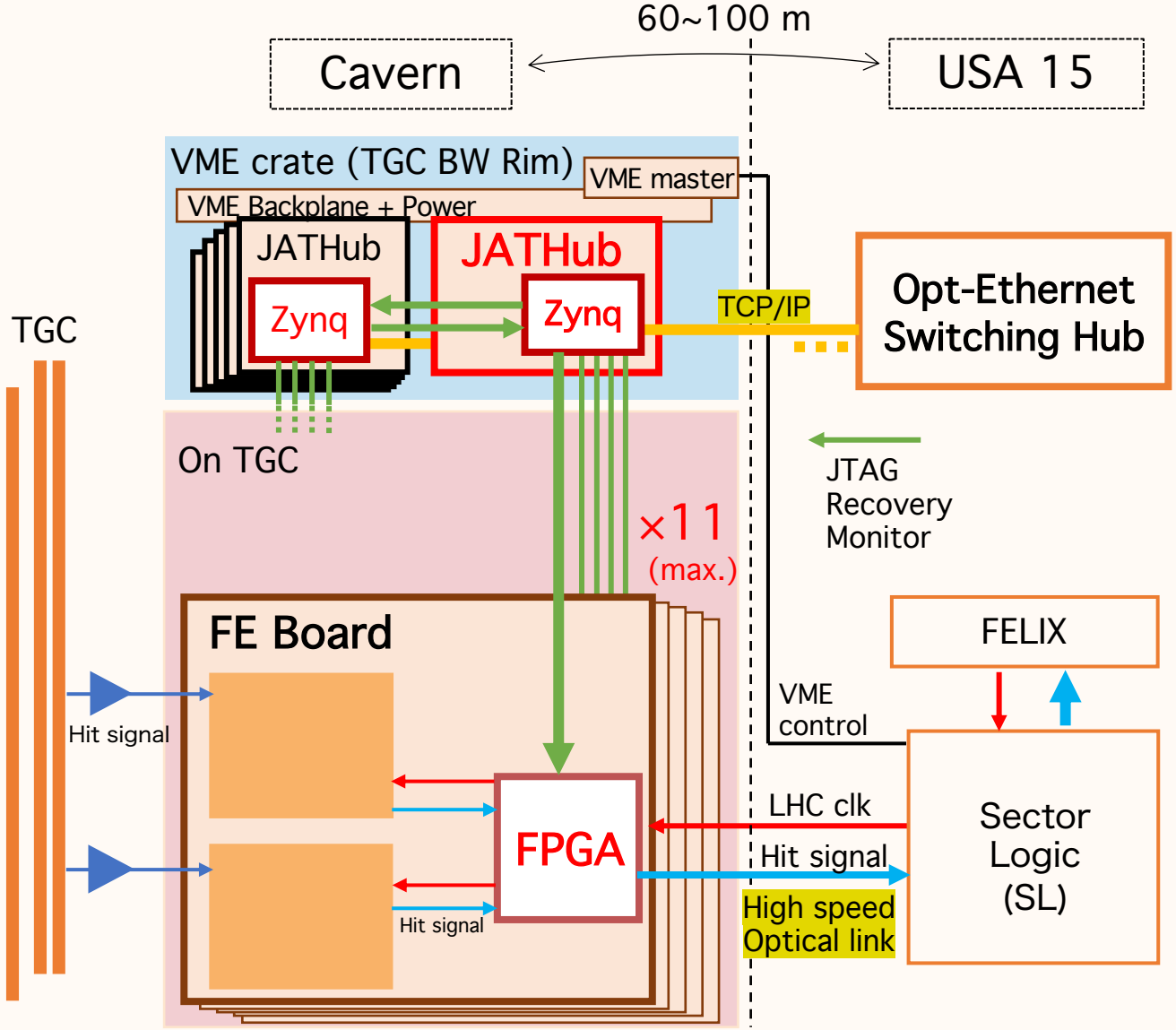
  the VME crates being used in the pit

  (6 JATHubs in 1 VME crate)

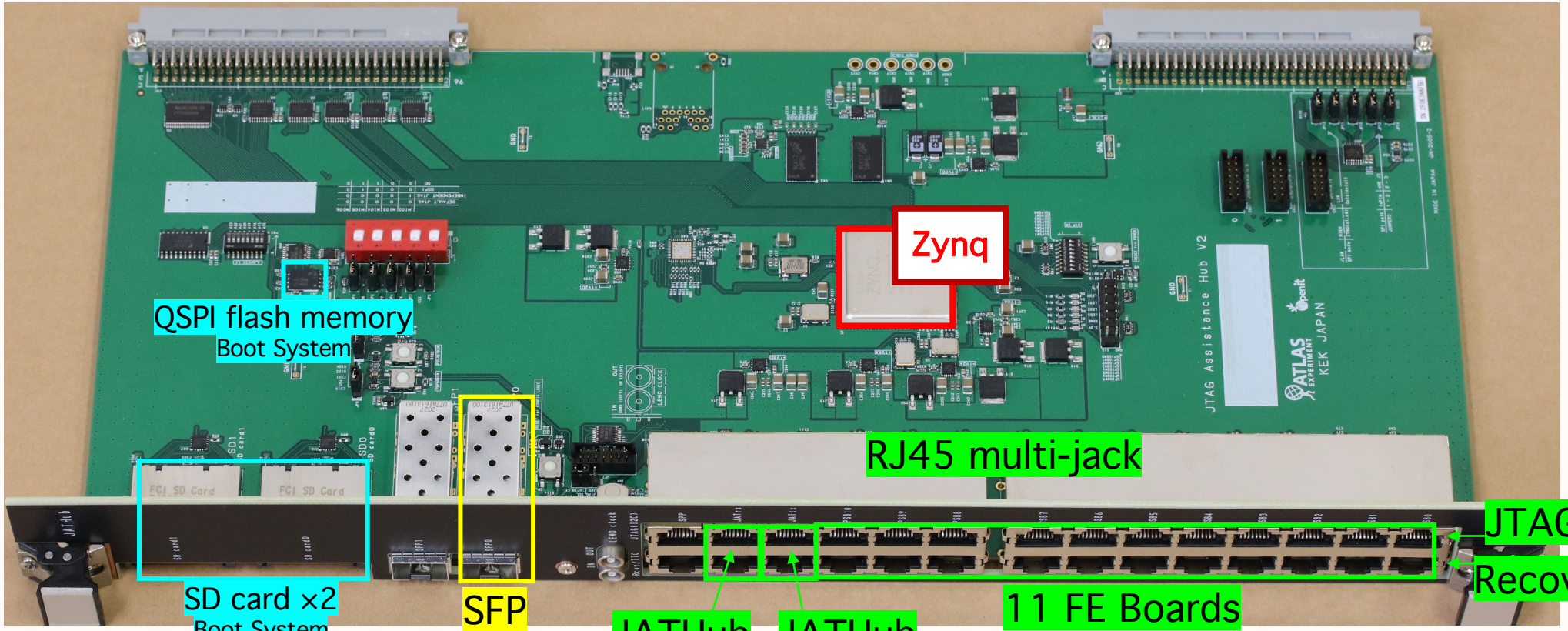


Interfaces and Functions of the JATHub

- Opt-Ethernet network with USA15
- Control of max. 11 FPGAs on the FE Boards
  - JTAG access to the FPGAs
  - Recover the FPGAs from unrecoverable SEU errors
  - Monitor LHC clock phase
- Interactive control with the neighboring JATHub
  - JTAG access to the Zynq
  - Recover the Zynq from unrecoverable SEU errors
- Redundant boot system with SD ×2, QSPI
- Behaving as a VME slave module



JATHub Final Prototype Board (delivered Feb. 2021)



- Zynq-7000: XC7Z045-2FFG900I
- PCB 14 layers
- Height: 9U, Width: VME 2 slots

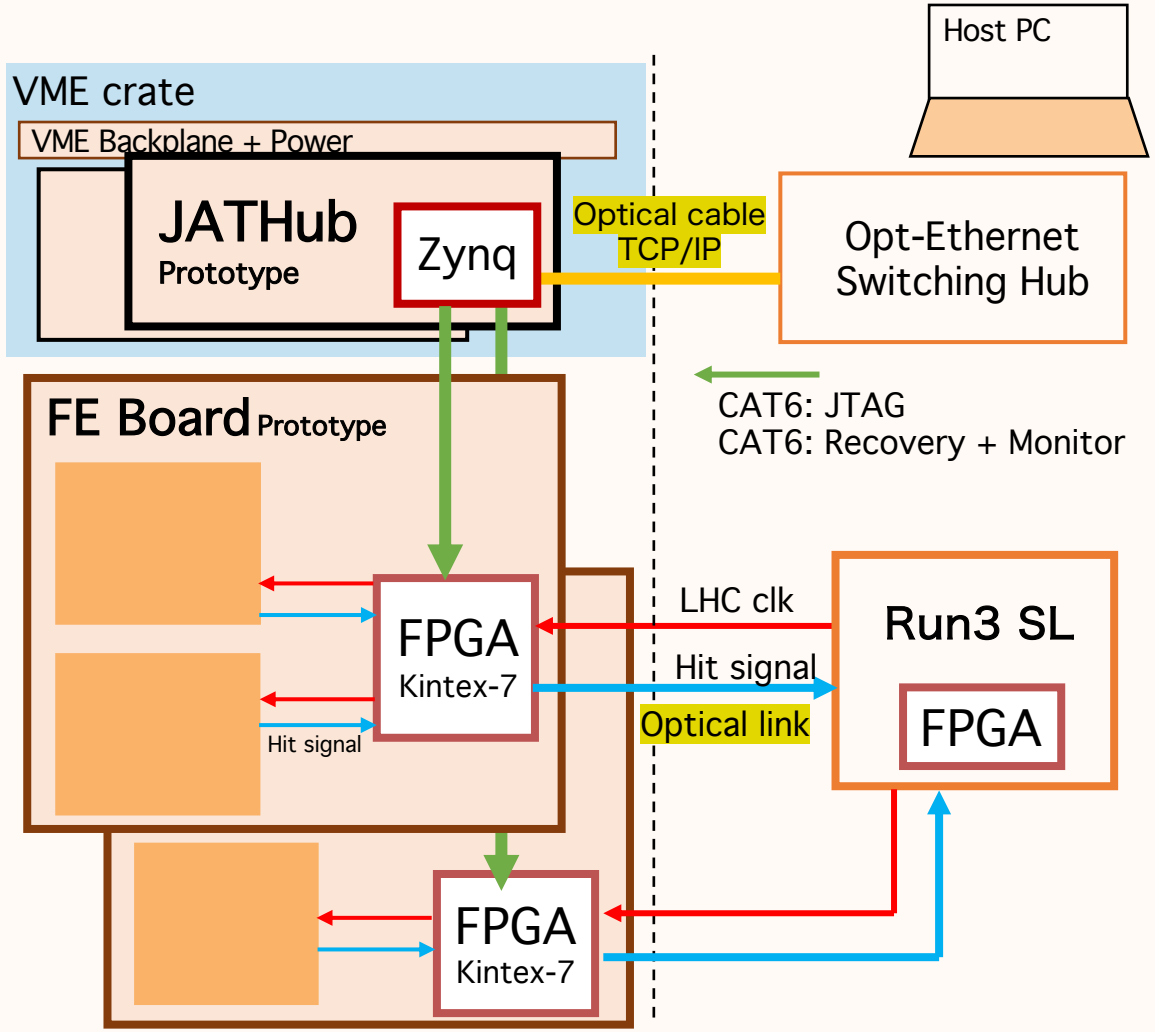
Open source consortium of Instrumentation

Integration Test for the TGC Front-end Electronics Control System

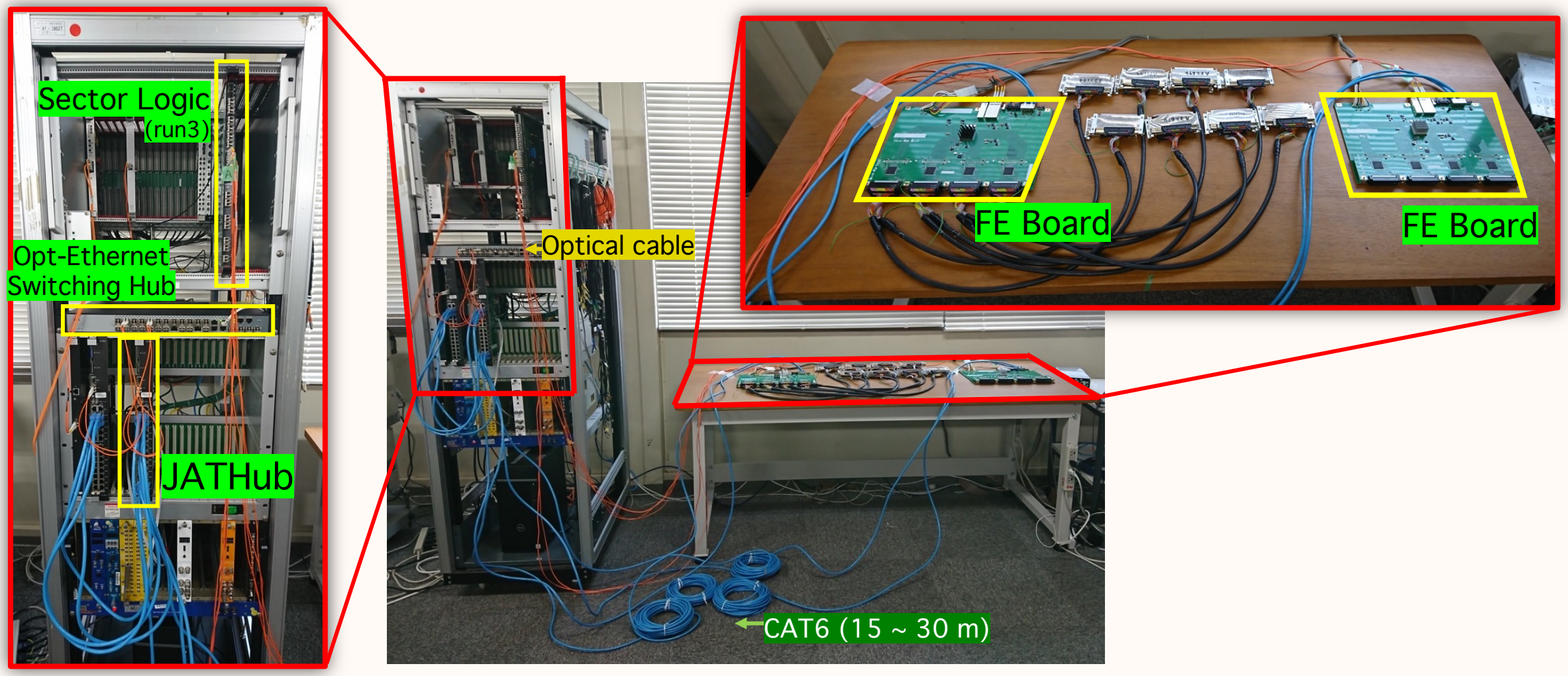
TGC Front-end Control System Integration Test

- Built a testbench (FE Board, SL, JATHub) at KEK
  - Substitution of the SL ATCA blade: Run3 SL

- The list of test items
  ① JTAG control with the infrastructure close to the ATLAS cavern
  ② Demonstration of the measures against radiation damage
  ③ Calibration of the LHC clock on the FE board



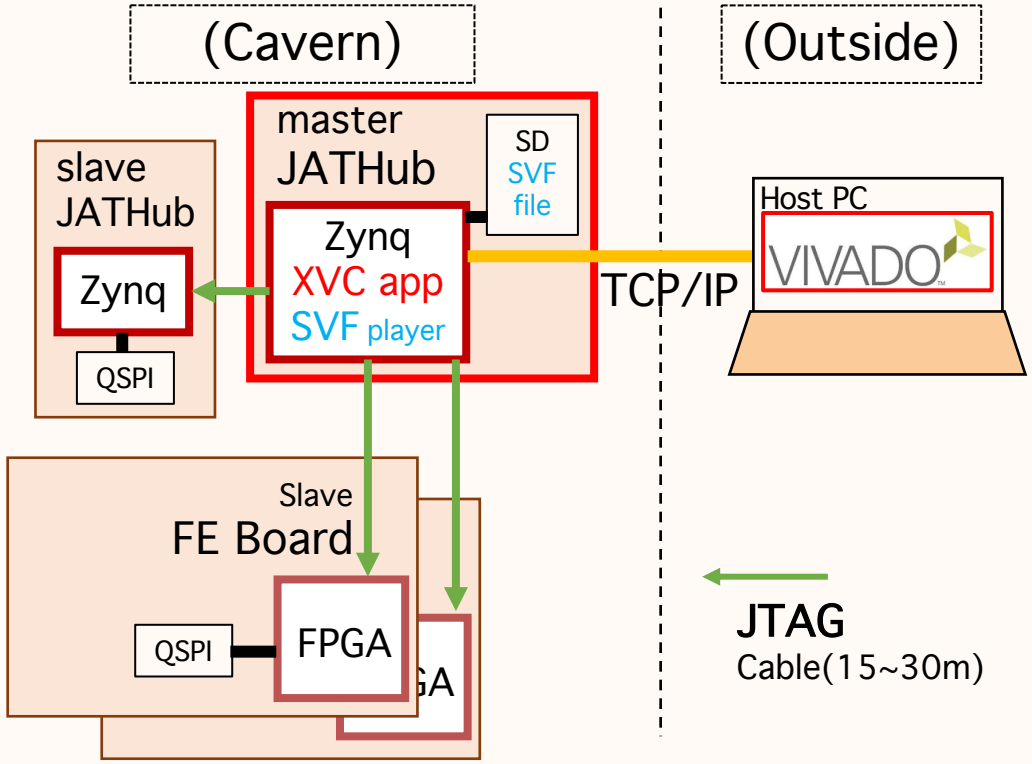
Testbench for the Integration Test



① JTAG Access to Remote FPGAs and Zynq

- FPGAs and Zynqs in the ATLAS cavern need to be configured remotely by JTAG access

- 3 targets of JTAG access
  - Program firmware to **FPGAs**
  - Program files to **QSPI flash memory**
    - FPGA's QSPI: Configuration file including firmware data
    - Zynq's QSPI: Boot file
  - Debug **firmware logic on Zynq, FPGA**

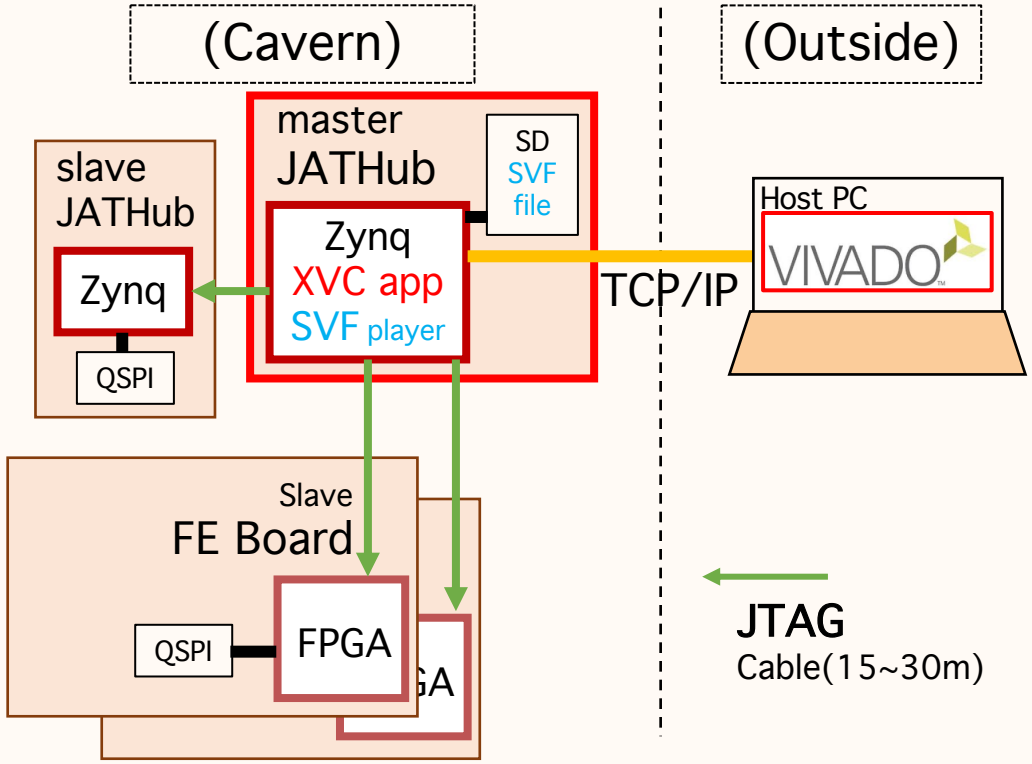


- QSPI programming is the most important for the operation in the cavern, because when a module is reset, it reads the file in QSPI first

① Implementation of JTAG Access Function

Implemented 2 kinds of JTAG access methods

- Xilinx Virtual Cable (XVC) :
  - Access to master JATHub with TCP/IP from Host PC and access to the slave module with JTAG, by running the XVC application in master JATHub (XVC is the TCP/IP based protocol accessing like JTAG)
  - Enable to use the functions of Vivado running in a Host PC for remote FPGAs
    - ・Program FPGA and QSPI
    - ・Debug firmware logic
      - ・Integrated Logic Analyzer (ILA)
      - ・IBERT
- Serial Vector Format (SVF) player :
  - SVF player handles JTAG signals of slave FPGAs, Zynqs by bit-banging by reading SVF file (records JTAG pattern)
  - SVF file stored in SD can be made by Vivado
  - SVF player can program FPGA, QSPI

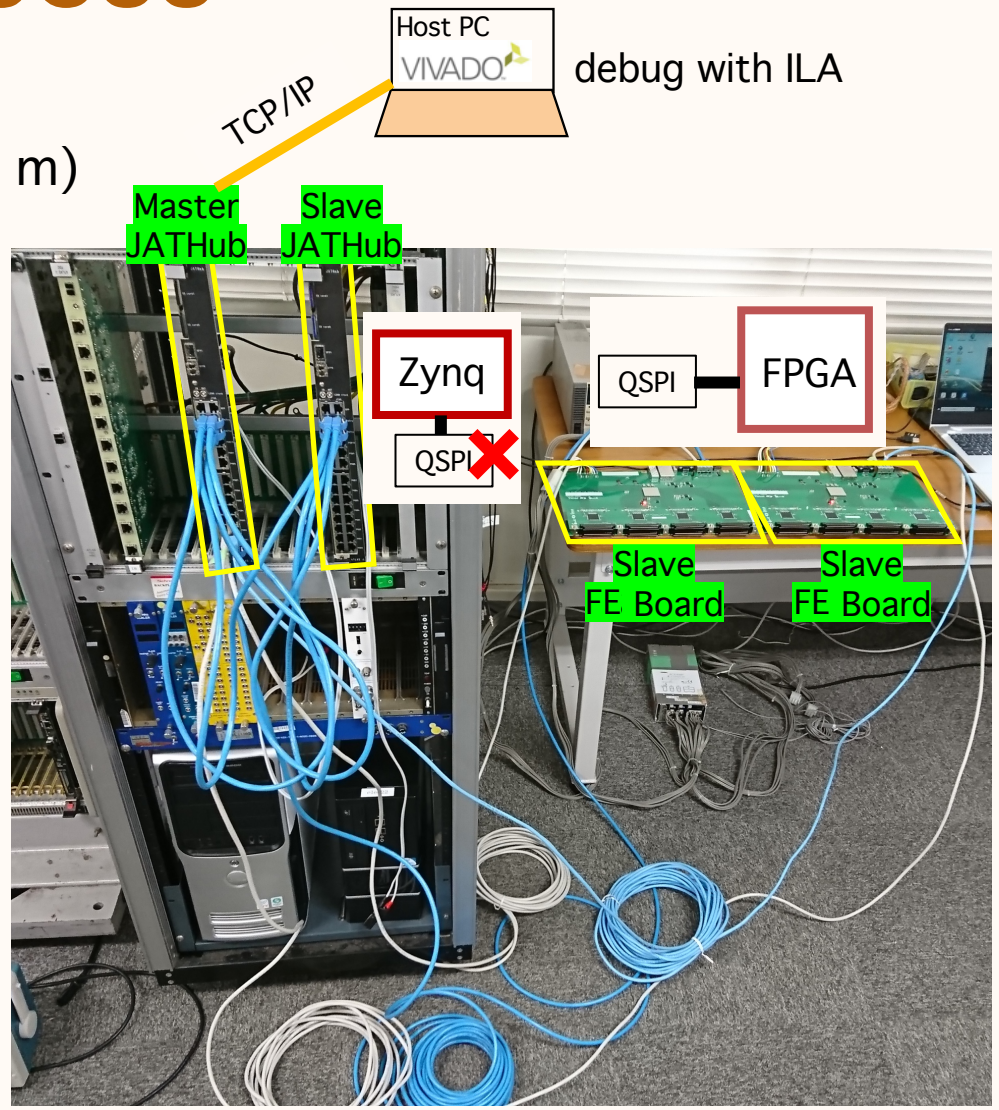


① Testing of JTAG Access

- Connected master JATHub and slave module by CAT6 (15~30 m)
  - Optimized the JTAG clock freq. to 1.25 MHz

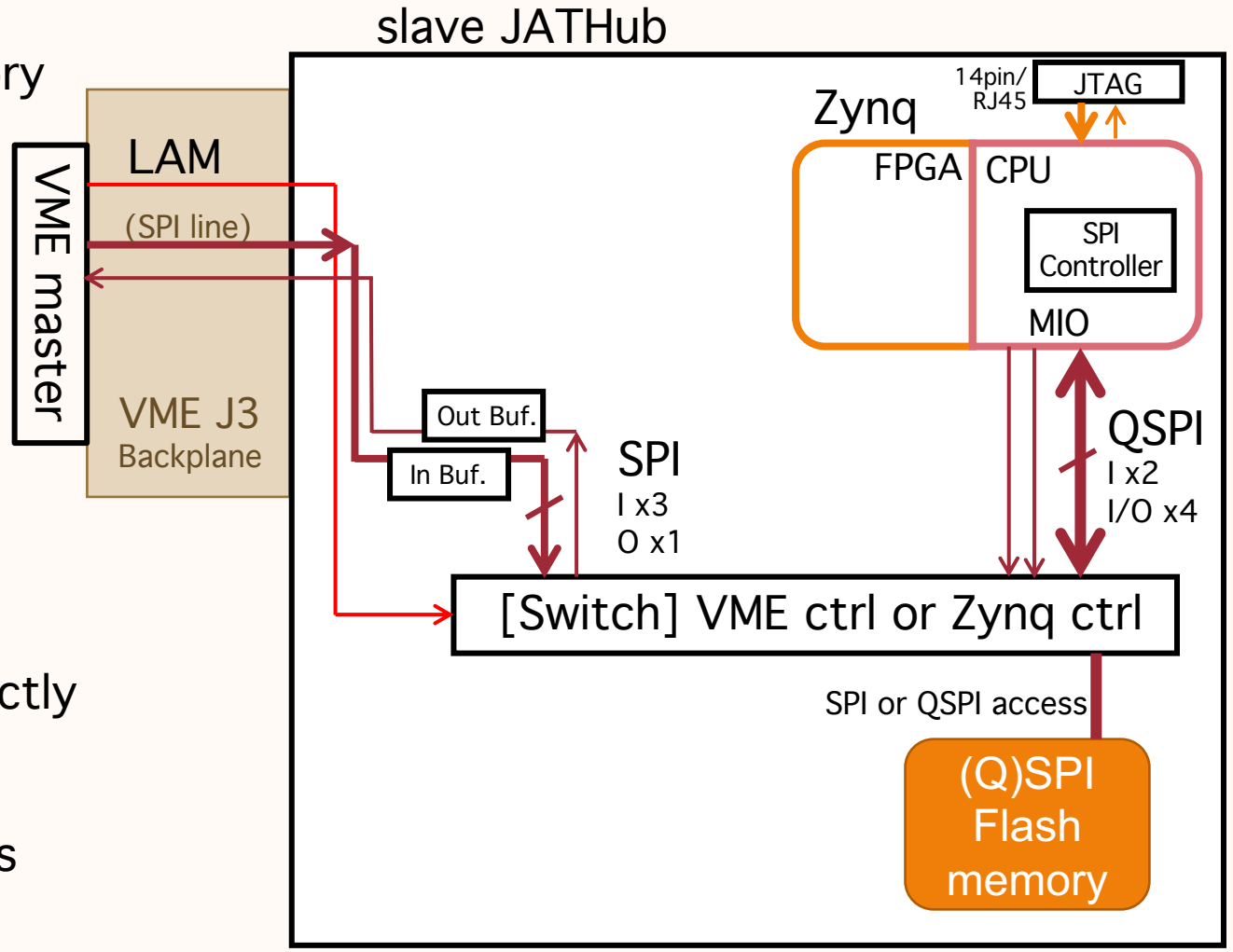
- Program FPGA, FPGA's QSPI
  - XVC: Succeeded by controlling Vivado running in a Host PC
  - SVF player: Succeeded
  - -> We will use SVF player at the operation in the cavern
    to avoid TCP/IP access during the JTAG operation
- Debug firmware logic on Zynq, FPGA
  - XVC: Succeeded by controlling Vivado running in a Host PC
  - -> We will use XVC at the operation in the cavern

→ **Succeeded to configure remote FPGAs and Zynq**
*[problem] Failed to program only Zynq's QSPI



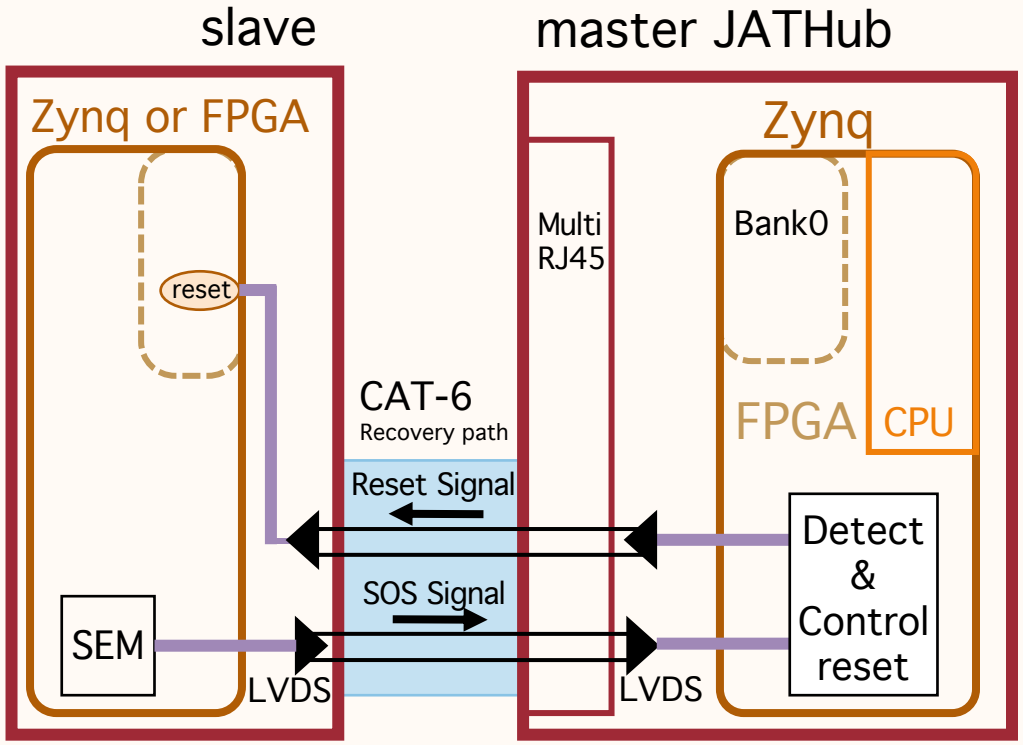
Increase the Accessibility to Zynq flash memory

- Need to program remote Zynq QSPI flash memory to rewrite Zynq's boot file
- Failed to program by JTAG access via Zynq
  - Indirect QSPI programming via XVC failed by unknown reason
  - Vivado doesn't support to make SVF file for the indirect programming of Zynq's QSPI
- Established bypass to program Zynq's QSPI directly using VME path
- Software-level development of the direct access to Zynq's QSPI with this bypass is in progress



② Mitigation Scheme for SEU on Slave Modules

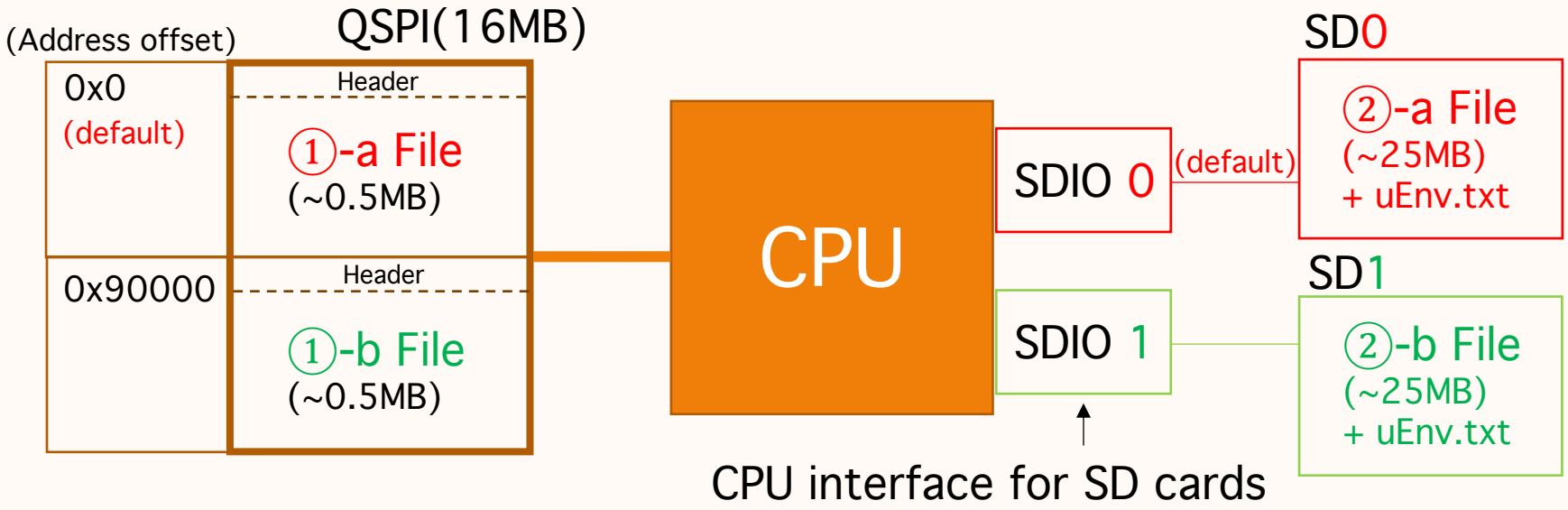
- Soft Error Mitigation (SEM) controllers are running on the FPGAs and Zynqs, and automatically recover the most of SEU errors
- Reset signal are triggered by JATHub when unrecoverable SEU error is reported by a slave module via a robust communication path
- Equipped debouncer IC to reject unwanted short reset signals
- Implemented the recovery path in master JATHub, with voting logic at various places of the path
- Tested this recovery function
  - Master JATHub connects with slave JATHub, and slave FE Boards
  - Succeeded to recover the slave modules



② JATHub Boot System with 2 SDs & QSPI

- Boot Files for Zynq SoC can be divided into ①, ② (petalinux 2018.3)
  ① Initial Boot File (BOOT.BIN) (~0.5 MB)、② Second Boot File (image.ub, firmware) (~25 MB)
  - ① Program the same 2 Initial Boot Files (①-a, ①-b) into QSPI, attaching offset value for each
  - ② Store the same 2 Second Boot Files (②-a, ②-b) into each SD card(SD0, SD1)

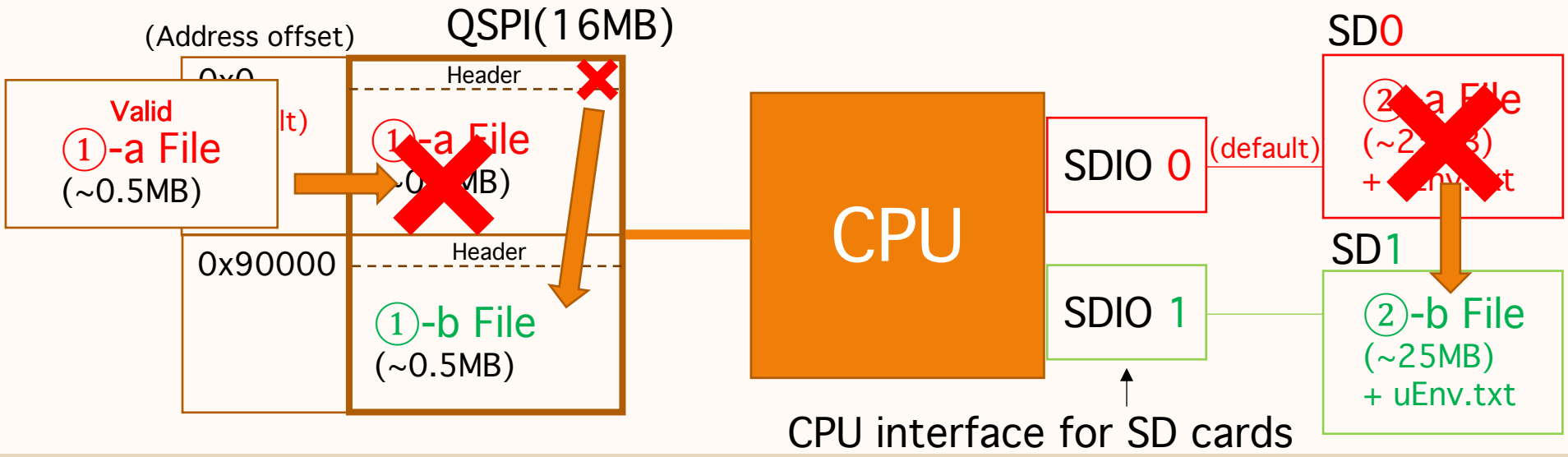
- By default, when CPU is powered on, CPU reads ①-a File with the smallest offset value at first
- By default, after ①-a File is loaded, CPU reads ②-a File



② System of Boot Redundancy on the JATHub

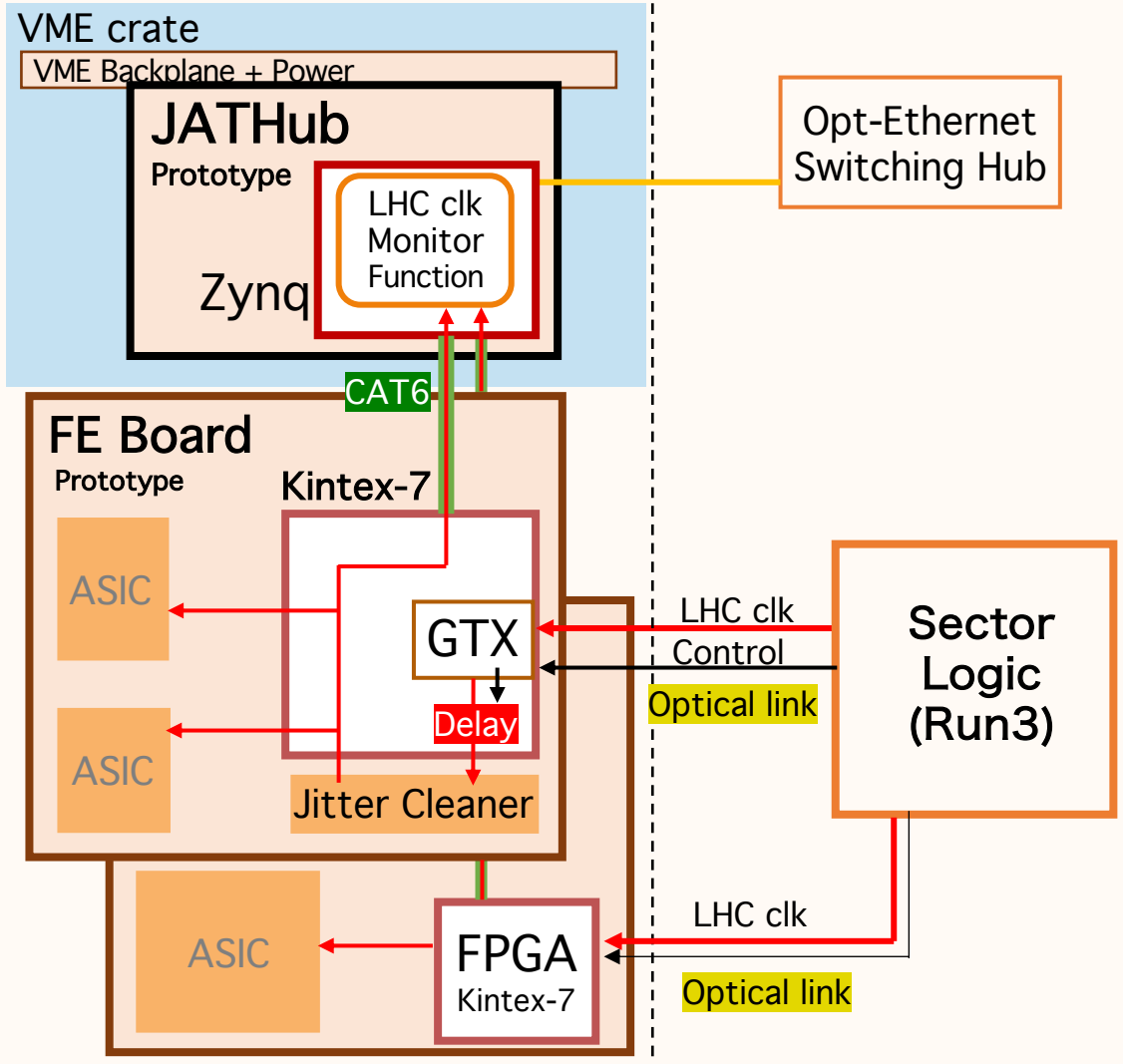
- When CPU fails to read ①-a File
  - When the header of the file was damaged
    → CPU will automatically read ①-b File
  - When something wrong in the file, except for its header
    - Overwrite a valid ①-a File from outside
    → CPU will read the valid ①-a File
- When CPU fails to read ②-a File
  → CPU will automatically read ②-b File in SD 1

※ Tested this boot redundancy with invalid ①-a and ②-a; Boot system worked correctly



③ Calibration of the LHC Clocks on FE Boards

- LHC clock phases on all the FE Boards need to be matched in accuracy of <1 ns
- Due to the different fiber length of SL and FE board, Calibration of the LHC clock on FE board is required
- Procedure of the calibration:
  1, SL sends LHC clock to FE Board by optical link
  2, FPGA recovers LHC clock from 8b/10b protocol
  3, JATHub monitors the distributed LHC clock
  4, SL controls delay parameters in FPGA to adjust the recovered LHC clock
- Demonstrated the calibration in the testbench

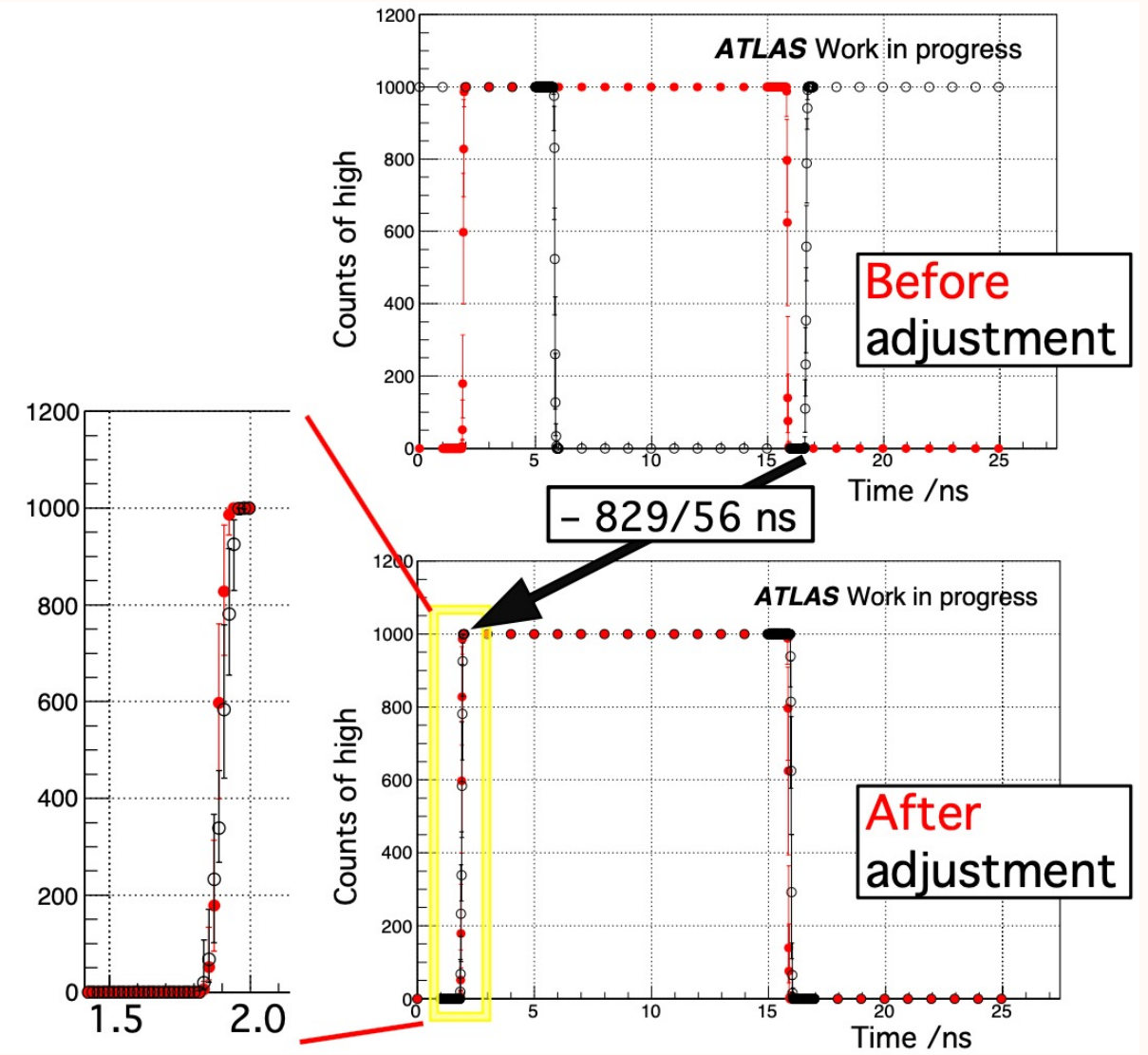


③ Demonstration of the LHC Clocks Calibration

- Realized to monitor the LHC clocks of FE boards on JATHub at the same time in accuracy of 1/56 ns
- Realized to delay the LHC clocks of 2 FE boards by the SL in accuracy of 1/56 ns

- According to the monitoring result on the JATHub, the delay parameter on the FE board was adjusted by the SL
- The phase adjustment was achieved

→ The clock distribution with fixed latency in accuracy of ~20 ps was successfully performed



Summary

✓ Designed and developed the JATHub as the center of the Phase-2 ATLAS Muon Trigger front-end control system, satisfying the following requirements
  - Remotely control and monitor ~1500 FPGAs in the ATLAS cavern
  - Ensure the robust operation even in a high radiation area

✓ Almost completed the testing of the JATHub final prototype board

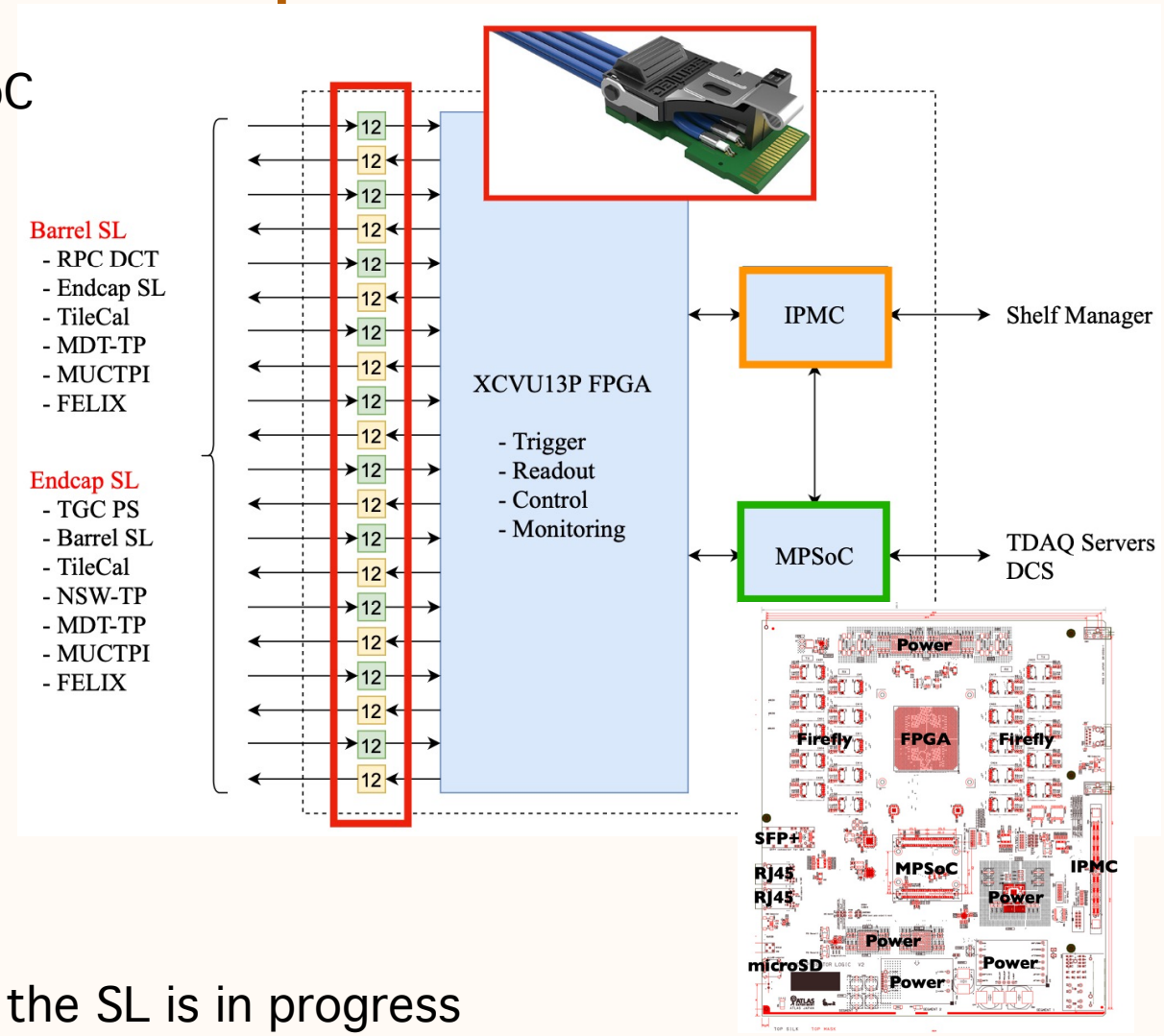
✓ Almost completed the demonstration of the front-end control system in the testbench

- Preparing for the FDR in Jul. 2021
- Preparing for the PRR in Feb. 2022
- Produce about 160 JATHub mass-production model and install in 2025

Functions of the JATHub	Implementation & Testing
1000BASE-X Opt-Ethernet	Clear
JTAG access to remote slave modules	Clear
Recovery procedures for slave modules	Clear
Monitoring the LHC clk on PS Board	Clear
Redundant boot system	In progress
Behaving as a VME slave module	Clear

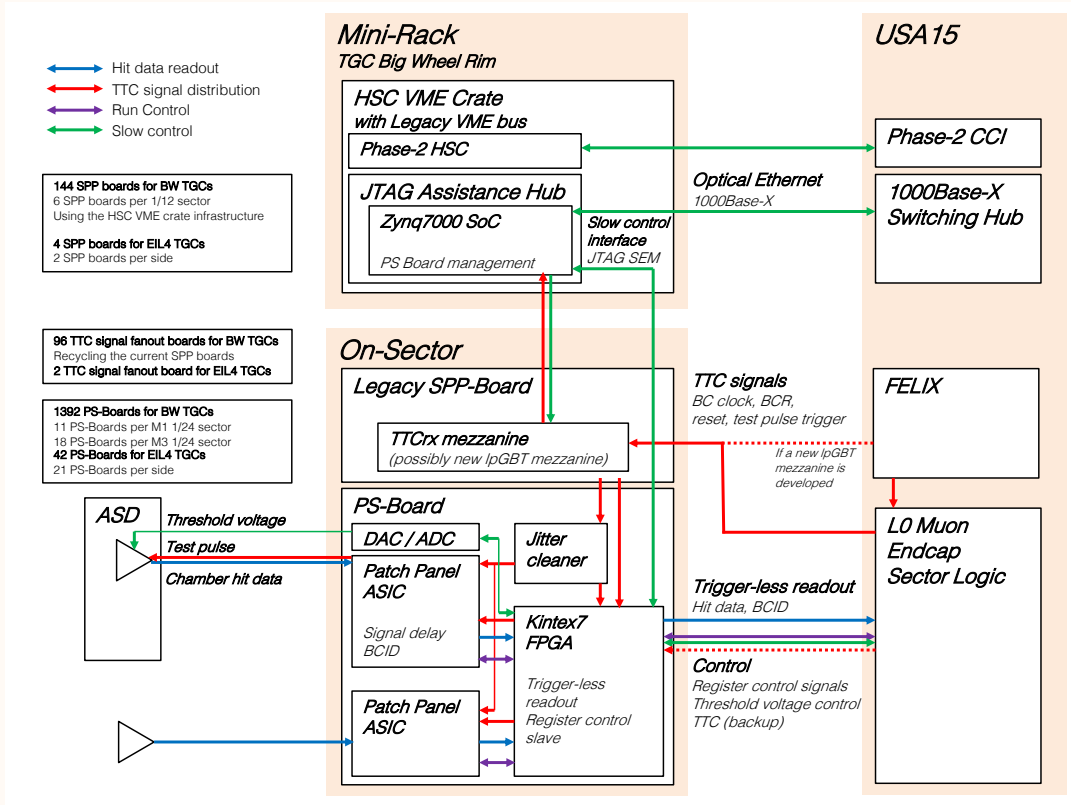
[FYI] Current Status of the Phase-2 Endcap SL ATCA Blade

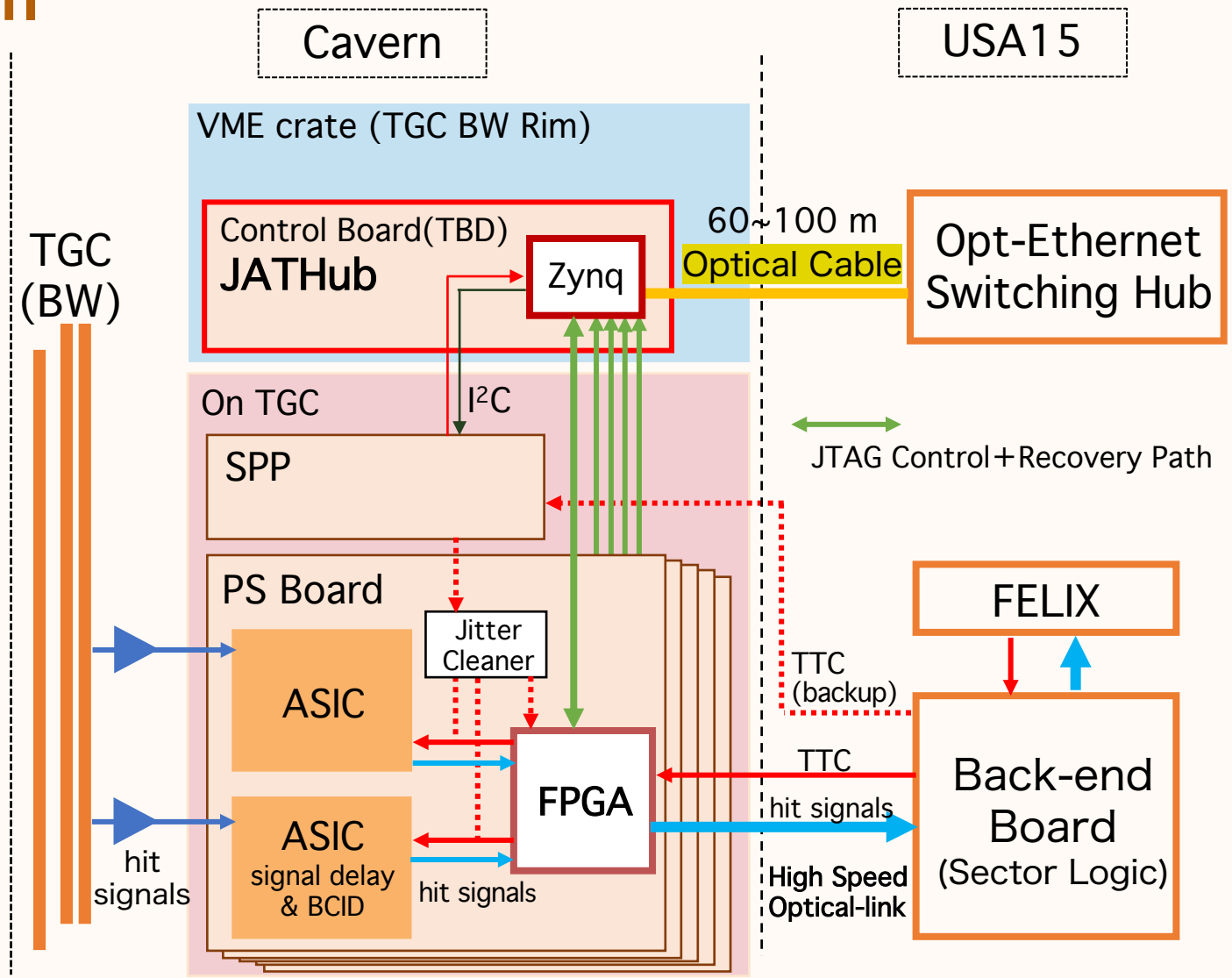
- Phase-2 SL ATCA blade uses Zynq UltraScale+ MPSoC
  - Primary design: Enclustra SoM (Mercury XU5)
- Usage of MPSoC
  - Interface for the ATLAS run control
  - Configuration and monitoring of Virtex UltraScale+ (XCVU13P) on SL
- Phase-2 SL ATCA blade prototype board will be delivered in Autumn 2021
- Demonstration on an evaluation board (XU5 & PE1)
  - Compiled in Petalinux 2019.2
  - Succeeded to build and boot CentOS 7
- Development of firmware to control Virtex FPGA on the SL is in progress



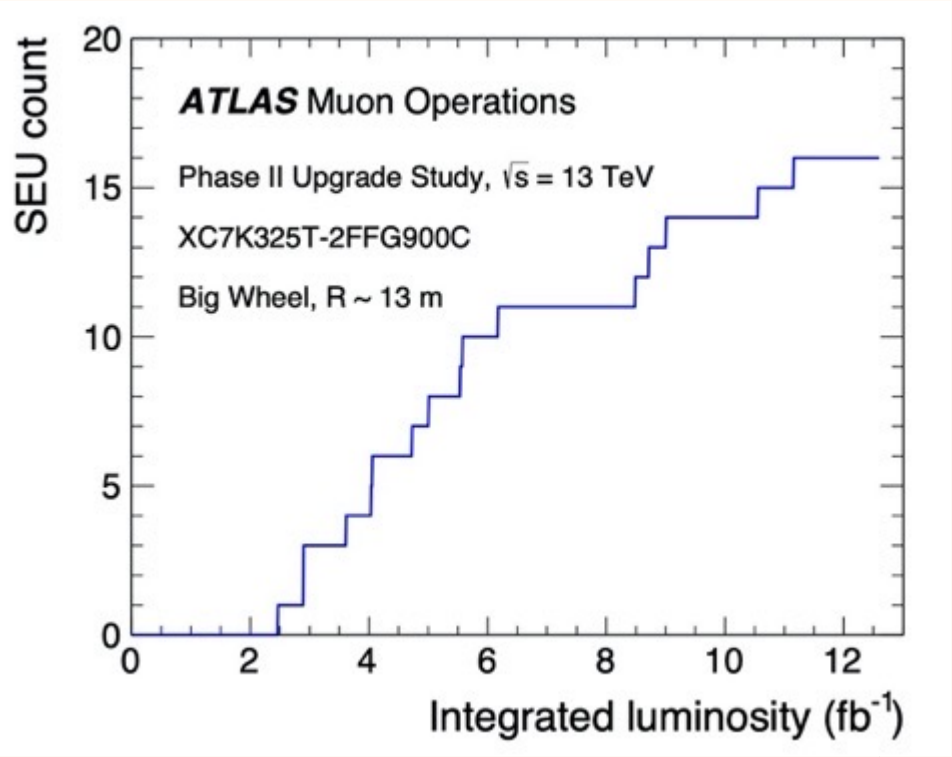
Backup

System of TGC Readout・Trigger Electronics for Phase 2 in Detail





SEU Counts at PS board in Phase 2



Run2 (test result) 165 hours

HL-LHC (calculated) 45 hours

- SEU count test for FPGA
  at the location of PS board in Run 2(2018)
  [Link]ATLAS public results

- Peak Luminosity in Phase 2

  → $7.5\times10^{34}cm^{-2}s^{-1}$

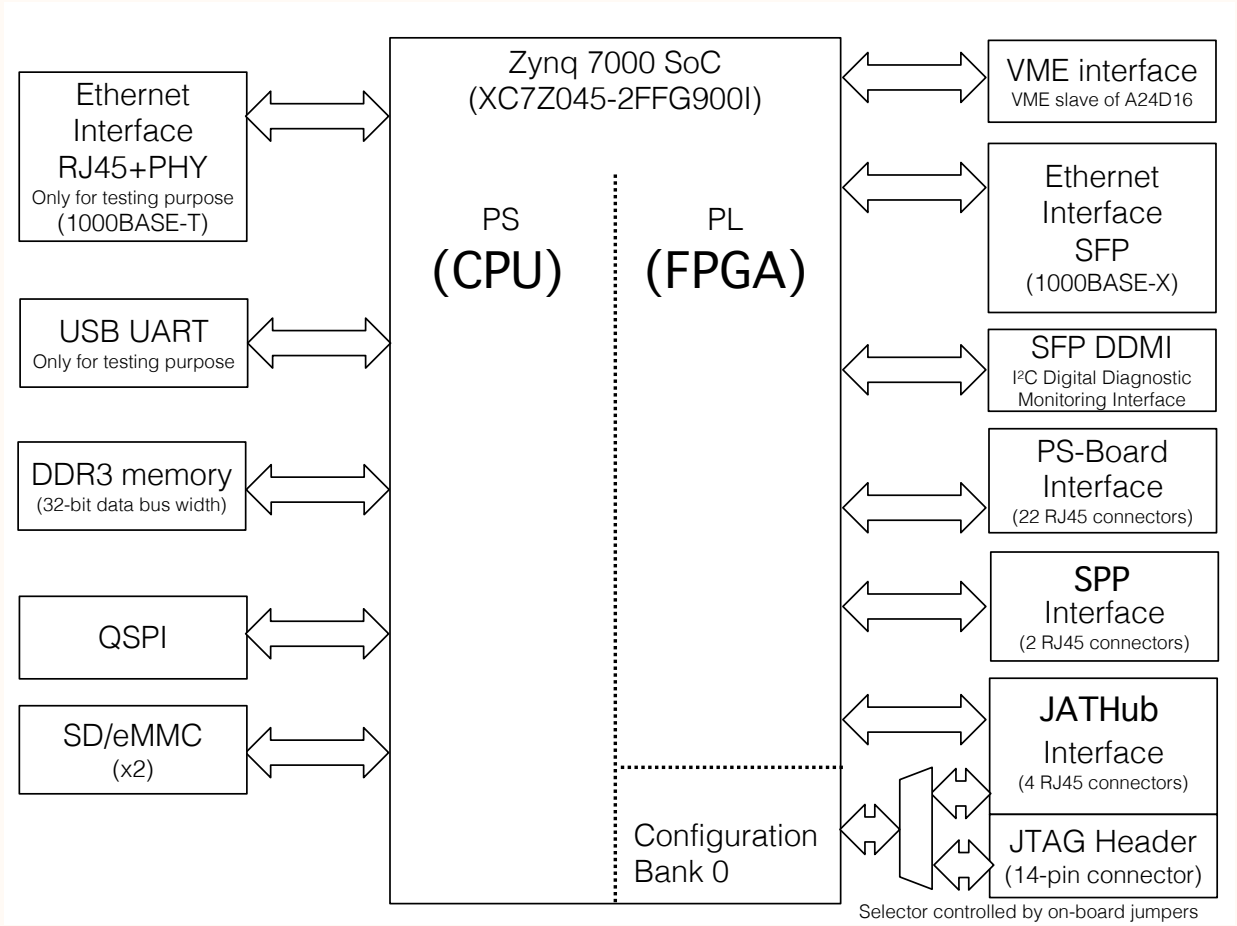
- Frequency of SEU in FPGAs of all PS boards in ATLAS cavern

  →Approximately 1 time per 10 seconds

- [note] Unless 2 or more SEUs are occurred at the same time in the same FPGA, SEM(Soft Error Mitigation) in FPGA will automatically recover the function of FPGA.

JATHub Design around Zynq SoC

QSPI + SD Boot→



←Power &VME Data Path

←Opt-Ethernet

←PS Board × 11

←SPP

←Neighbouring JATHub (Tx & Rx)

Pin Assignment of JATHub RJ45 Ports

PIN ASSIGNMENT on RJ45 for PSBoard(i)

PIN	CN4(A-H),CN5(A-C)
1	PSB-TDO+
2	PSB-TDO-
3	PSB-TDI+
4	PSB-TMS-
5	PSB-TMS+
6	PSB-TDI-
7	PSB-TCK+
8	PSB-TCK-

PIN	CN4(I-P),CN5(G-I)
1	PSB-RECOVERY-REQUEST-B+!
2	PSB-RECOVERY-REQUEST-B-!
3	PSB-MONITORING+
4	PSB-PRGB-*!
5	PSB-PRGB+*!
6	PSB-MONITORING-
7	/PSB-TRANSCEIVER-RESET+*!
8	/PSB-TRANSCEIVER-RESET-*!

PIN ASSIGNMENT on RJ45 for Legacy SPP Board(ii)

PIN	CN5(F)
1	LGCYSPP-SDA-W+
2	LGCYSPP-SDA-W-
3	LGCYSPP-SDA-R+
4	LGCYSPP-SCL-W-
5	LGCYSPP-SCL-W+
6	LGCYSPP-SDA-R-
7	LGCYSPP-SCL-R+
8	LGCYSPP-SCL-R-

PIN	CN5(L)
1	LGCYSPP-TTC-CLK+
2	LGCYSPP-TTC-CLK-
3	LGCYSPP-TTC-BCR+
4	N/A
5	N/A
6	LGCYSPP-TTC-BCR-
7	N/A
8	N/A

PIN ASSIGNMENT on RJ45 to Neighbouring JATHub Board (TX)(iii)

PIN	CN5(D)
1	SPP-TDO+
2	SPP-TDO-
3	SPP-TDI+
4	SPP-TMS-
5	SPP-TMS+
6	SPP-TDI-
7	SPP-TCK+
8	SPP-TCK-

PIN	CN5(J)
1	SPP-RECOVERY-REQUEST-B+!
2	SPP-RECOVERY-REQUEST-B-!
3	SPP-MONITORING+
4	SPP-PRGB-*!
5	SPP-PRGB+*!
6	SPP-MONITORING-
7	/SPP-PORB+*!
8	/SPP-PORB-*!

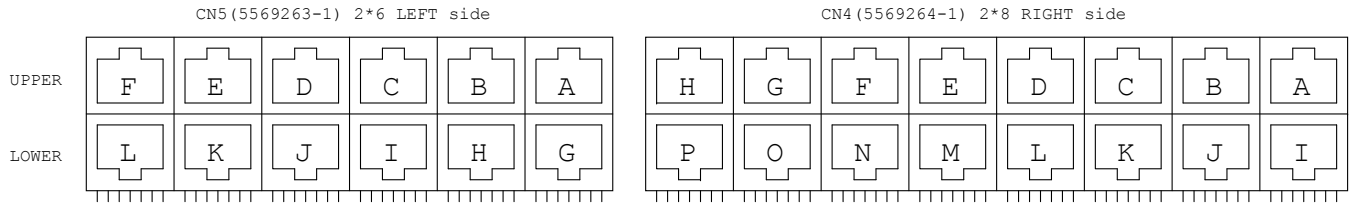
PIN ASSIGNMENT on RJ45 from Neighbouring JATHub Board (RX)(iv)

PIN	CN5(E)
1	SPP-TDO+
2	SPP-TDO-
3	SPP-TDI+
4	SPP-TMS-
5	SPP-TMS+
6	SPP-TDI-
7	SPP-TCK+
8	SPP-TCK-

PIN	CN5(K)
1	SPP-RECOVERY-REQUEST-B+!
2	SPP-RECOVERY-REQUEST-B-!
3	SPP-MONITORING+
4	SPP-PRGB-!
5	SPP-PRGB+!
6	SPP-MONITORING-
7	/SPP-PORB+!
8	/SPP-PORB-!

*:Program_b singals and the reset signals are in high impedance when the Zynq isn't configurated or the JATHub isn't powered on(v)
!:Negative Logic (Active Low)(vi)
All signals driven by transmitter DS90LV047ATMTCX/NOPB have fail safe function; default high impedance(vii)
All signals received by receiver SN65LVDT348PWR have fail safe function; default high(viii)

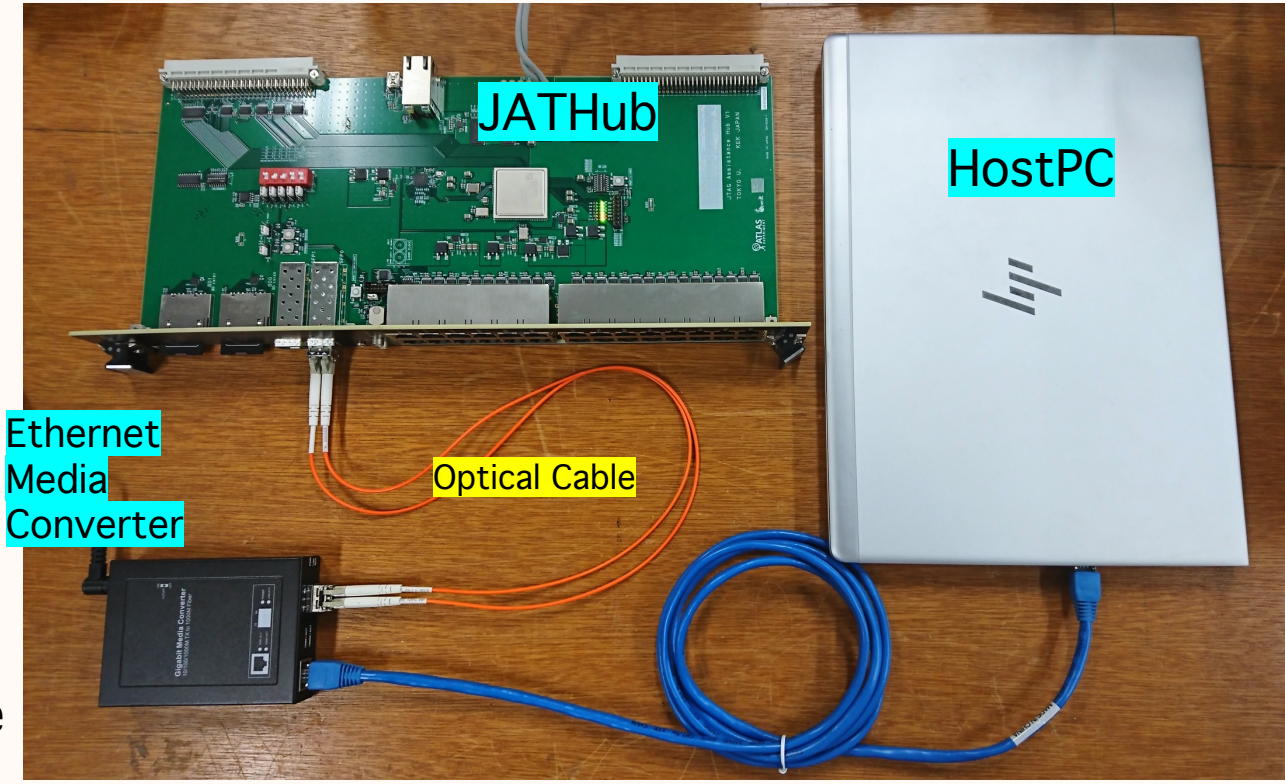
PORT ASSIGNMENT of RJ45 Multi-Ports(ix)



1000Base-X Ethernet Test

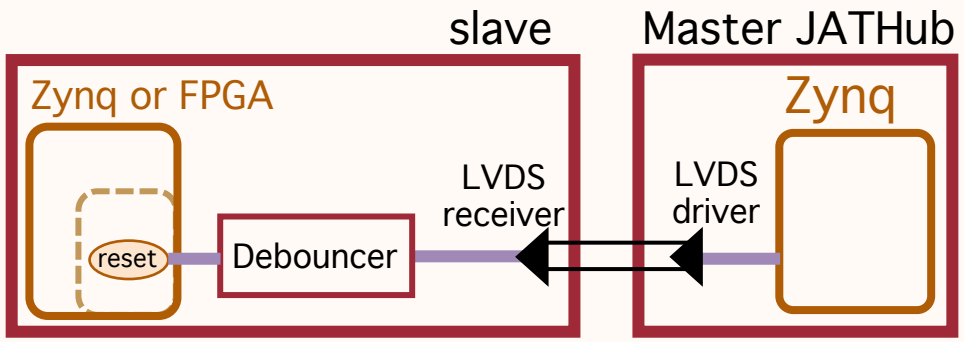
- Implemented PHY in FPGA part of Zynq,
  and connected CPU and GTX transceiver
  (which connects to SFP module)
  → Enable to communicate with
  Zynq by optical cables

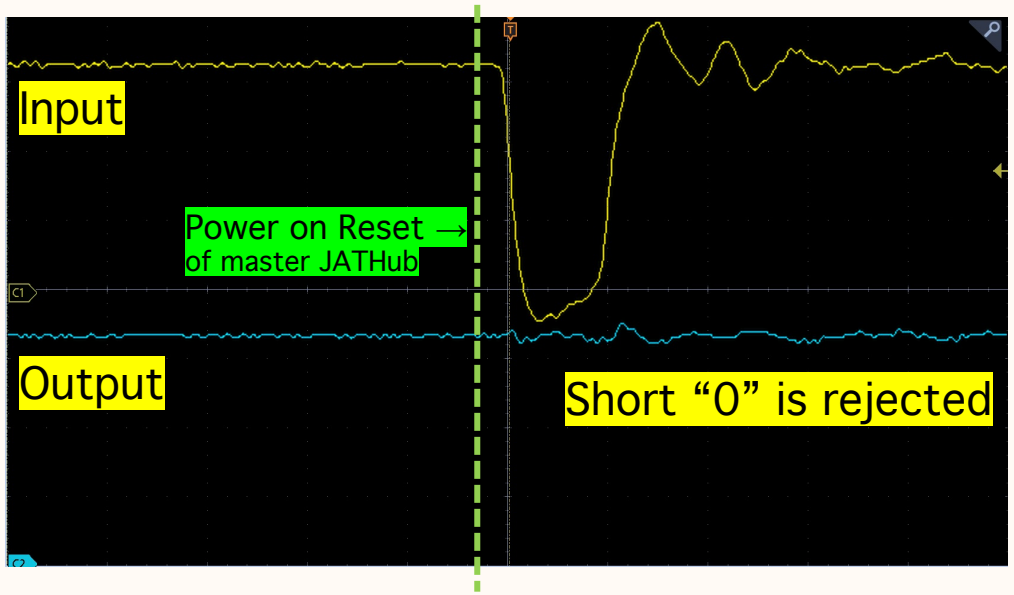
- Tested Opt-Ethernet with the JATHub prototype
  - Connected Host PC and JATHub with optical cable
  - Succeeded to establish ethernet network
    - Successfully sent PING and SSH



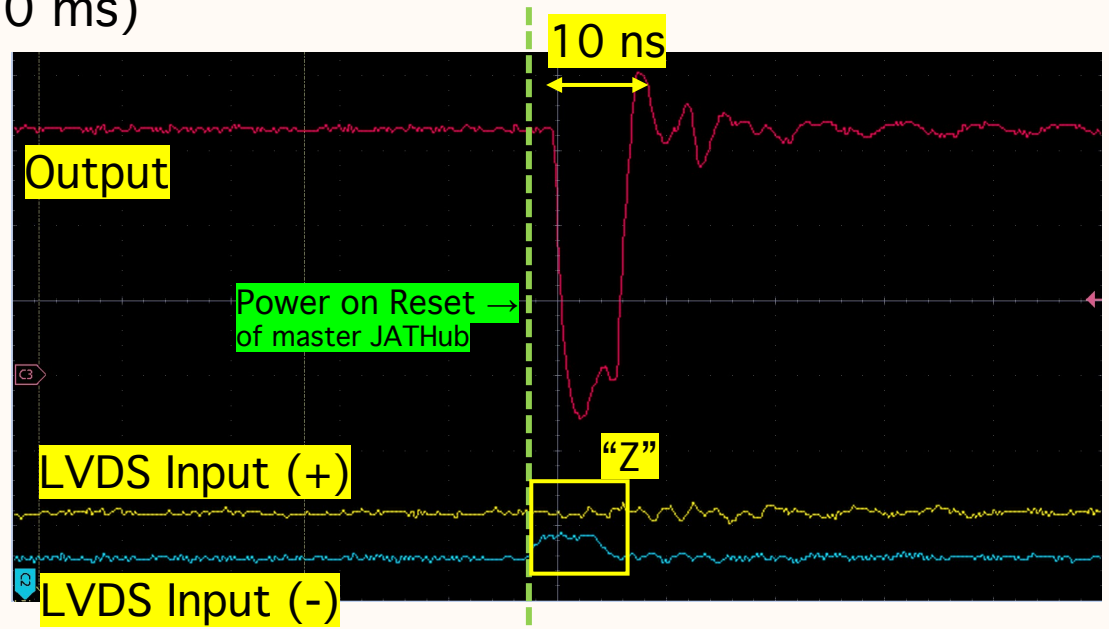
② Stable handling of the reset signal

- Reset signal needs to be “1” in idle state
  while master JATHub handles reset signals(active-low) of slave modules
- LVDS receiver IC issued short “0” when input signal became high impedance (“Z”) by Power-on-Reset of the master JATHub
  → Debouncer IC of the slave module
  rejects unwanted short “0” reset signals (less than 80 ms)





I/O signals of debouncer IC (slave)

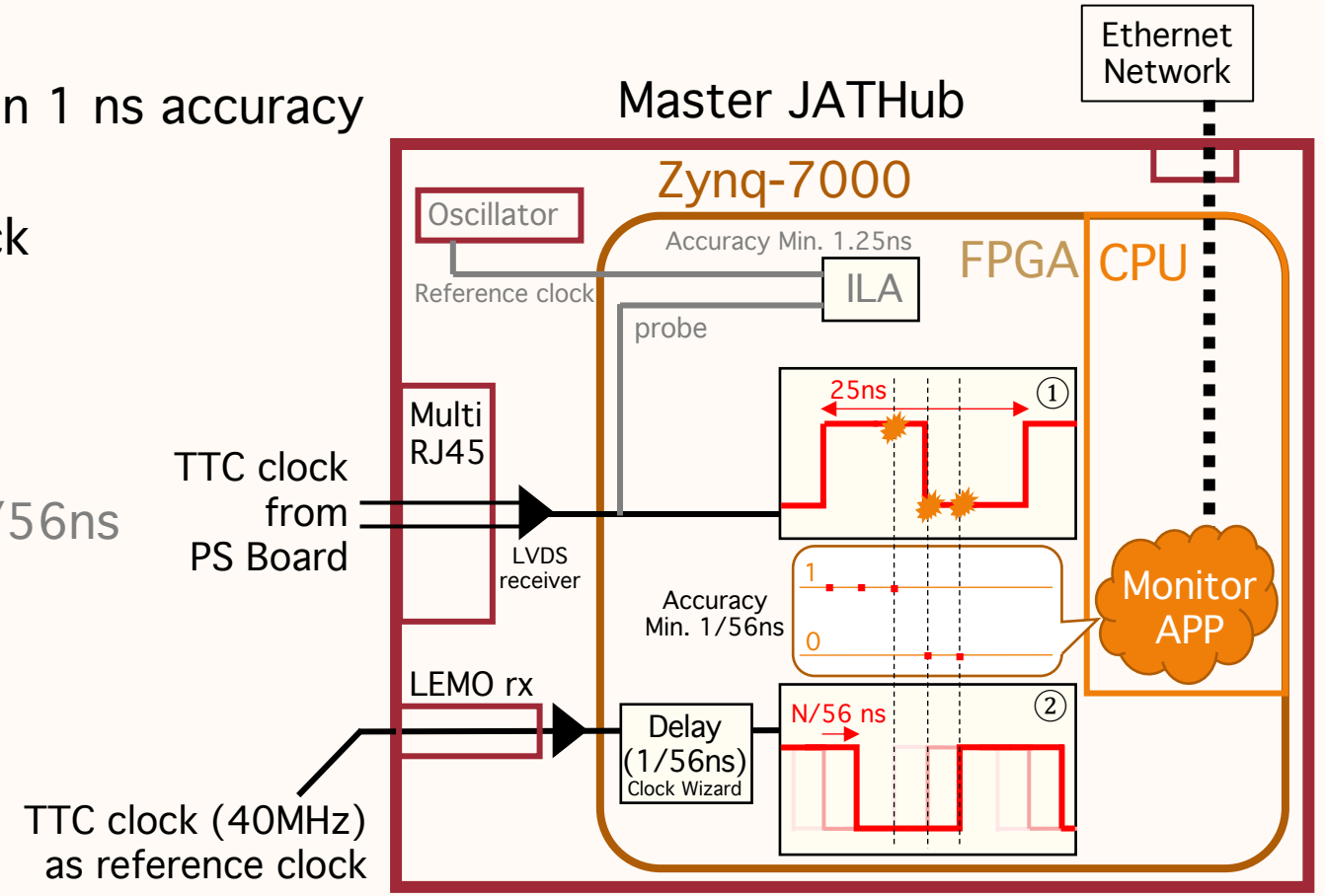


I/O signals of LVDS receiver IC (slave)

③ Monitoring LHC Clock Phase of FE Board

- need to synchronize LHC clock phases
  on all the FE Boards in the cavern with less than 1 ns accuracy

- Implemented firmware to monitor the LHC clock
  with 1/56 ns accuracy
  - Read TTC clock from PS Board
    at rising edge of reference TTC clock
  - Shift phase of the reference TTC clock by 1/56ns
    and read the clock from PS Board again
    (repeat until ref. clk phase shifted by 25ns)
  - Enable to read max. 11 TTC clocks
    from PS Boards at the same time



→ **Succeeded to monitor TTC clock**