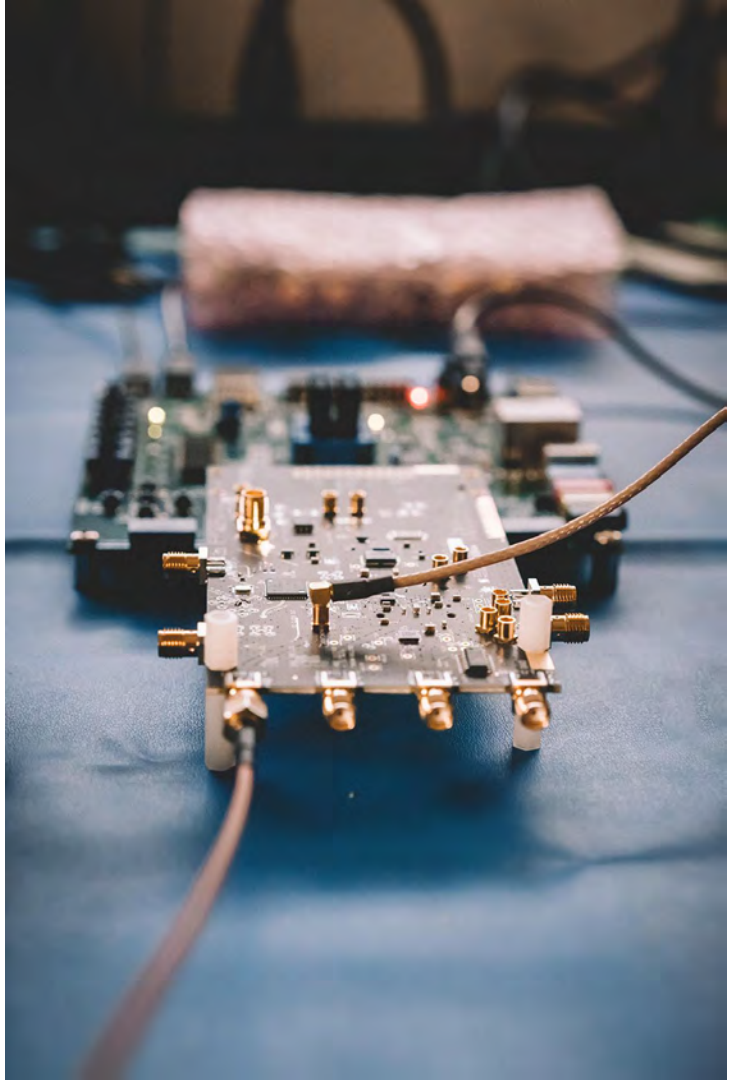

NALU SCIENTIFIC
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Waveform Digitizing and Processing Front-end Microelectronics for large Experiments

June 8, 2021
Isar Mostafanezhad, Ph.D.
Founder and CEO at Nalu Scientific LLC

Work partially funded by US DOE SBIR Grants:

DE-SC0015231, DE-SC0017833, DE-SC0020457

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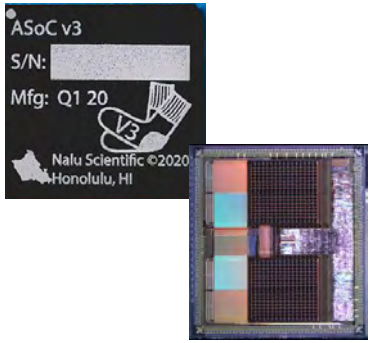
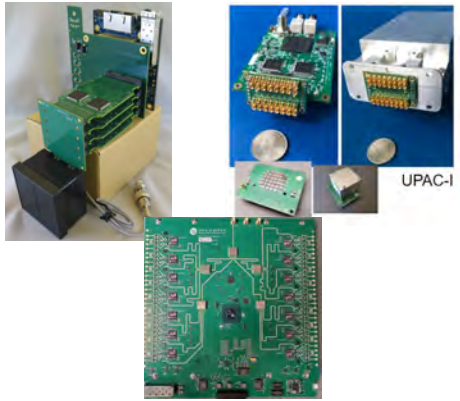
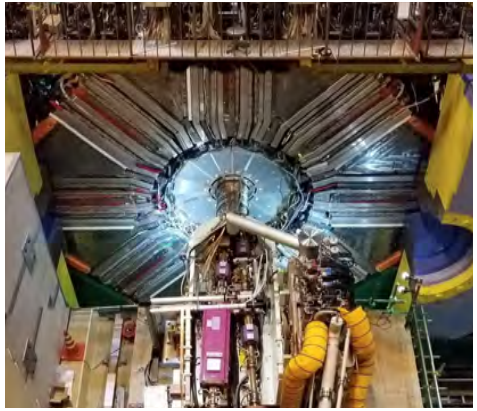
WAVEFORM DIGITIZER SoCs
FOR PRECISE TIME OF FLIGHT ESTIMATION







1. Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

2. Integration:

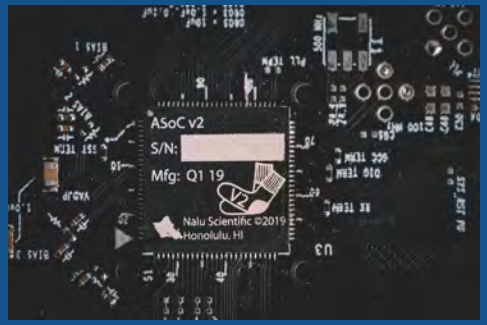
- SiPM
- M/A PMTs
- LAPPD
- Detector arrays

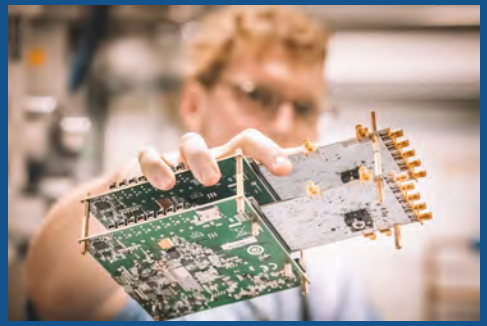
3a. Main application:

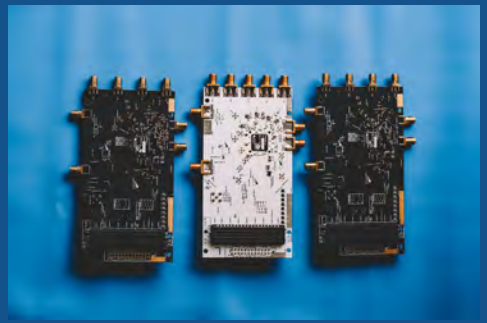
- NP/HEP experiments
- Astro particle physics

3b. Other applications:

- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging







ABOUT NALU SCIENTIFIC

Fast Growing Startup in Honolulu, Hawai'i

- Located at the Manoa Innovation Center
- Over $11M in committed funding, 18 staff members
- Access to advanced design tools
- Rapid prototyping and testing lab

Scientific Expertise

- HEP/NP particle detection and tracking
- Radiation detection
- Readout electronics for Nuclear & Particle Physics detectors

Technical Expertise

- Analog + digital System-on-Chip (SoC)
- Field Programmable Gate Arrays (FPGA)
- Complex multi-layer Printed Circuit Boards (PCBs)

Nalu = 'wave' in native Hawaiian language

Funding, Collaboration and Workforce Development

FY16-21

✔ **$11 M Secured by Nalu**
- ✔ 9x SBIR Phase I
- ✔ 6x SBIR Phase II
- ✔ Various matching grants
- ✔ Misc. contracts

FY16-20

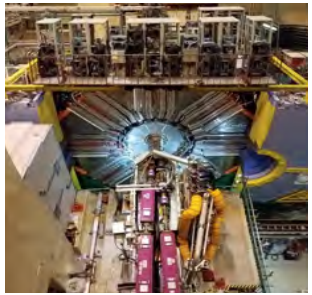
✔ **$1.2M Sponsored Research**
- ✔ University of Hawaii
- ✔ National Labs
- ✔ 4x post docs
- ✔ 4x graduate students
- ✔ Misc. materials and supplies

2x MS and 2x PhDs had their first jobs at Nalu Scientific.

FY21-23

✔ **New possibilities:**
- ✔ New tech-dev based on capabilities
- ✔ Sensor integration
- ✔ Custom design
- ✔ New partnerships

Why Hawaii?
- Strategic location - Asia <> US
- University of Hawaii
- Greater impact on State
- “Hawaii Brand”
- Retain local expertise



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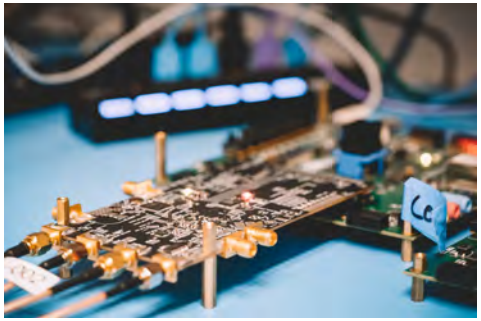
Current SoC-ASIC Projects

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-3	0.6	2k	64	80-120	May'21
AARDVARC	8-14	2.5	32k	4	4	Rev 3 avail
AODS	1-2	1	16k	1-4	100-200	Rev 1 avail
STRAWZ	5	2	2k	64	10	Dec'22



- **ASoC**: Analog to digital converter System-on-Chip
- **HDSoC**: SiPM specialized readout chip with bias and control
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option
- **STRAWZ:** Streaming Autonomous Waveform-digitizer with Zero-suppression

Work funded by DOE SBIRs. Chips designed using commercial EDA tools.
University of Hawaii as subcontractor.

ASoC V3 DESIGN DETAILS

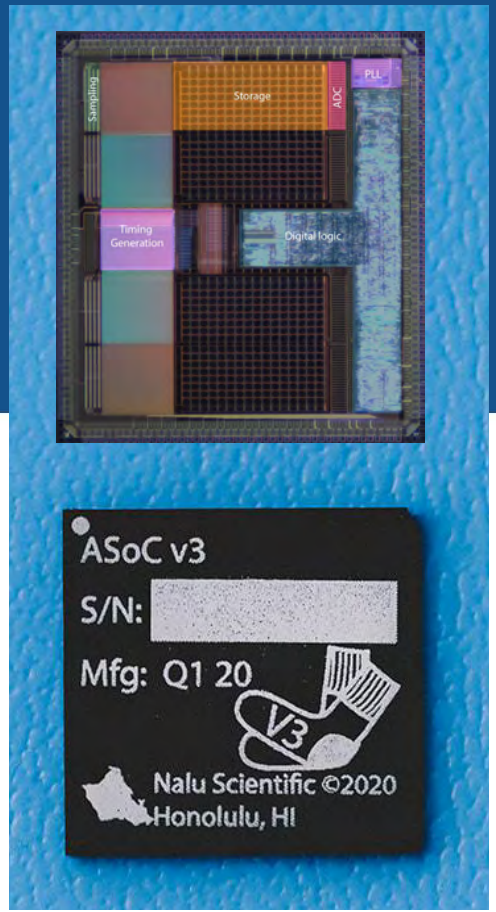
Compact, high performance waveform digitizer

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size

Parameter	Spec
Sample rate	2.4-3.6GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Number of ADC bits	12 bits
Supply Voltage	2.5V
RMS noise	~1.5 mV
Digital Clock frequency	25MHz
Timing resolution	<25ps (see below for details)
Power	120mW/channel
Analog Bandwidth	850MHz
Serial interface	Up to 500 Mb/s***

- Calibration memory access
- PLL on chip
- Isolated analog/digital voltage rings
- Serial interface
- Self triggering
- Completed DOE Phase II SBIR
  - Eval cards avail
  - Custom boards under dev

IEEE NSS 2021



NaluScope Common Software and GUI

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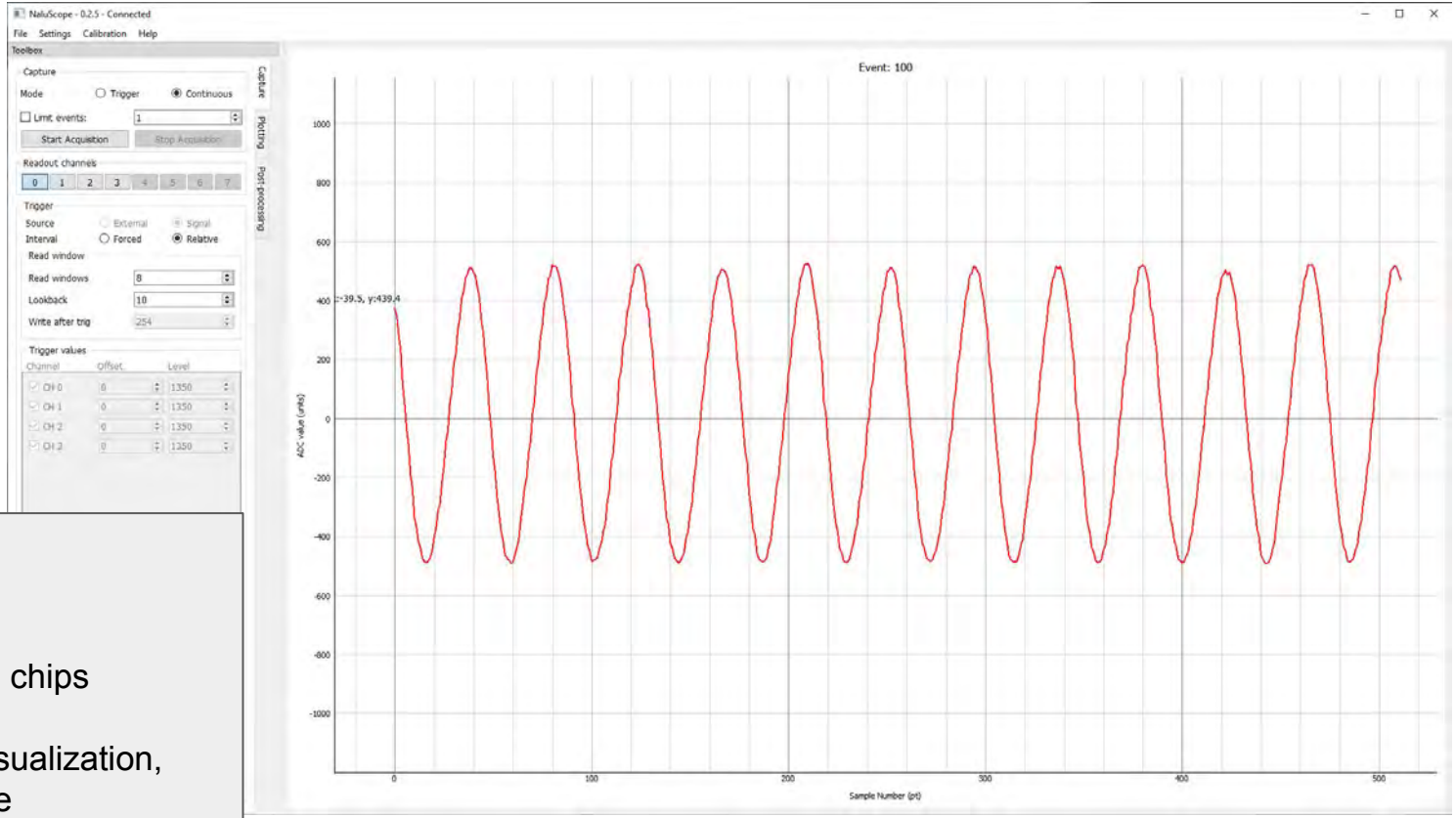

- Windows/Linux PC
- USB interface
- GUI, CLI interfaces
- Common to all Nalu chips
- DAQ configuration
- Data exploration, visualization, curation and storage

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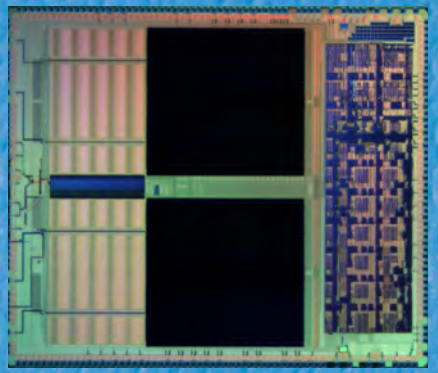
AARDVARC V3 DESIGN DETAILS

Compact, high performance waveform digitizer

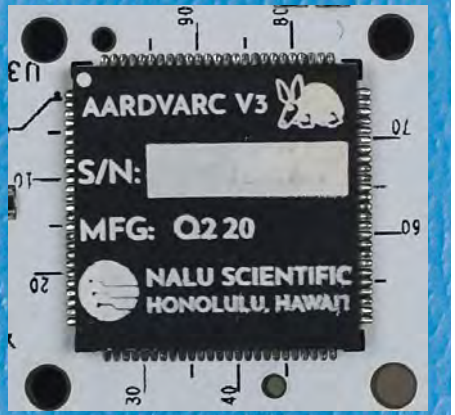
- High performance digitizer: 10+ Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size



Parameter	Spec
Sampling Rate	10-14 GSa/s
ABW	> 1GHz
Depth	32k Sa
Trigger Buffer	~3 us*
Deadtime	0**
Channels	4
Supply/Range	1.2V/0.3-0.9V
ADC bits	12
Timing accuracy	<5ps (@13 GSa/s)
Technology	130 nm CMOS
Power	80mW/ch

- On chip calibration
- On chip PLL
- On chip feature extraction
- Isolated analog/digital voltage rings
- Serial interface
- Funded DOE Phase IIA SBIR

IEEE NSS 2021

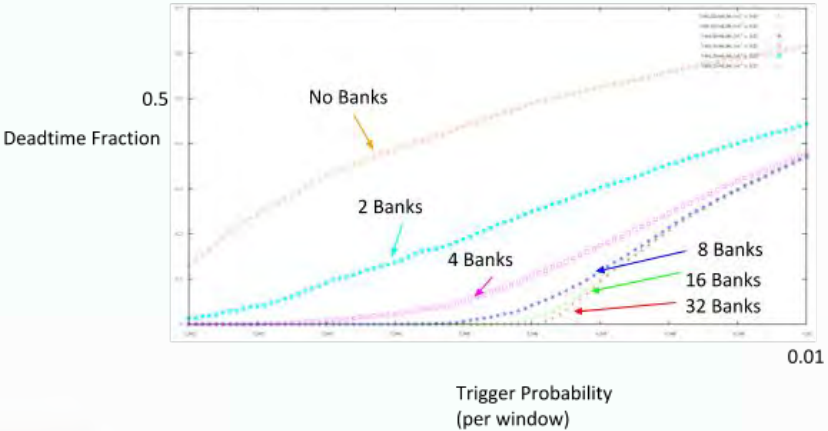


AARDVARC v3

Simulation of deadtime-less operation

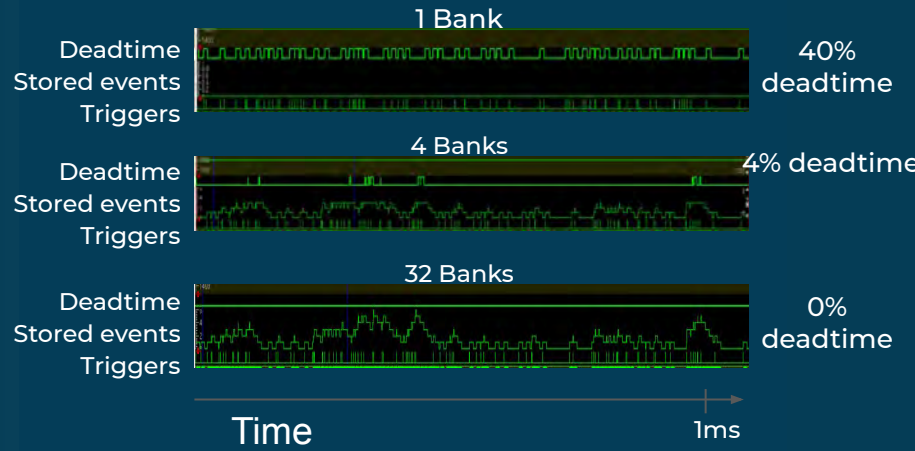
Banking system:

- Storage array flexibly partitioned
- Handles multiple hits
- Reduce deadtime



Simulation showing 0 deadtime growing asymptotically with the number of banks for average Poisson rates below maximum rate. Trigger probability = raw hit per channel.

- Logic level simulations with real estimates for digitization/readout (full 4 channels readout, Rate of 125kHz)



NALU SCIENTIFIC
ENABLING INNOVATION

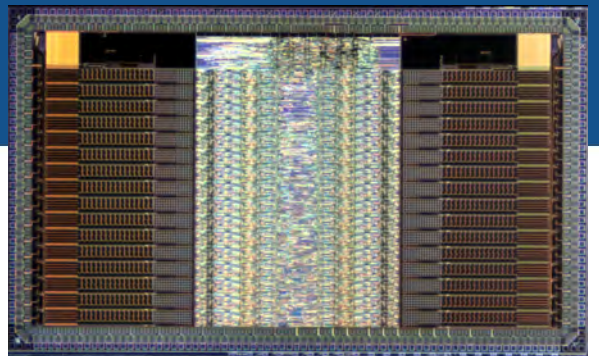
HDSoC V1 DESIGN DETAILS

High density waveform digitizer with dead-timeless readout

- High Density: 64 channels
- Highly integrated, SiPM gain + bias
- Commercially available, low cost CMOS

Parameter	Spec
Sampling Rate	1-2 GSa/s
ABW	> 600MHz
Depth	2k Sa
Trigger Buffer	~3 us*
Deadtime	0**
Channels	64
Supply/Range	2.5
ADC bits	12
Timing accuracy	80-120ps
Technology	250 nm CMOS
Power	TBD

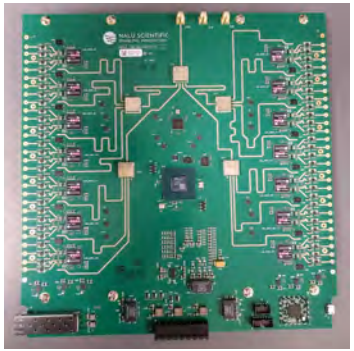
- On chip calibration
- Serial interface
- On chip feature extraction
- Virtually dead-timeless
- 32 ch proto chip fabricated
- Phase II SBIR awaiting award
- Next steps: packaging and eval



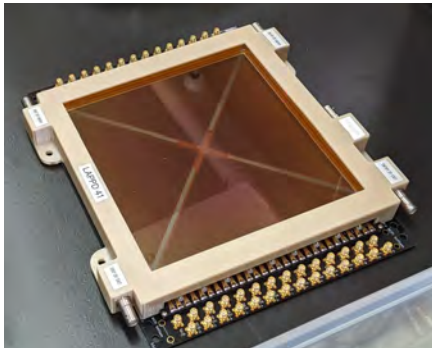
HDSoC v1 die shot

** Simulated Up to 240 KHz / ch with single serial link using on-chip self trigger and feature extraction.
Up to 400 kHz / ch with additional serial links.

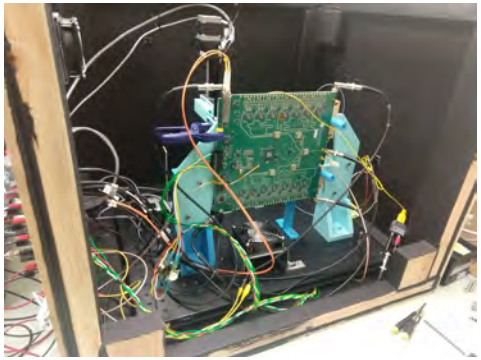
Integration efforts - HIPeR



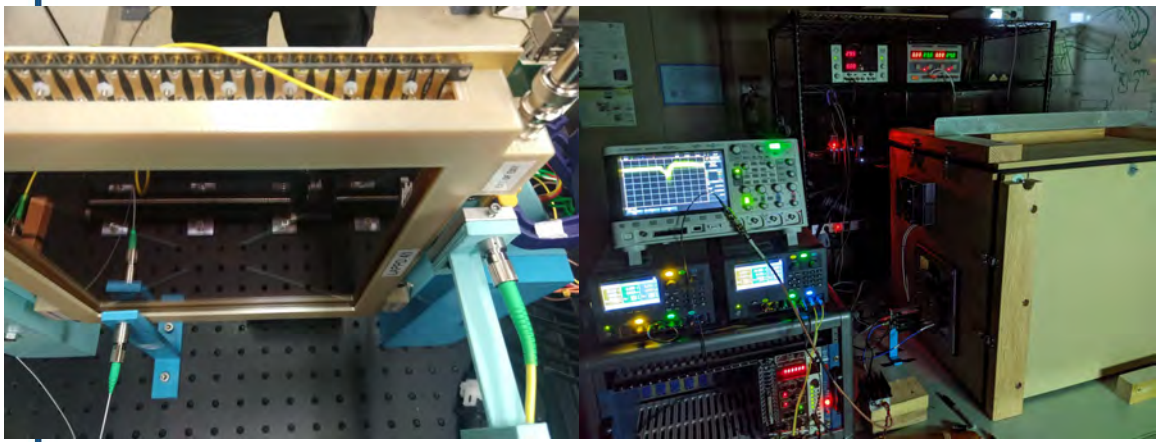
AARDVARC based readout

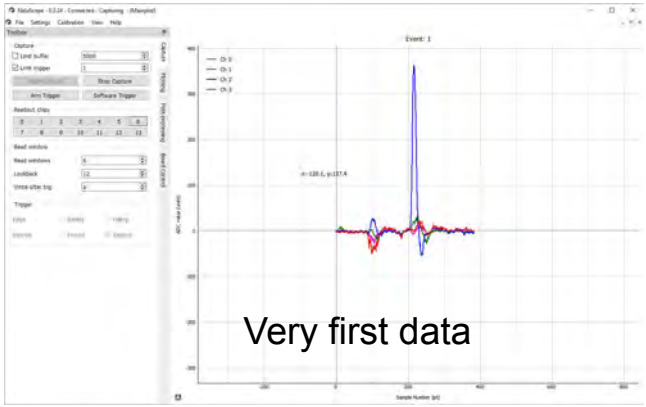


Incom's Gen 1 LAPPD



Integration and testing (UH)





Nalu Scientific Phase I SBIR in collaboration with Incom and University of Hawaii.

Dead-timeless operation

- **Multi-bank switched capacitor array:**
  - Older versions of chips (ASoC, AARDVARC)
  - Long internal analog memory (storage)
  - Capable of self triggering
  - Suitable for long trigger delays (3-5 us)
  - Large die size
  - **ASoC V3 may be able to readout up to ~100 kHz of input rate without deadtime (estimated).**
- **Virtual analog memory:**
  - New lines of chips (HDSoC, STRAWZ)
  - Unlimited virtual depth (up to a certain rate)
  - Small die size, lower power
  - Dead-timeless up to a certain rate, designed with self-triggering in mind
  - Suitable for streaming mode readout
  - Feature extraction and on-chip data reduction
  - Estimated 240-400 kHz rate handling

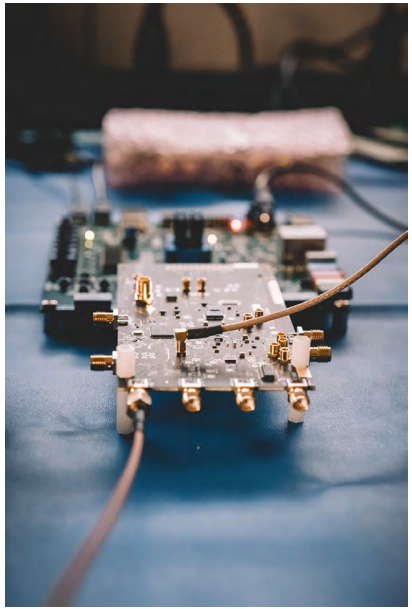
How can Nalu contribute?

Project	Frequency (GHz)	Buffer Length	Channels	Timing Res. (ps)	Rate handling	TRL	Suitable for	Detectors
ASoC	3-5	16k	4	35	~100kHz	High	Low density, precision timing, flexible board integration	
HDSoC	1-3	2k	64	80-120	~240, 400 kHz	rev1	High density SiPM, MA-PMT	
AARDVARC	8-14	32k	4	4	~125kHz	Med	Precision timing, low density	
STRAWZ	5	2k	64	10	~500 kHz	Low	High density, precision timing	
AODS	1-2	16k	1-4	100-200		Med	High dynamic range	

- **ASIC Tech** shovel ready and likely to around for next 10 years (F. Barbosa talk earlier)
- **Knowledgebase** created through significant investment from DOE SBIR program.
- **Experiment in mind** through high levels of integration: clock, calibration, memory
- **Commercial grade** design tools used to create commercial chips
- **Teaming** with scientists on EIC-PID readout, white papers, etc
- **Strategic partnerships** with system integrators to connect chips to DAQs
- **Working relationships** with U. of Hawaii and several National Labs

NEED A SUMMARY PAGE, INCLUDING "WHERE WE ARE GOING FROM HERE"

Summary



- Nalu Scientific portfolio of FE/digitizer electronics
  - Specialized for NP/HEP experiment readout
  - High integration (clock, memory, calibration)
  - Packaged chips and eval cards available
  - Additional testing under way including irradiation
- Expertise:
  - NP/HEP electronics/FW development
  - Advanced mixed signal ASIC design
  - A variety of detector electronics design
- Funding:
  - SBIRs: covers costly chip development
  - Trade studies: initial assessment
  - Custom design contracts: Implementing new packaging and PCB designs
- Next steps:
  - Continue chip+PCB development
  - Continue engagement with experiments in order to tailor the designs to evolving experiment needs
  - New integration efforts under way.
  - Eval boards available for testing

ACKNOWLEDGEMENTS

US Department of Energy Office of Science

Hawaii Technology Development Corporation (HTDC)

University of Hawai'i at Manoa Department of Physics

Backup