System-on-Chip in Accelerators and Technology Sector

System On Chip Workshop, 7-11 June 21, CERN

Mamta Shukla, BE-CEM-EDL

Acknowledgements: D.Bett, K. Blantos, A. Boccardi, D.Cobas, G.Daniluk, I.Degl'Innocenti, E.Gousiou,G.Hagmann, M.Lipinski, P. Peronnard, H.Sandberg, J.Serrano, A.Spierer, J.Storey, F.Vaga, T.Wlostowski (CERN)
P. Jansweijer(NIKHEF)

Outline

- SoC in Accelerator and Technology Sector
- SoC based Projects in A&T Sector
  - White Rabbit
    - Switch v4
    - Nodes - SPEC7, SPEXI7
  - Fast Interlock Detection System
  - Distributed I/O Tier
  - Beam Control System for SPS LLRF
  - HL-Beam Position Monitoring
  - Beam Gas Ionization
- Requirements
- Efforts

Outline

- **SoC in Accelerator and Technology Sector**

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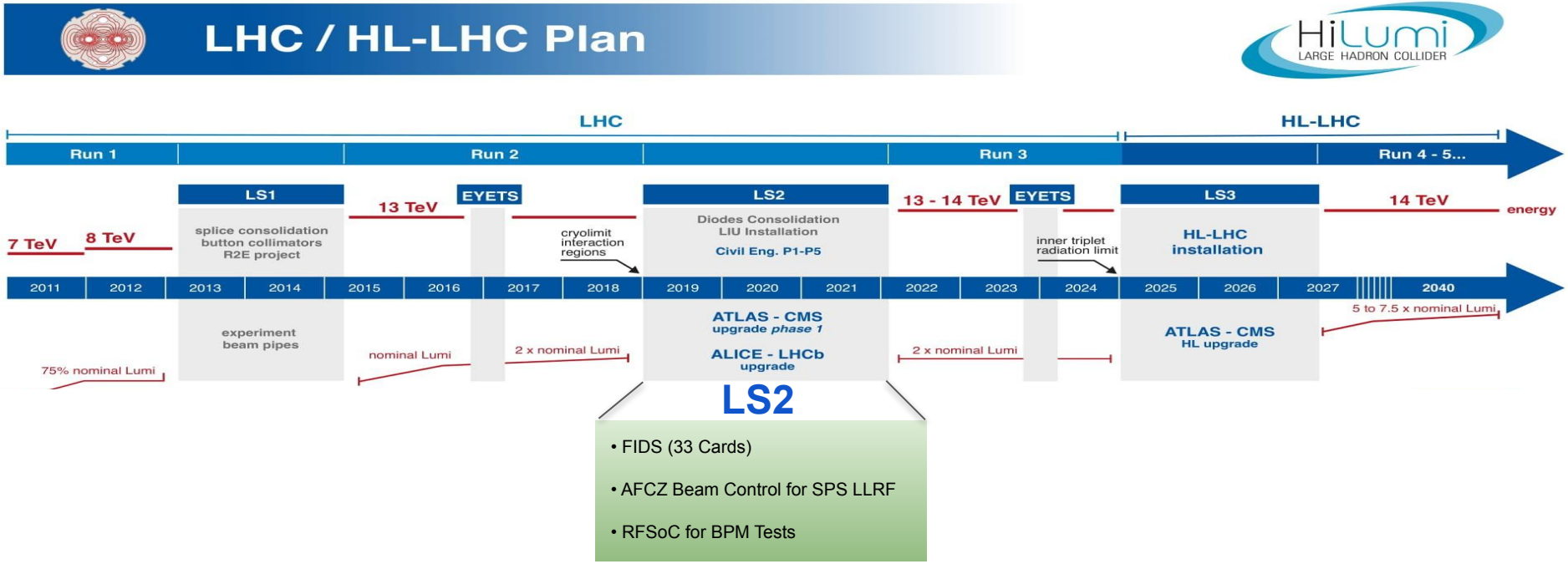
Overview

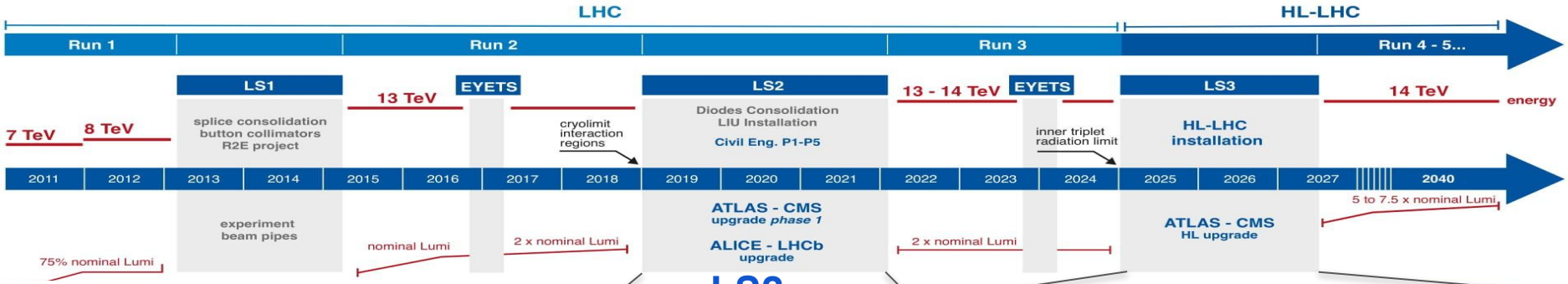


LS2

- FIDS (33 Cards)
- AFCZ Beam Control for SPS LLRF
- RFSoC for BPM Tests

Overview

LHC / HL-LHC Plan



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LS3

- Distributed I/O Tier
- AFCZ Beam Control for SPS LLRF
- FIDS(33 More cards)
- SPEXI7 for SaMBuCA project for LHC Collimators Upgrade
- White Rabbit Switch 4
- RFSoC for BPM
- BGI Processing System

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- SoC in Accelerator and Technology Sector
- **SoC based Projects in A&T Sector**
  - **White Rabbit**
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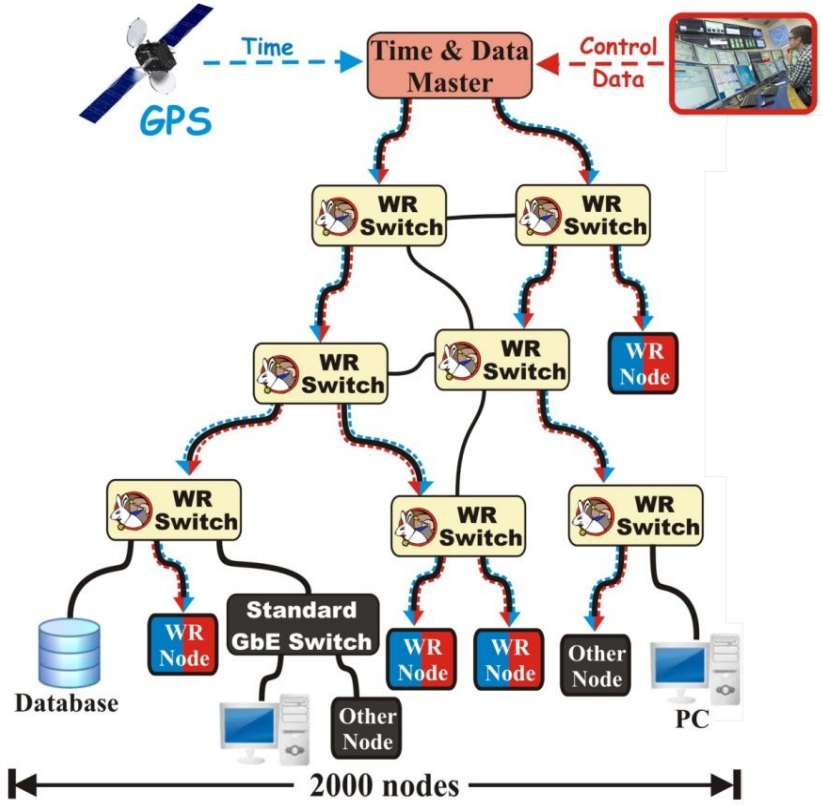
White Rabbit

- CERN and GSI initiative for control and timing
- Based on well-established standards
  - Ethernet (IEEE 802.3)
  - Bridged Local Area Network (IEEE 802.1Q)
  - Precision Time Protocol (IEEE 1588)



Courtesy: M.Lipinski, J.Serrano, G.Daniluk, T.Wlostowski

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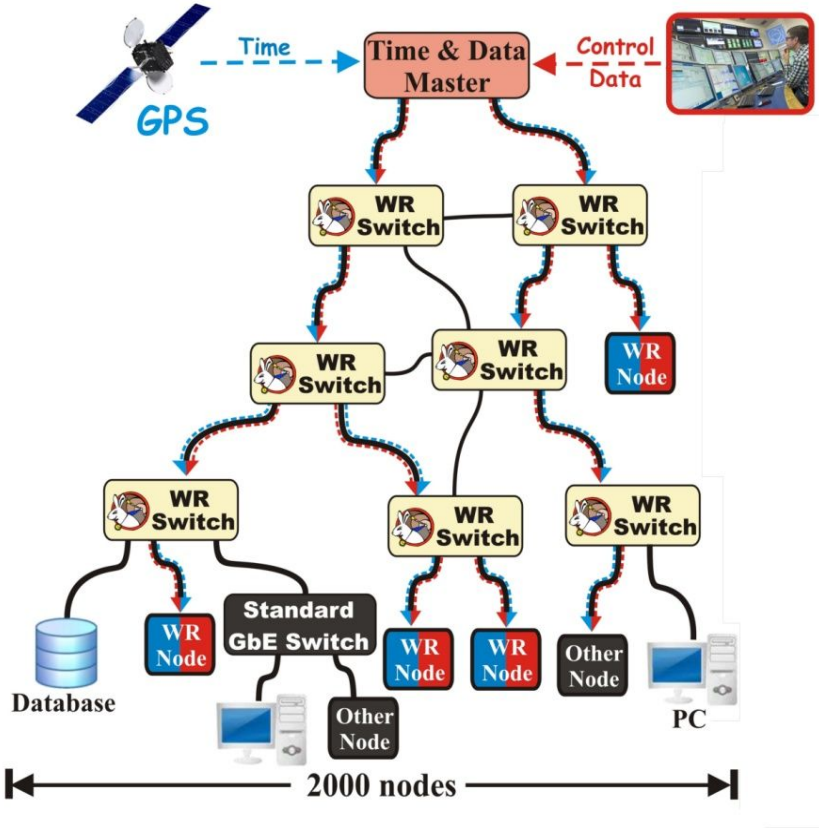
  - Sub-ns synchronisation (included in IEEE 1588)
  - Deterministic data transfer



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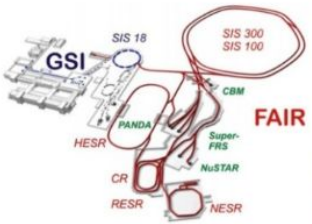
  - Deterministic data transfer
- Open source and commercially available
- Many applications worldwide

CERN & GSI Accelerator Facilities



German Stock Exchange

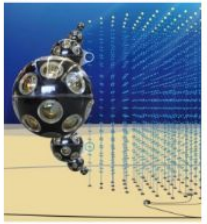
National Time Labs (NL, FI, FR, US, UK, IT)

MIKES
NPL National Physical Laboratory
VSL Dutch Metrology Institute
INRiM Istituto Nazionale di Ricerca Metrologica
l'Observatoire de Paris SYRTE
NIST National Institute of Standards and Technology

European Space Agency for Galileo

Large High Altitude Air Shower Observatory

Cubic Kilometre Neutrino Telescope



Deutsche Telekom

Telecommunication for High Accuracy Time Dissemination

https://ohwr.org/project/white-rabbit/wikis/home

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Introduction to White Rabbit - M.Lipinski, G.Daniluk, BE-Seminar, 2019

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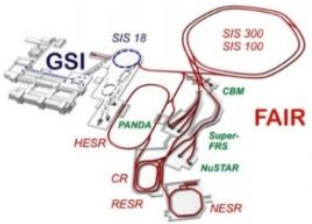

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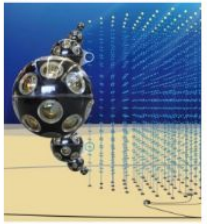

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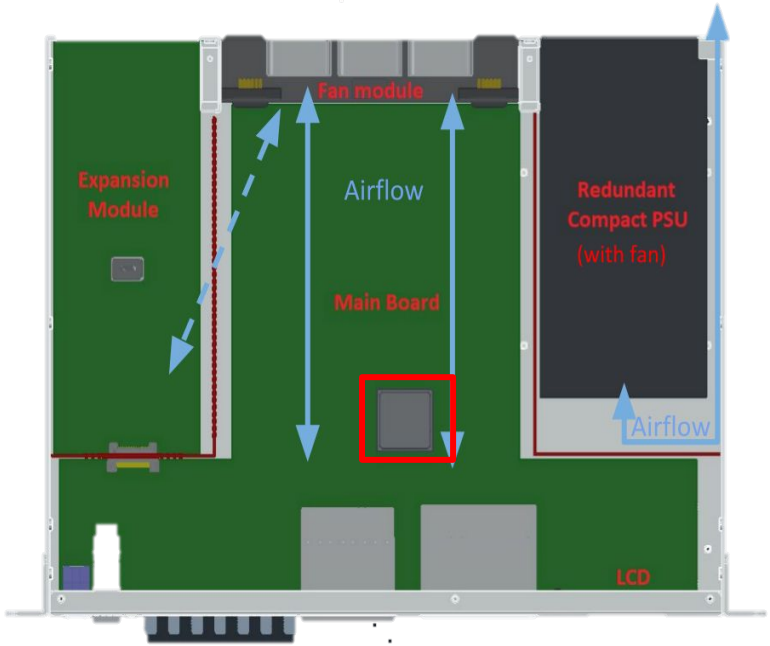
White Rabbit Switch

- It is a fully compliant Ethernet Switch that provides high accuracy synchronization and deterministic communication in an Ethernet-based network.

- **Choice of SoC**:
  - **Advances WR technology**
    - Newest Xilinx MPSoC
    - Sufficient FPGA resources for new features
    - Support for 10 Gbps and higher speeds
    - Extensible to accommodate new applications and improvements

  - **Ensures high reliability**
    - Redundant elements
    - Enough FPGA resources to implement reliability features

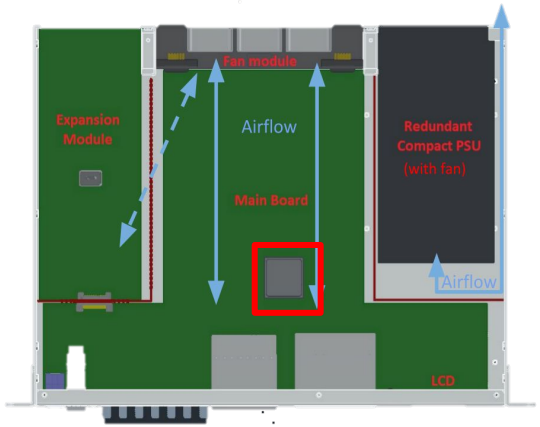


https://ohwr.org/project/wr-switch-hw-v4/wikis/home

Courtesy: M.Lipinski

White Rabbit Switch

- Zynq Ultrascale+ SoC with support for up to 32.75 Gbps
- **PL**: SFP interface, White Rabbit PTP core supports upto 24 ports
- **PS**:
  - SNMP and diagnostics
  - Embedded Linux



White Rabbit Switch Architecture

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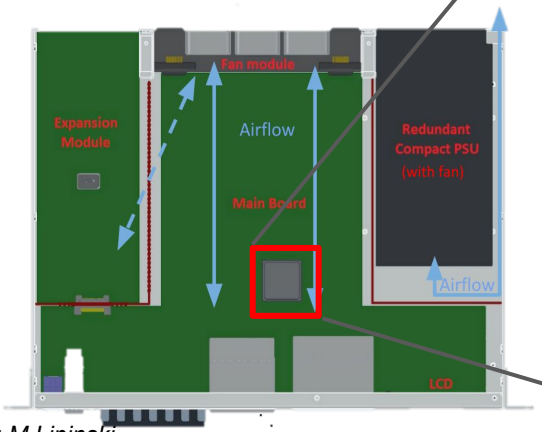

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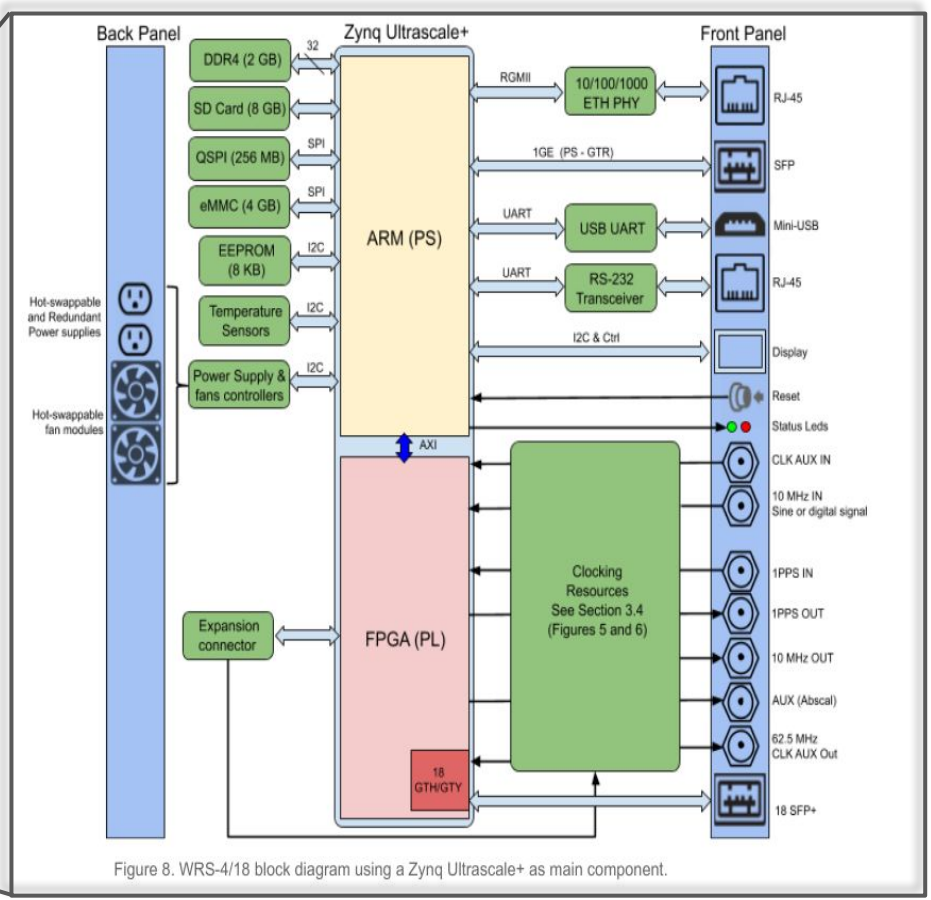
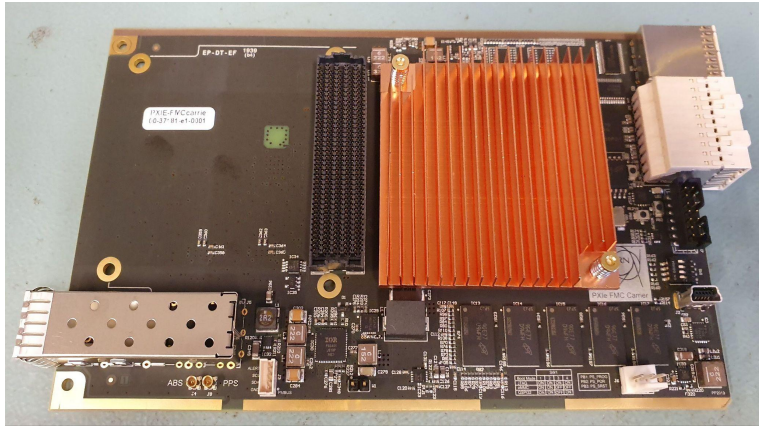


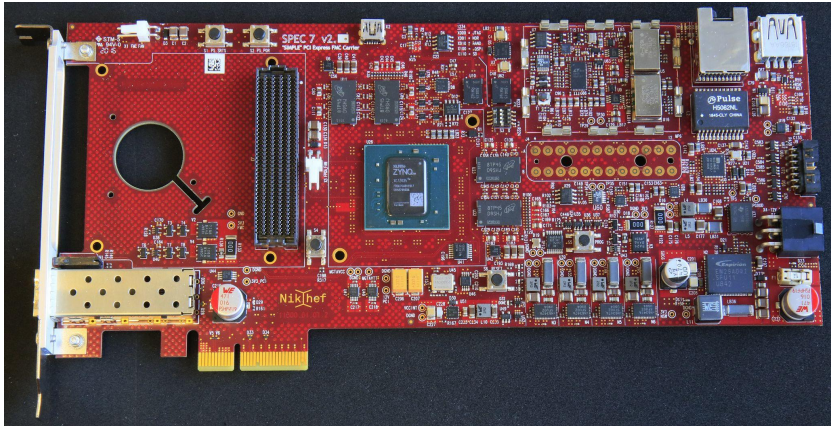
Figure 8. WRS-4/18 block diagram using a Zynq Ultrascale+ as main component.

White Rabbit Nodes

Different form factors (**PXIe, PCIe, CompactPCI**) and SoC on the nodes; hosted in FECs



Simple PXI Express Carrier 7(SPEXI7)



Simple PCI Express Carrier 7 (SPEC7)

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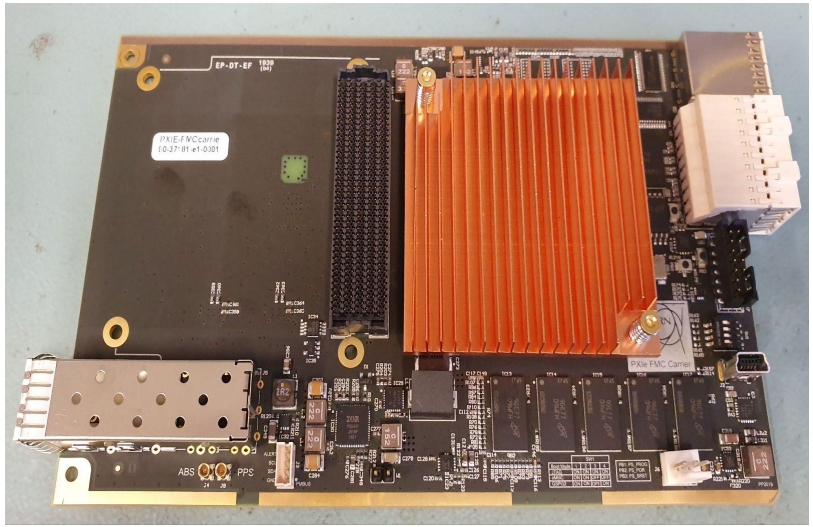

- Zynq Ultrascale+ PXIe FMC Carrier
- Developed in Sensors Acquisition and Motion Control framework
- **PL**:
  - White Rabbit PTP core and application specific core

  PS:
  - PXIe core for enumeration within 100ms
  - Reconfiguration of FPGA fabric
- **Applications:**
  - Follow up candidate for SPEC [In study]
  - LHC Collimators Upgrade
  - Mechatronics Application

Courtesy: Paul Peronnard, BE-CEM

https://ohwr.org/project/spexi7u/wikis/home

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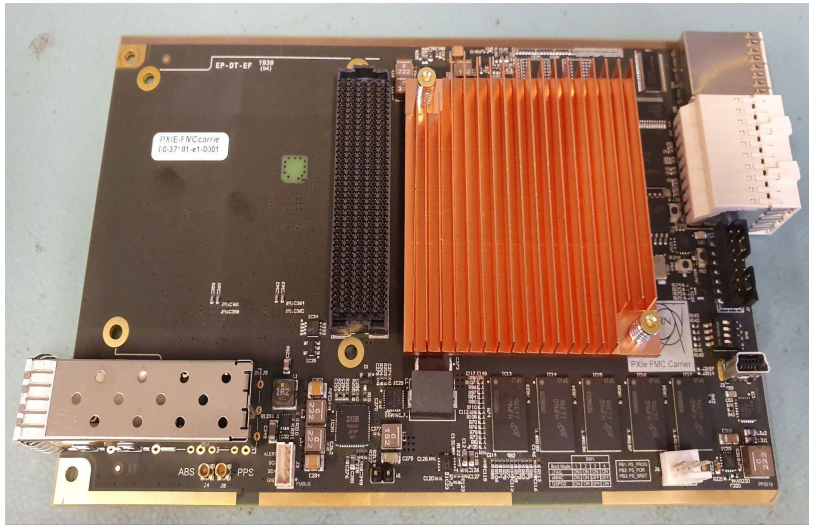

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FRAS Motorized Axes Control System, P.Peronnard

Courtesy: Paul Peronnard, BE-CEM

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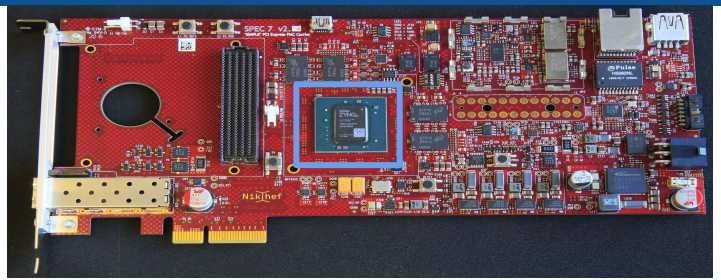
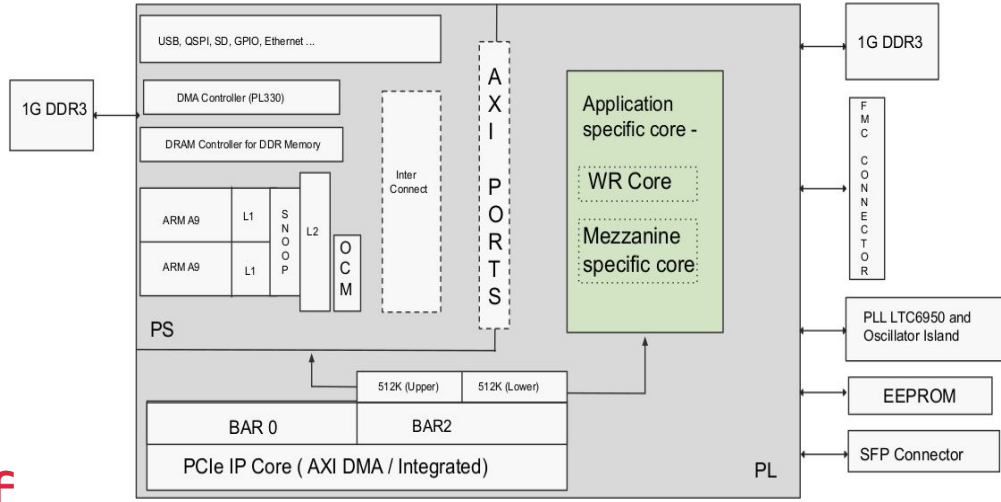
Simple PCI Express Carrier 7 (SPEC7)

- Zynq 7000 Family SoC (XC7Z030-1FBG676C) and Dual-Core ARM Cortex A9 processor
- It is optimised for low jitter for White Rabbit deployment with provision of specific clock island of PLLs
- **PL**:
  - White Rabbit PTP core and application specific core
  - Holds Golden Image for 100ms PCIe enumeration

  PS:
  - Reconfiguration via AXI Uartlite and PCIe XDMA
  - Integrate for Standalone use
- **Applications:**
  - Follow up candidate for SPEC [In study]
  - Timing source for the WRITE (White Rabbit Industrial timing Enhancement)
  - High Precision Slaved External Clock (HPSEC)
- Collaboration between NIKHEF and CERN





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The EMPIR initiative is co-funded by the European Union's Horizon 2020 research and innovation programme and the EMPIR Participating States

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  - **Fast Interlock Detection System**
  - Distributed I/O Tier
  - Beam Control System for SPS LLRF
  - Beam Position Monitoring
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- Requirements
- Efforts

Fast Interlock Detection System

- Fast pulsed kicker magnet systems are powered by high-voltage and high-current pulse generators.

- The control of pulsed systems requires the use of fast digital electronics:
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  - fast protection of the high-voltage thyratron and semiconductor switches

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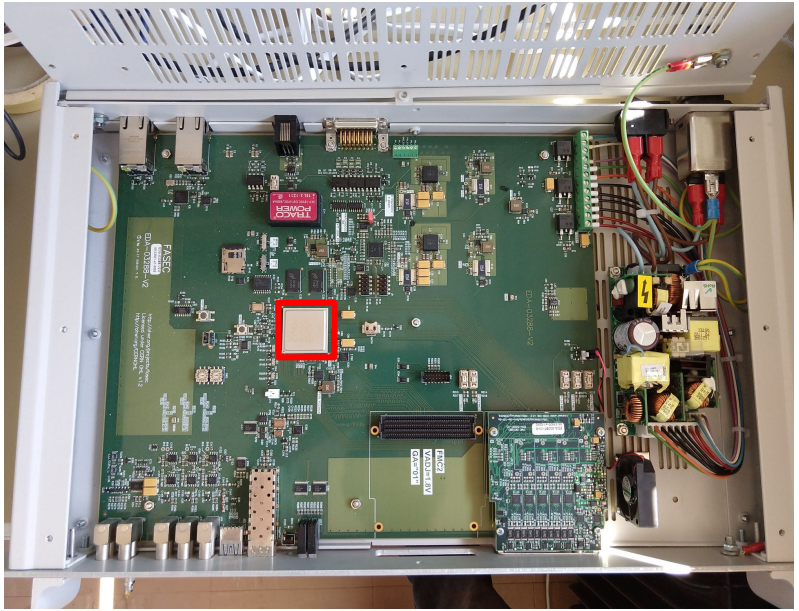
- **Solution**: Single hardware implements fast-interlocking functionality

- **Choice of Xilinx Zynq-7000 SoC**:
  - Implementation of fast reaction times (<100 ns to retrigger) and variable comparator thresholds require a FPGA
  - Integrate it neatly within the CERN control framework



Courtesy: Pieter Van Trappen, SY-ABT

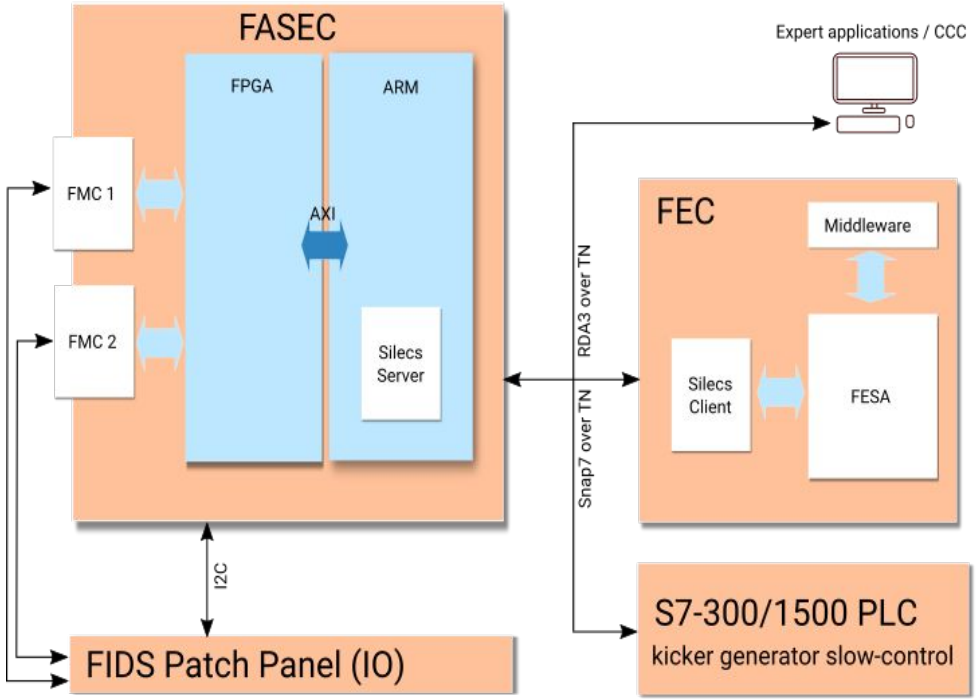
Fast Interlock Detection System

FPGA & ARM SoC FMC Carrier (FASEC)

- XC7Z030 controller, SoC with Kintex-7 fabric (PL) and Dual ARM Cortex-A9 (PS)

- **PL:**
  - Stores logic for fast detection and interlocking
  - White Rabbit PTP Core

- **PS**:
  - Implementation of an embedded (SILECS) Snap7 server
  - Automated test-procedure running on the card
  - Integrated digitizer & analysis functionality
  - Permanent diagnostics running on-board
  - Peripheral device drivers in Embedded Linux



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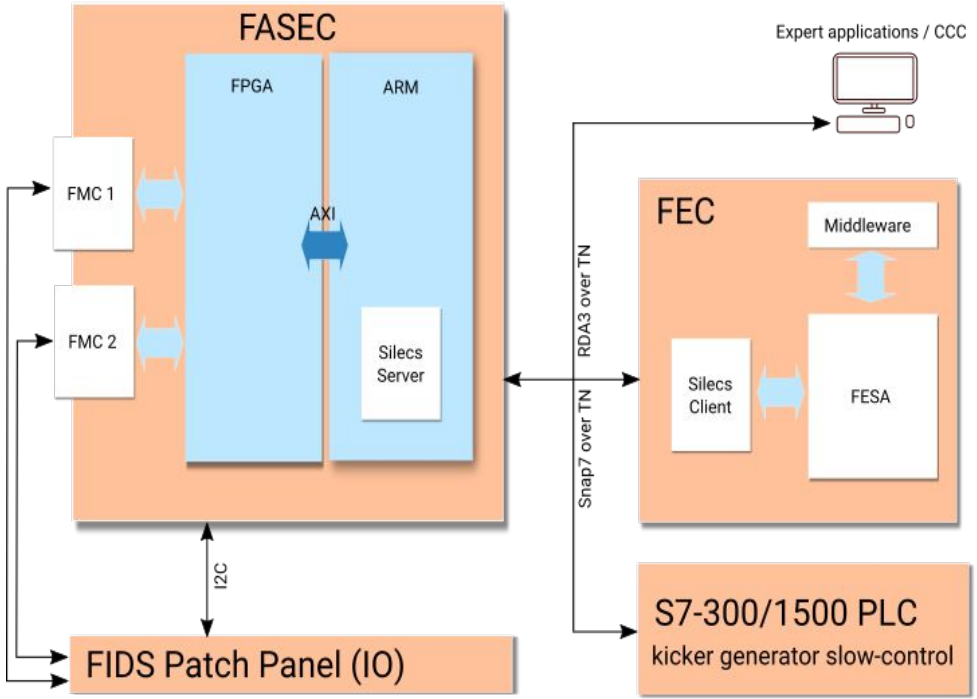
- **33 Systems** installed for **PS Booster** distributor, **PS** injection, **SPS beam** dump extraction and **LHC** injection installations and 33 more in next upgrade



SoC TECHNOLOGY FOR EMBEDDED CONTROL AND INTERLOCKING WITHIN FAST PULSED SYSTEMS AT CERN P.VAN TRAPPEN et al., ICALEPCS 2019

Courtesy: Pieter Van Trappen, SY-ABT

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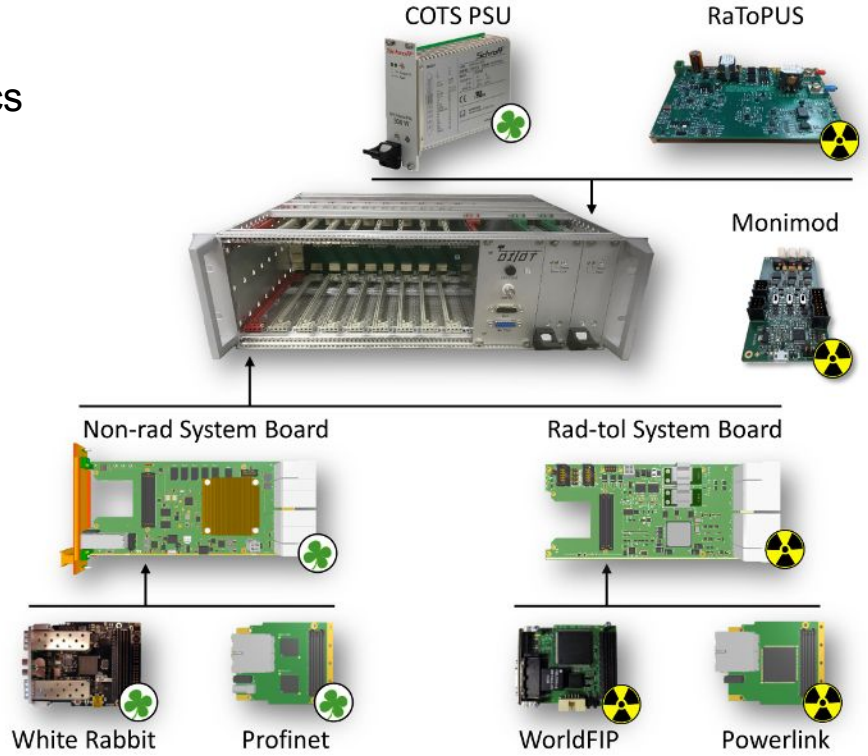
New Kit for Custom Electronics

Distributed I/O Tier

- **Low-cost, modular** platform for **custom** electronics
- based on **industrial** standards
- **Radiation-exposed** and **radiation-free** areas



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Radiation-exposed

Radiation-free

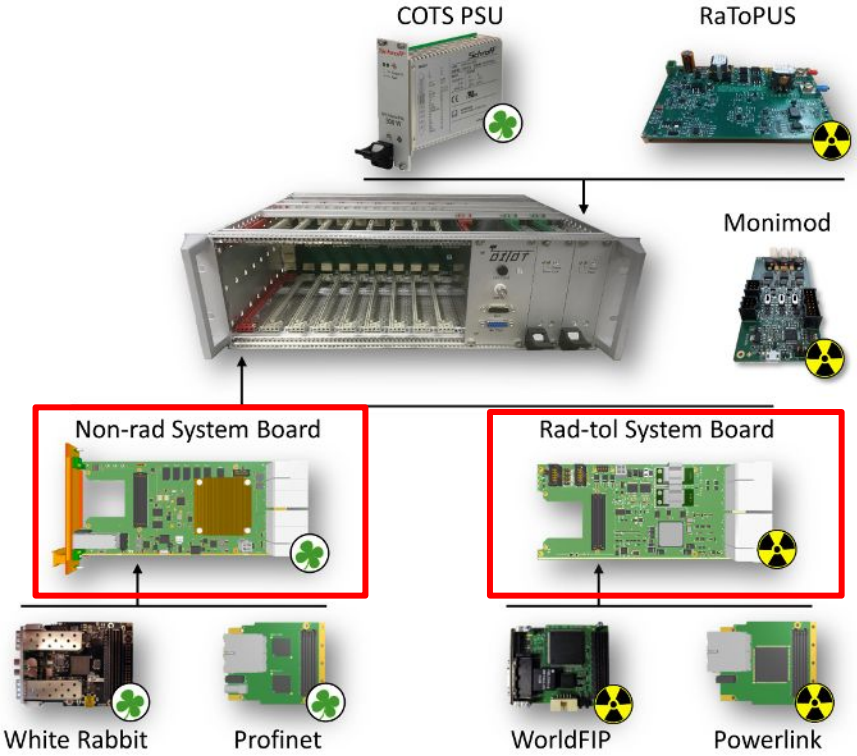
New Kit for Custom Electronics

Distributed I/O Tier

- **Low-cost, modular** platform for **custom** electronics
- based on **industrial** standards
- **Radiation-exposed** and **radiation-free** areas
- Interesting SoC use cases:

Non-Radiation Tolerant System Board:
PS: Controls framework and services, Remote Upgrades
PL: White Rabbit PTP core

Radiation Tolerant System Board:
- HydRA SoC Architecture
Soft CPU(based on RISC-V):FEC Monitoring Services
FPGA:Communication Logic Core



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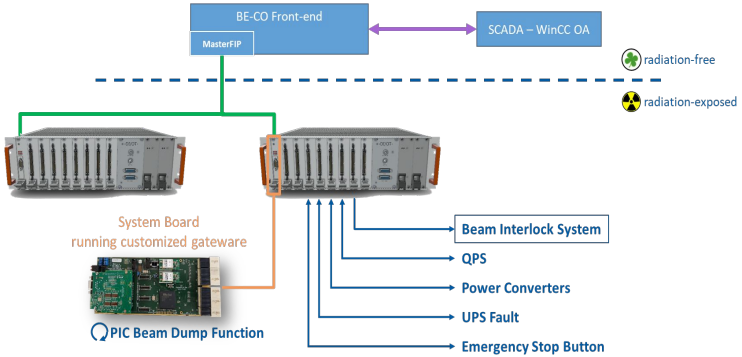
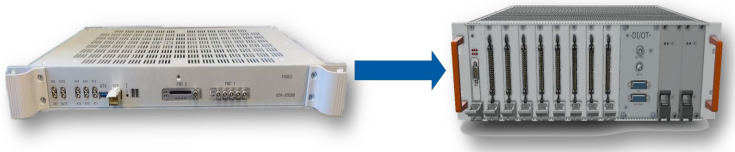
Applications

- Powering Interlock Controller, *TE-MPE*



- Fast Interlocks, *SY-ABT*



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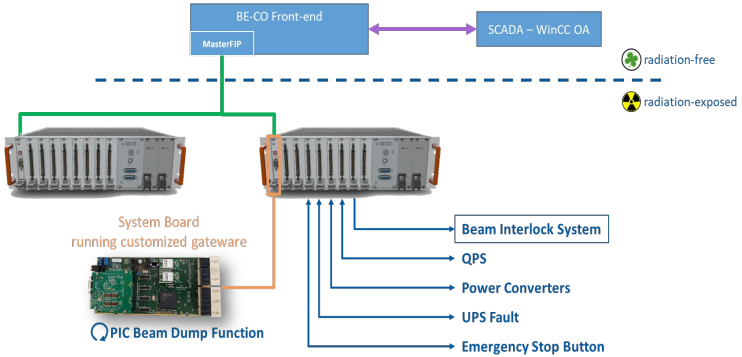

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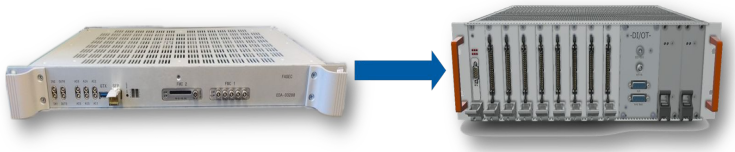
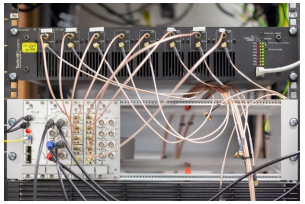
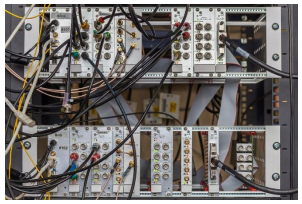
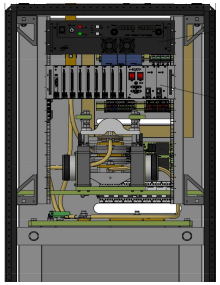


- Quantum Computing, *Creotech Instr. S.A., PL*





- Coupling Loss Induced Quench System (CLIQ) ,*TE-MPE*



Applications

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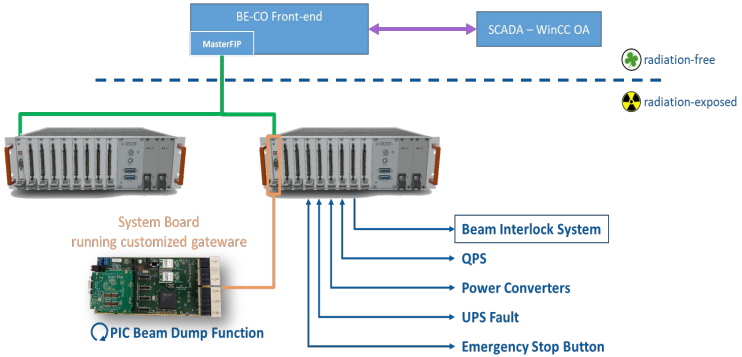
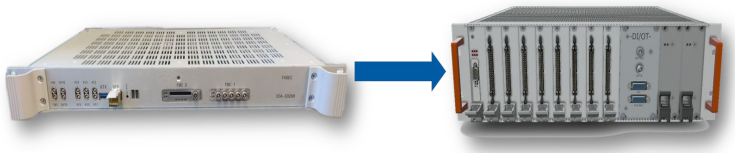
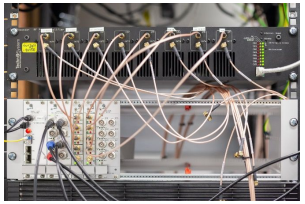
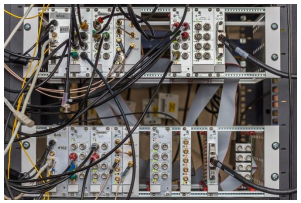


- Fast Interlocks, *SY-ABT*

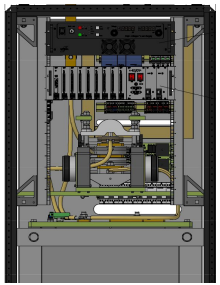


- Quantum Computing, *Creotech Instr. S.A., PL*



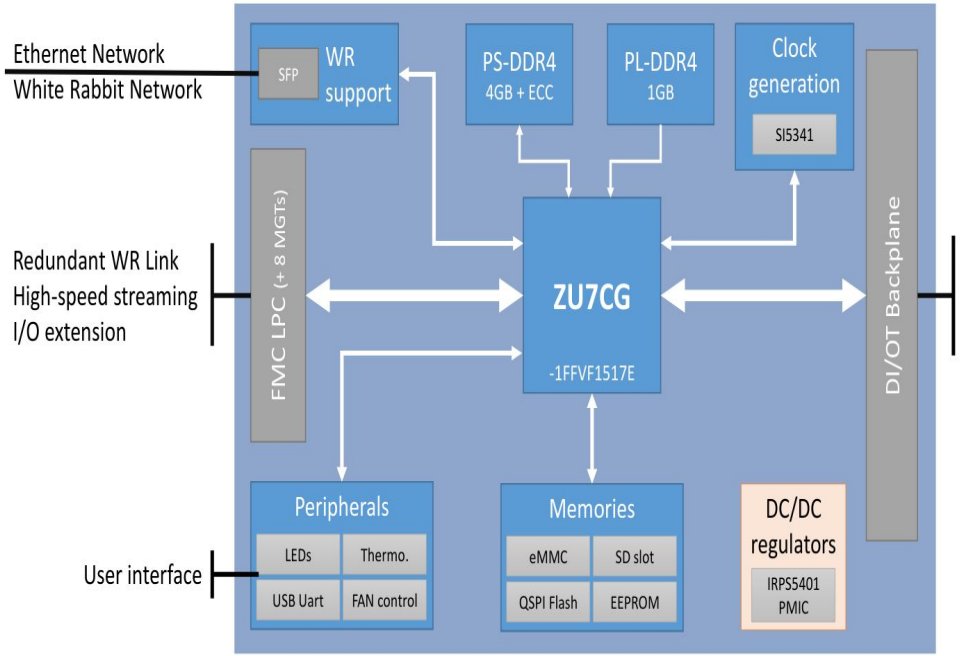


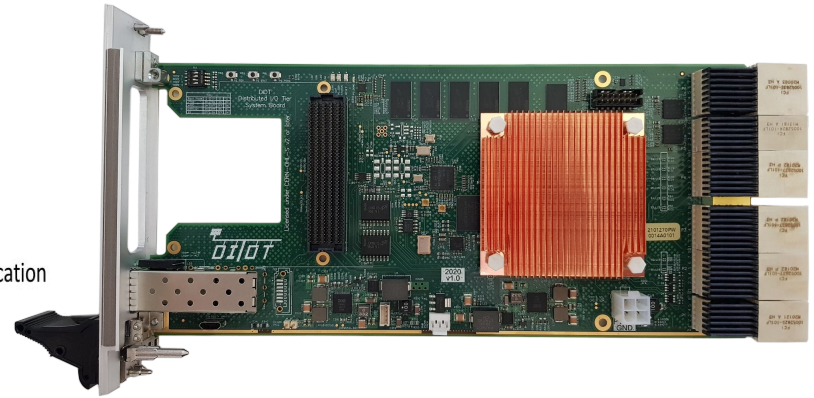
- Coupling Loss Induced Quench System (CLIQ) ,*TE-MPE*



G. Daniluk & E. Gousiou, *BE-Technical Meeting 04.06.20*

Non-Rad Tol System Board

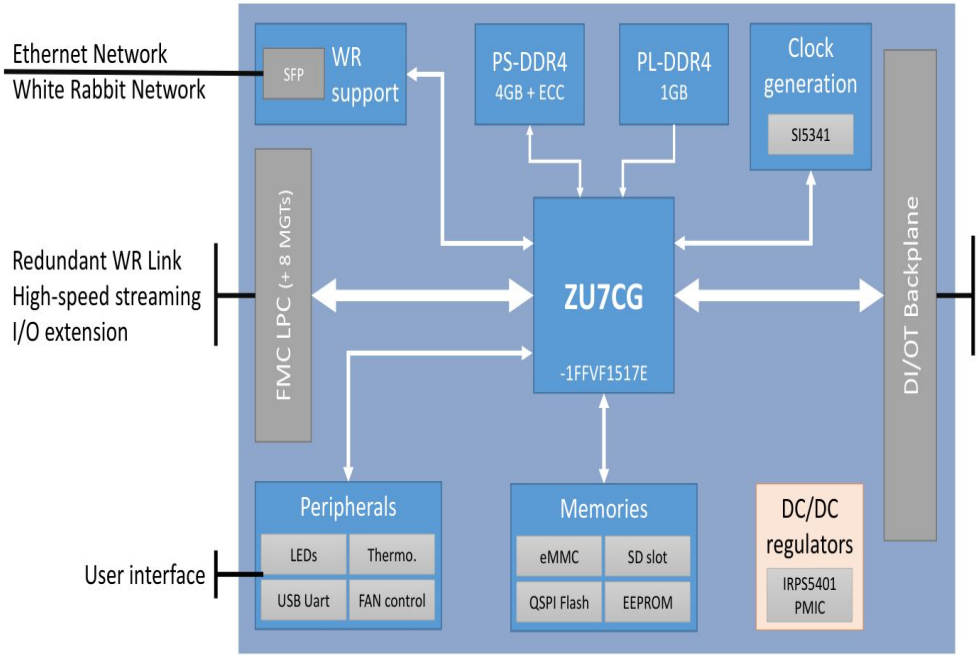


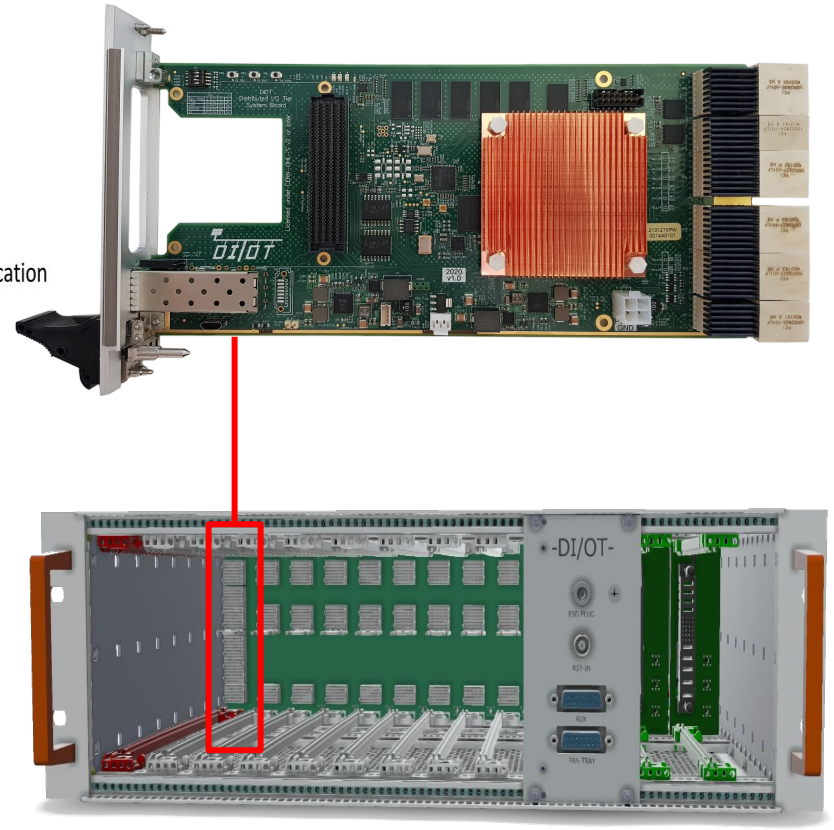


https://ohwr.org/project/diot-sb-zu/wikis/home

Courtesy: G.Daniluk, E.Gousiou

Non-Rad Tol System Board as Front-End Computer





Courtesy: G.Daniluk, E.Gousiou

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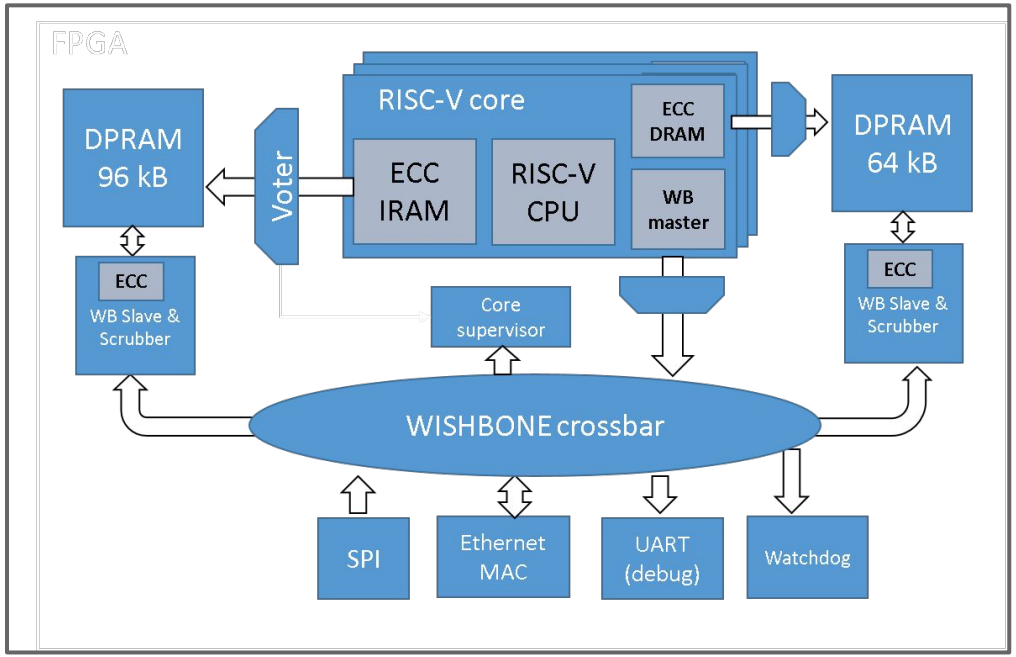
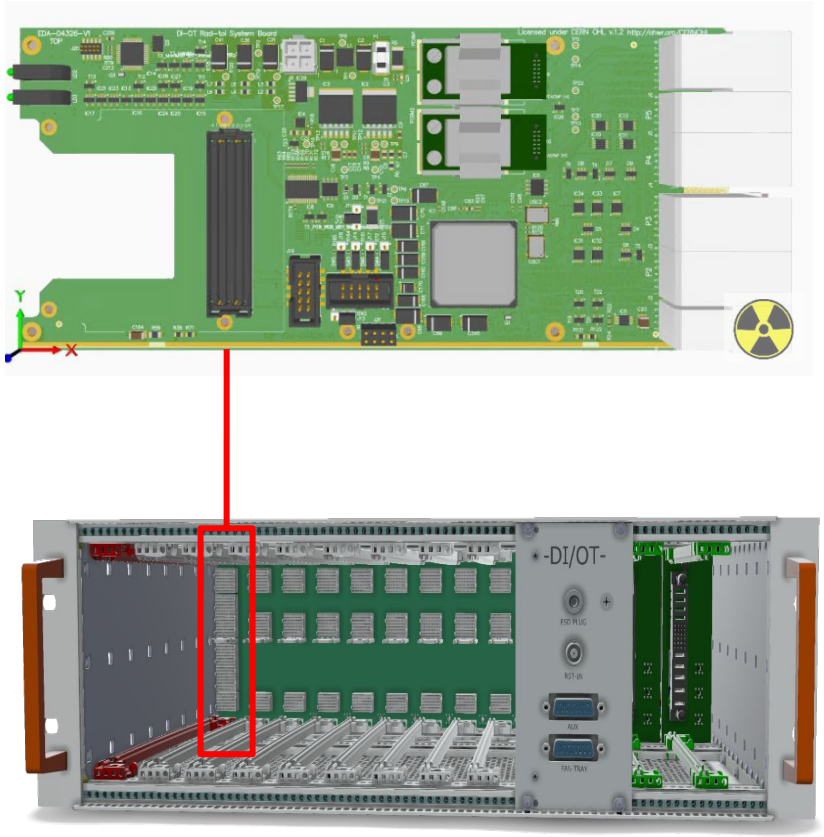
Hydra SoC Architecture for Rad Tol System Board





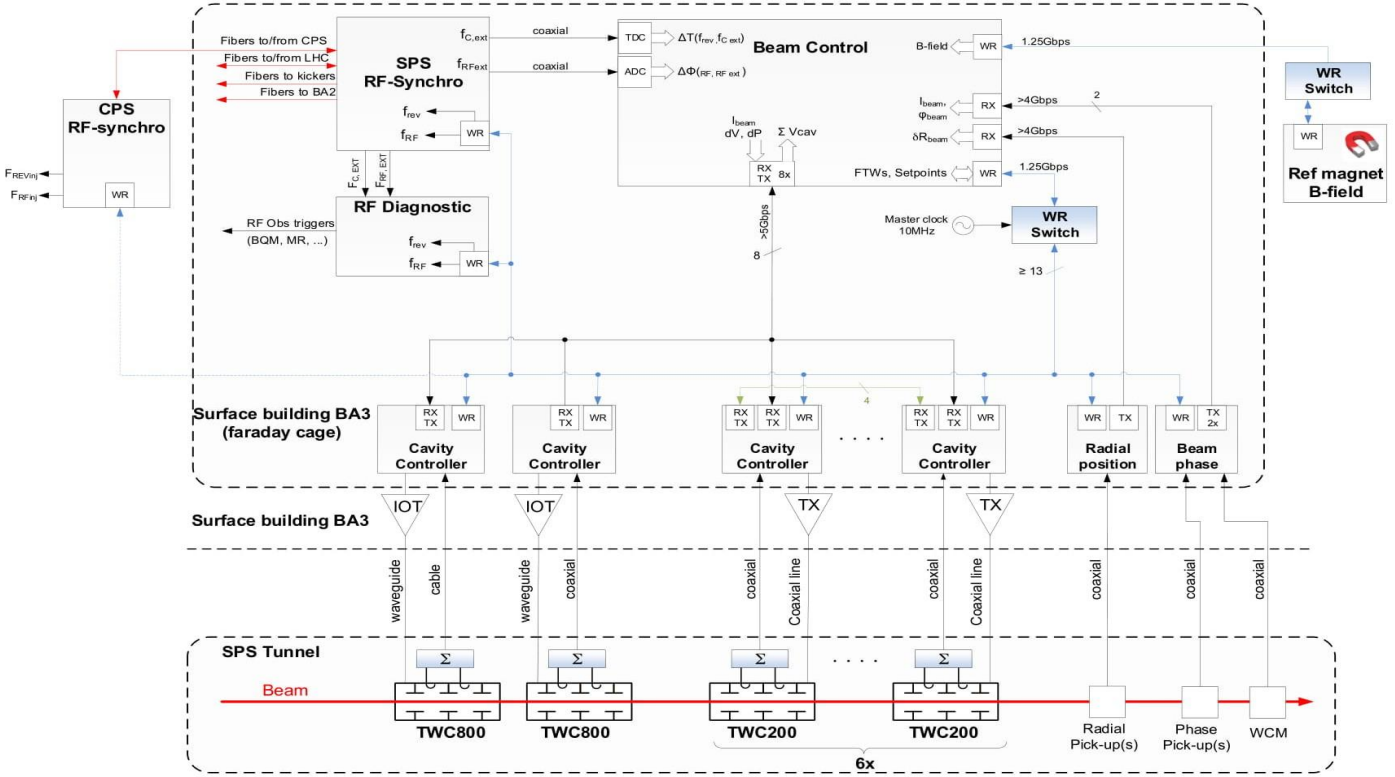
https://ohwr.org/project/hydra/wikis/home

Courtesy: G.Daniluk, M.Rizzi

Outline

- SoC in Accelerator and Technology Sector
- SoC based Projects in A&T Sector
  - White Rabbit
    - Switch v4
    - Nodes - SPEC7, SPEXI7
  - Fast Interlock Detection System
  - Distributed I/O Tier
  - **Beam Control System for SPS LLRF**
  - Beam Position Monitoring
  - Beam Gas Ionization
- Requirements
- Efforts

Beam Control AFCZ Card for SPS LLRF Upgrade



Courtesy: A.Spierer, G.Hagmann, T.Wlostowski

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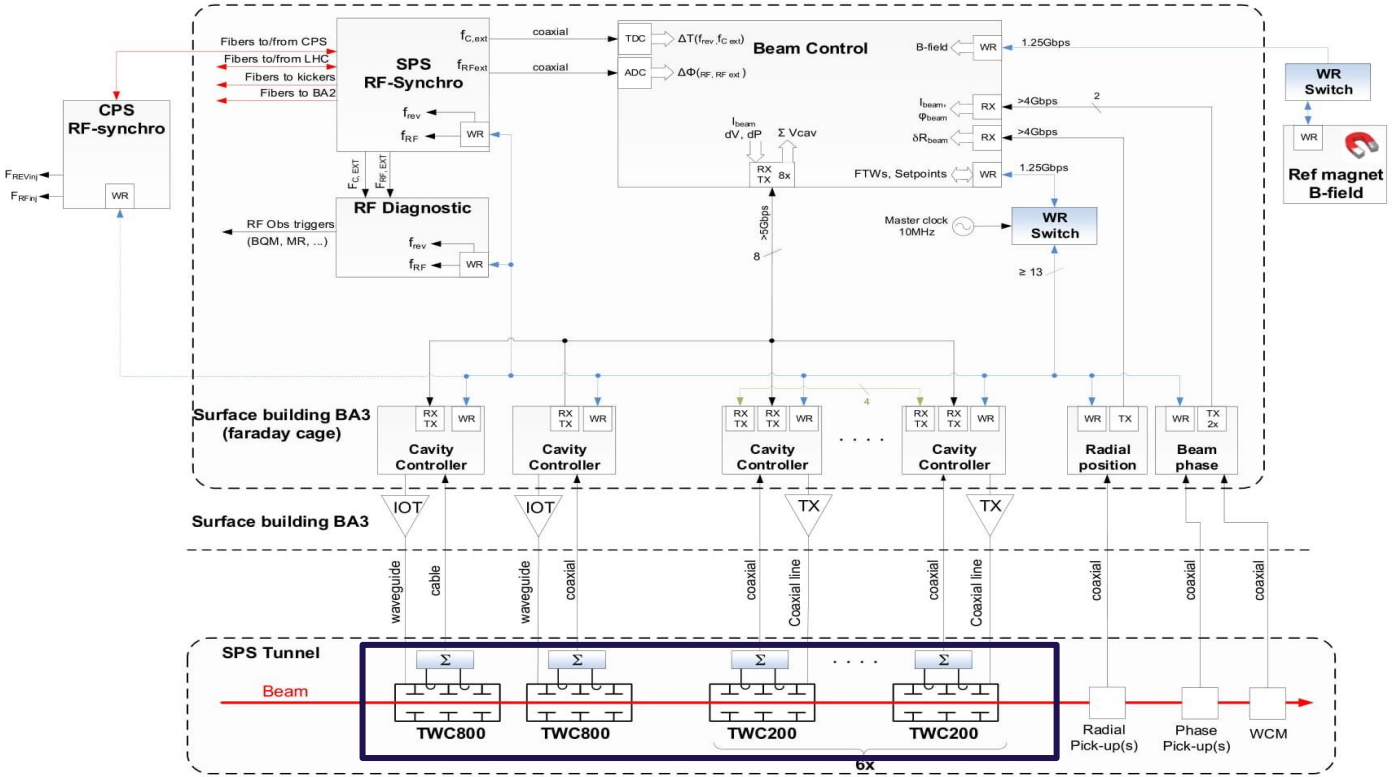

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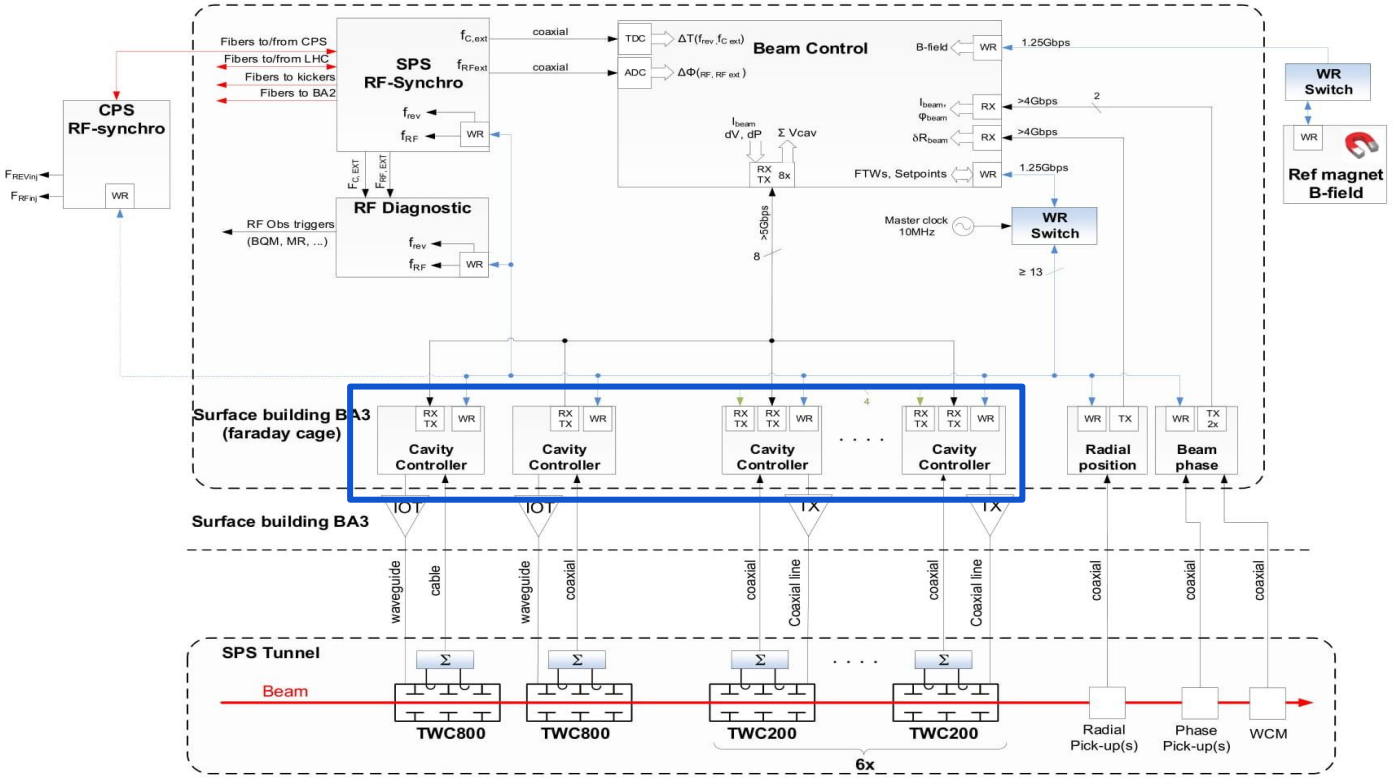

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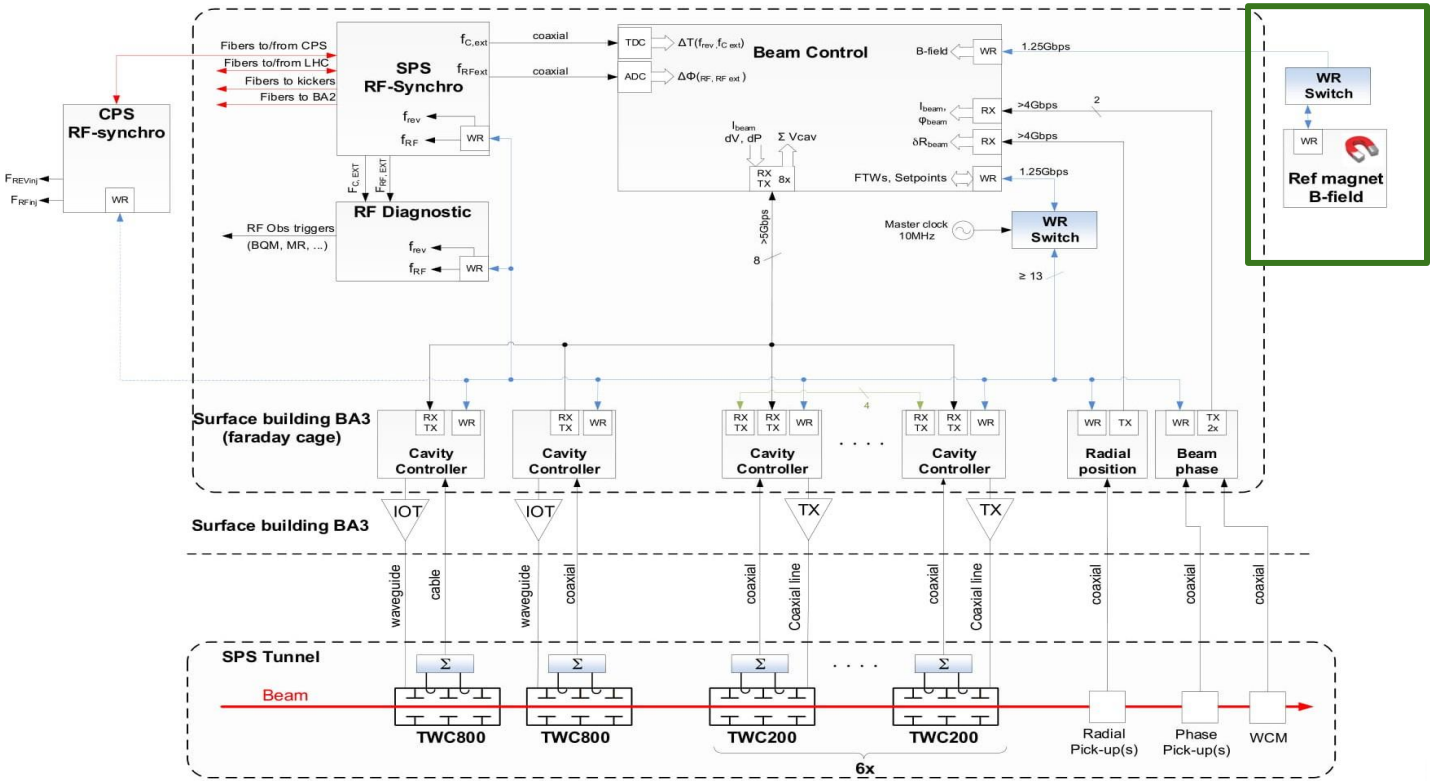

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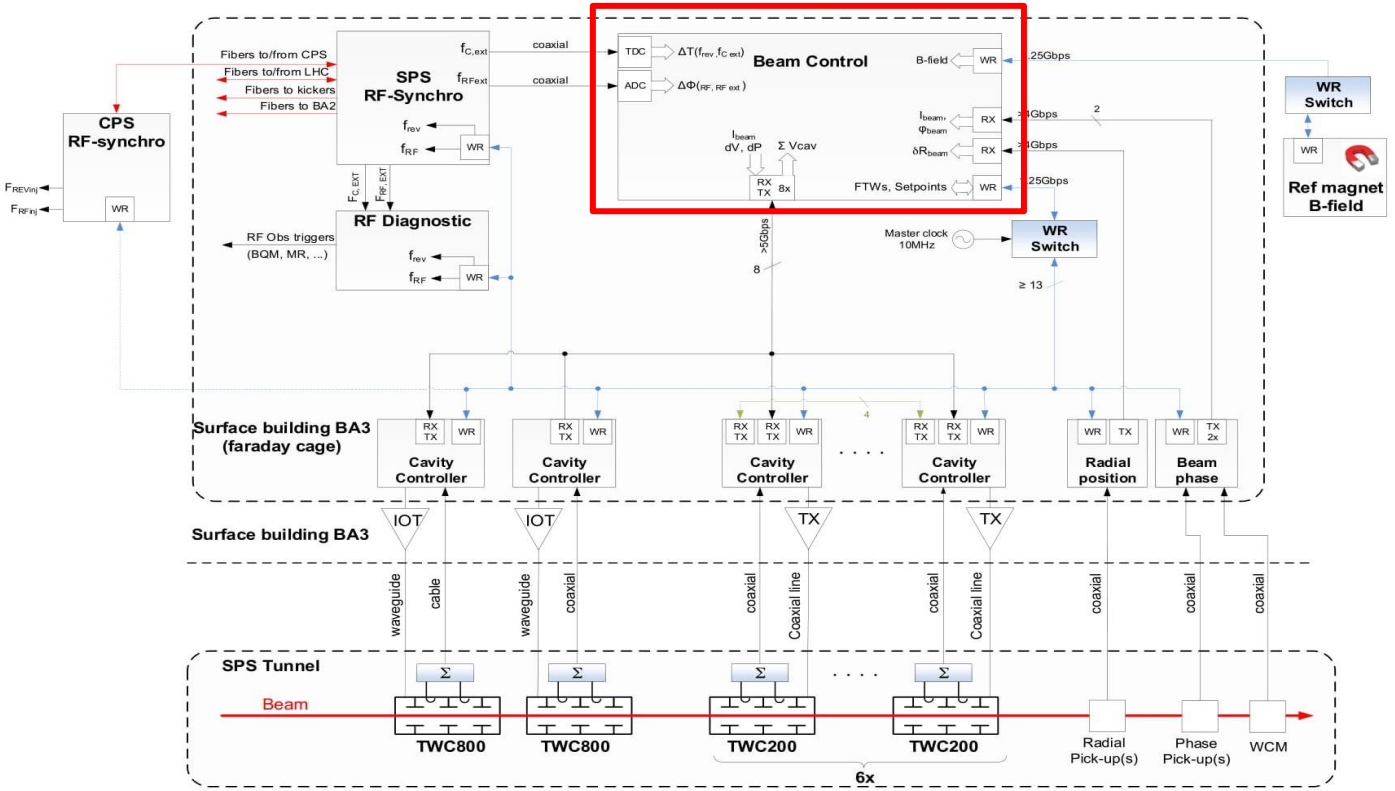

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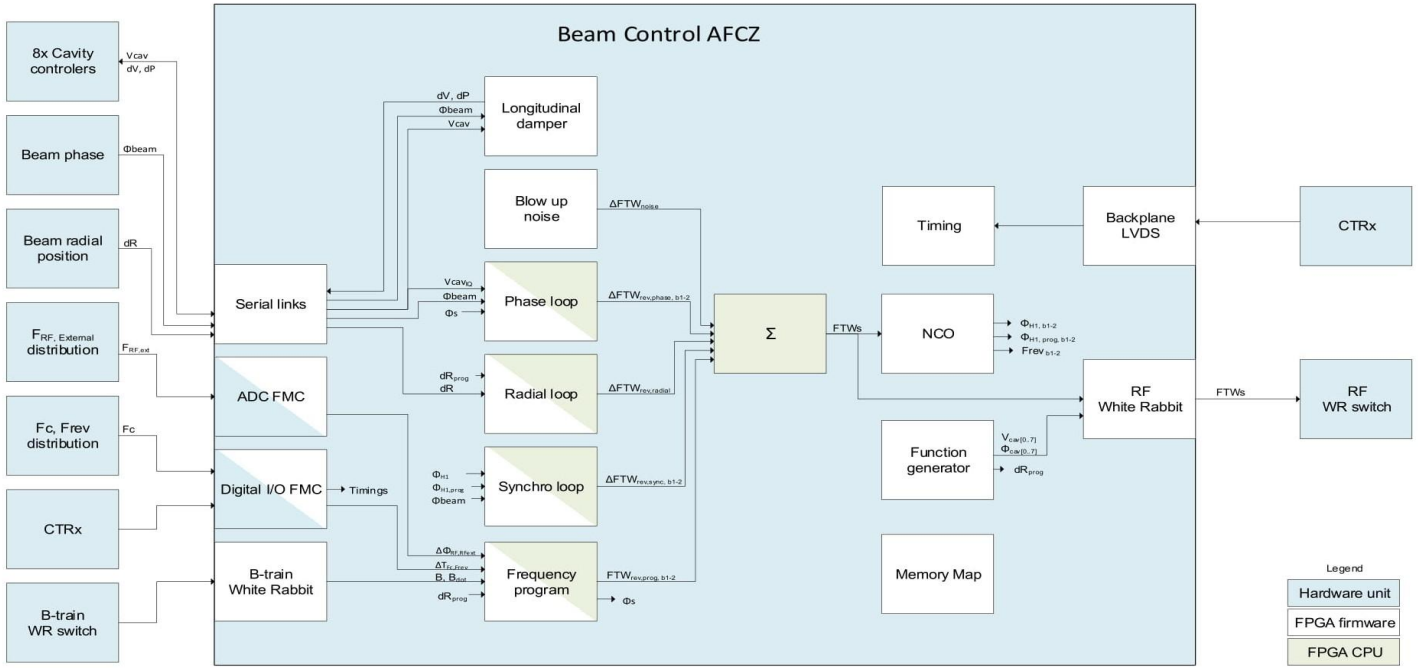
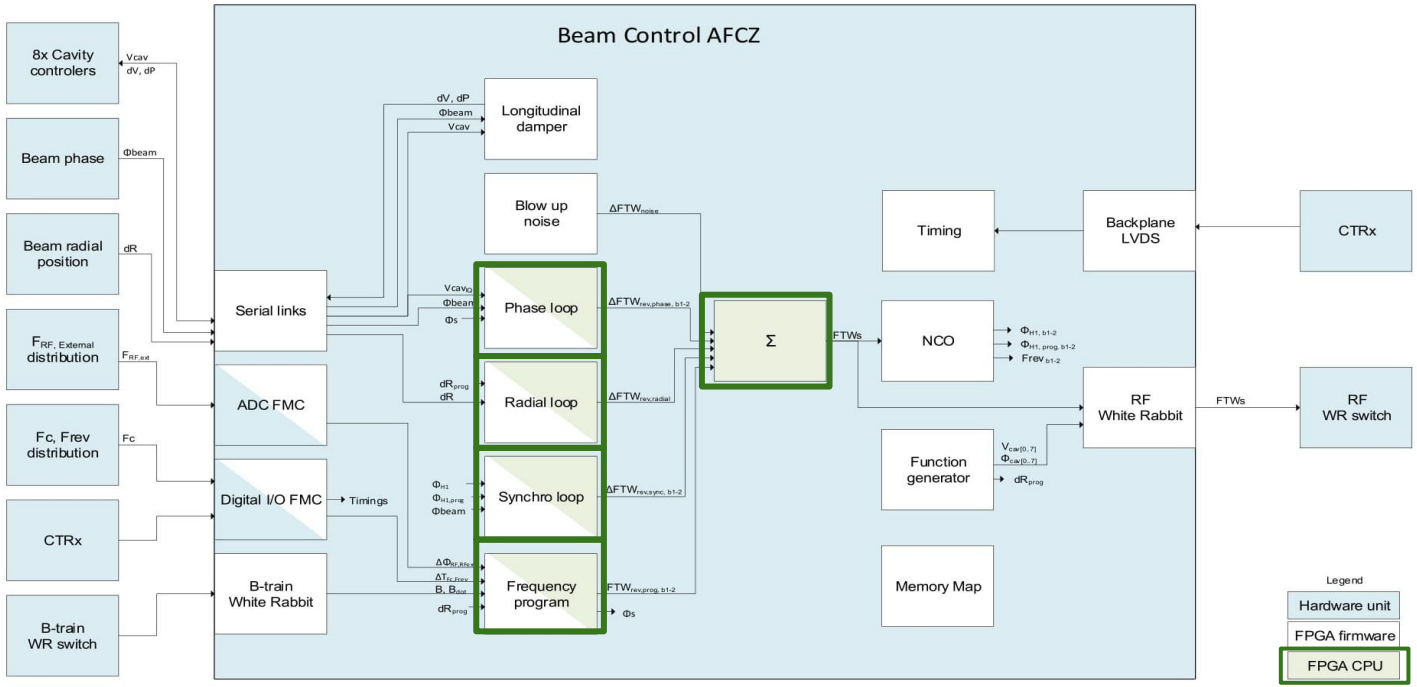


Upgrade of the SPS LLRF beam-based loops on the MicroTCA platform, A.Spierer, [LLRF-2019]

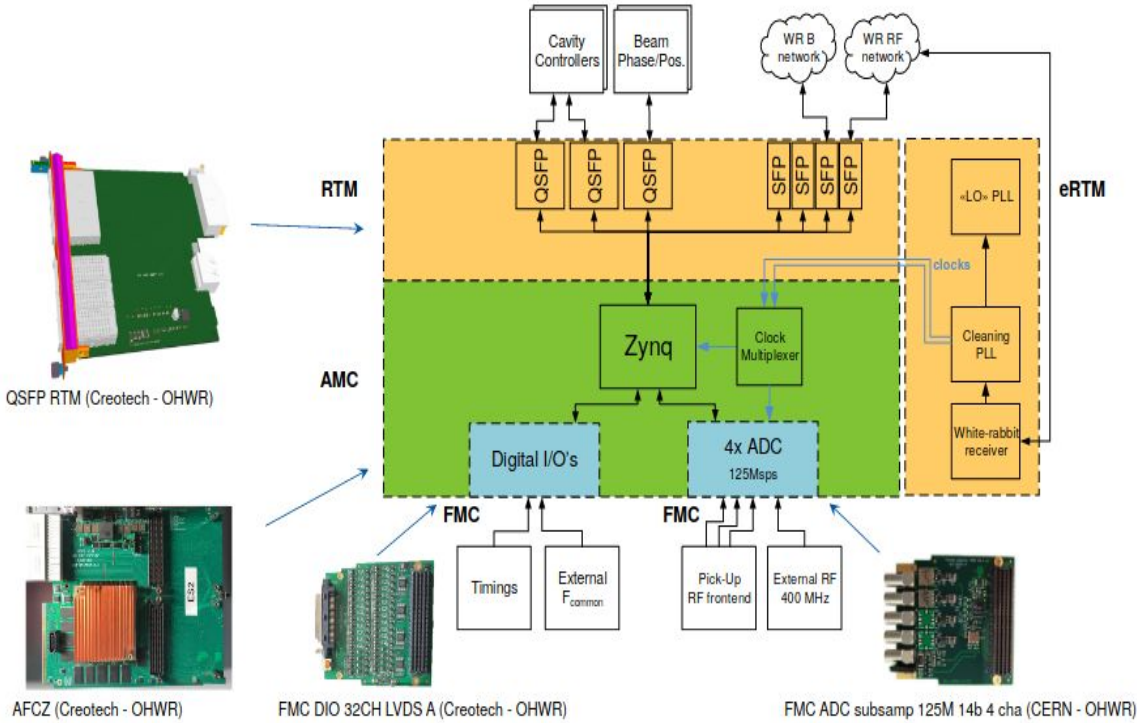
Beam Control AFCZ Card for SPS LLRF Upgrade



Upgrade of the SPS LLRF beam-based loops on the MicroTCA platform, A.Spierer, LLRF-2019

Beam Control AFCZ Card for SPS LLRF Upgrade

- AMC FMC Carrier based on Zynq Ultrascale+ Family
- **PL**:
  - White Rabbit PTP core to transfer Frequency Tuning Words (FTW) across SPS and LHC
- **PS**:
  - Bare Metal Application that implements biquadratic filters and algorithms to calculate feedback loops
- Beam Control system for SPS LLRF Upgrade deployed at BA3 (surface building) in Faraday Cage



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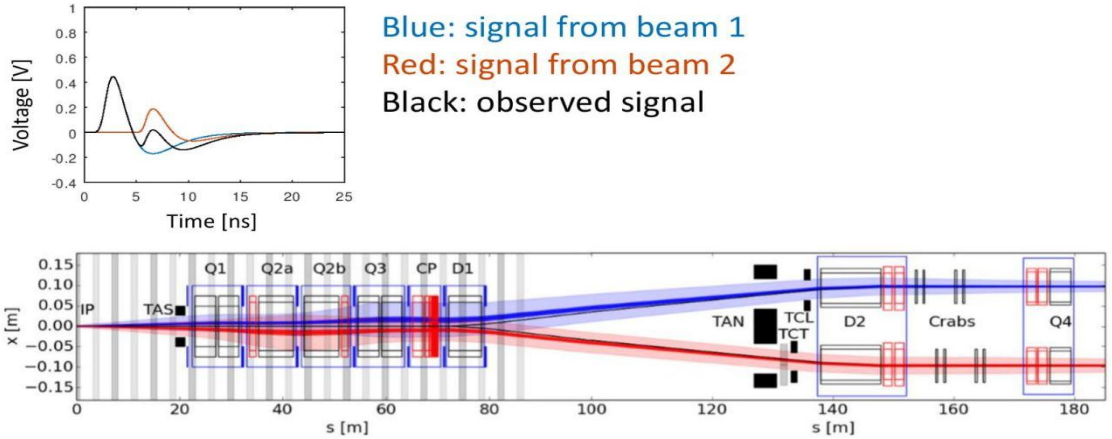
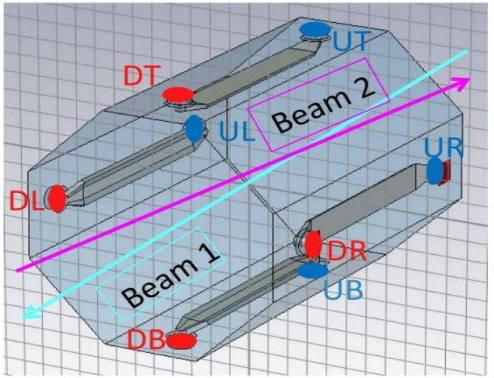
- Efforts

RFSoC in HL- Beam Position Monitoring System

- Close to LHC interaction regions, both beams are in a single pipe
- Each beam couples to a different end of the BPM, so all eight stripline ports should be measured to get horizontal and vertical position of both beams
- Coupling is not perfect, so measured signals contain contributions from both beams and additional processing is required to isolate the signal from the beam of interest



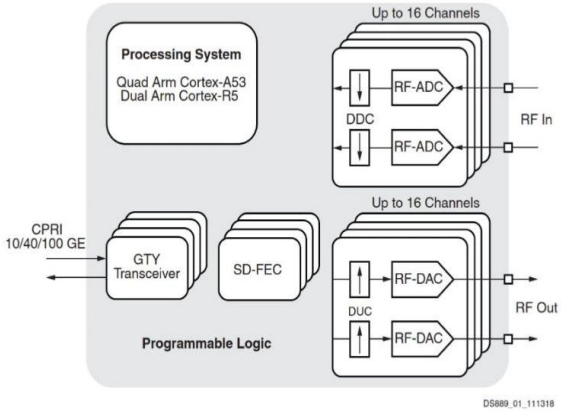


Courtesy: A.Boccardi, D.Bett, I.Degl'Innocenti

RFSoC in HL- Beam Position Monitoring System

Zynq RFSoC as prototype BPM processor [In Study]

- Evaluation board ZCU111 acquired as basis for prototype BPM processor
- RFSoC model XCZU28DR (Xilinx Zynq UltraScale+ architecture, gen. 1)



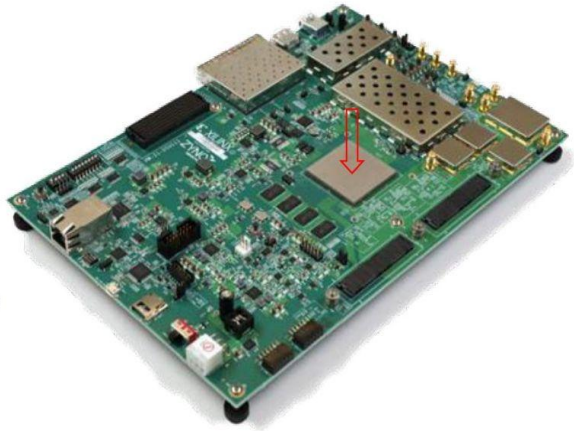


Figure 1: **Zynq UltraScale+ RFSoC**

Source: *Zynq UltraScale+ RFSoC Data Sheet: Overview (DS889)*

Processing System Features	
Application Processing Unit	Quad-core Arm Cortex-A53 up to 1.33 GHz
Real-Time Processing Unit	Dual-core Arm Cortex R5 up to 533 MHz

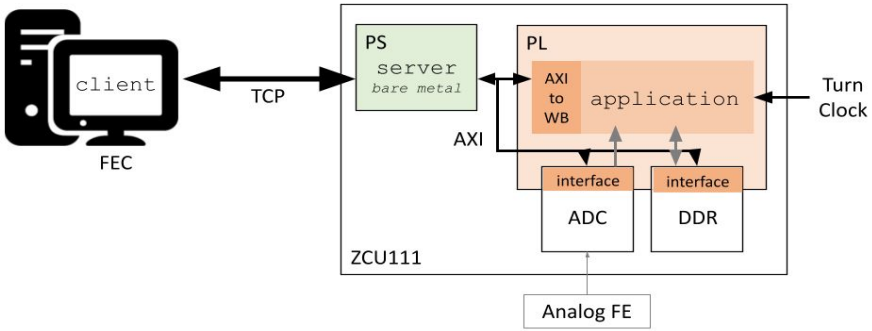
RF Features		
Max. RF input Frequency (GHz)		4
Decimation / Interpolation		1x, 2x, 4x, 8x
12-bit RF-ADC	# of ADCs	8
	Max Rate (GSPS)	4.096
14-bit RF DAC	# of DACs	8
	Max Rate (GSPS)	6.554

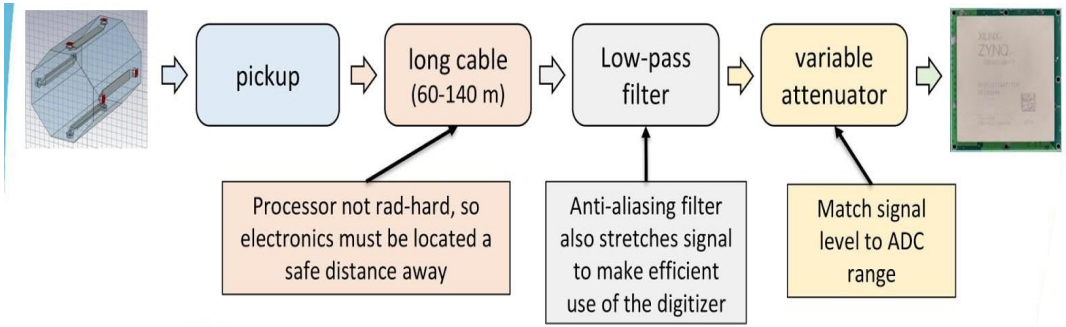
Programmable Logic	
System Logic Cells (K)	930
DSP Slices	4,272
Memory (Mb)	60.5
33 Gb/s Transceivers	16
Maximum I/O Pins	347

Courtesy: A.Boccardi, D.Bett, I.Degl'Innocenti

RFSoC in HL- Beam Position Monitoring System

Zynq RFSoC as prototype BPM processor



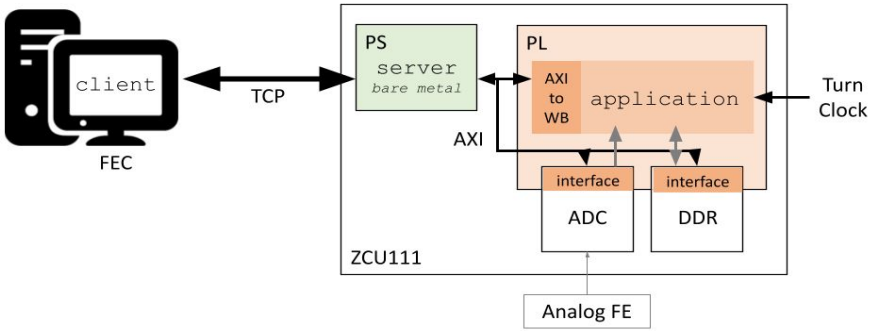


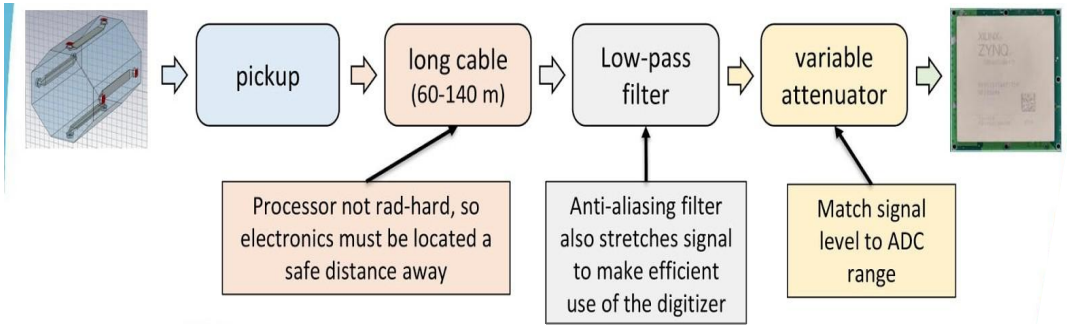
- Proof of Concept Implementation:
  - Acquire raw-data from Analog FE
  - Digitization of two planes pick-up signals
  - Data read-out from the memory for offline analysis
- Next, BPM Data-processing inside the FPGA
- **SoC:** Provides RF chain, DACs and ADCs on a single chip
- **PL**: Data Acquisition, Digitizing and Processing
- **PS**: Network Interface, Upstream data to FEC, RPU
- Simulation Framework for Study

Courtesy: A.Boccardi, D.Bett, I.Degl'Innocenti

RFSoC in HL- Beam Position Monitoring System

Zynq RFSoC as prototype BPM processor





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SIMULATION OF THE SIGNAL PROCESSING FOR THE NEW INTERACTION REGION BPMs OF THE HIGH LUMINOSITY LHC, D.BETT, IBIC 2020

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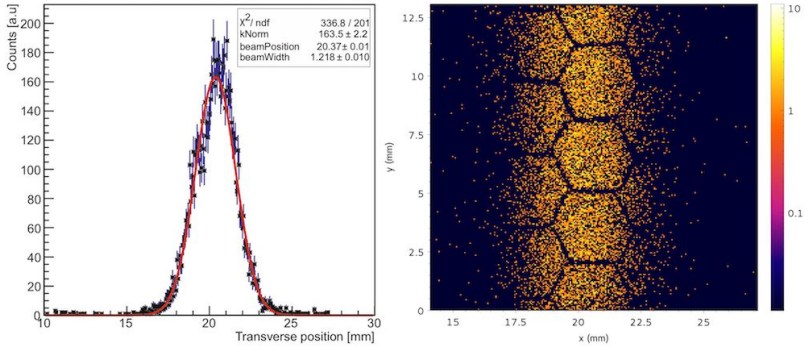
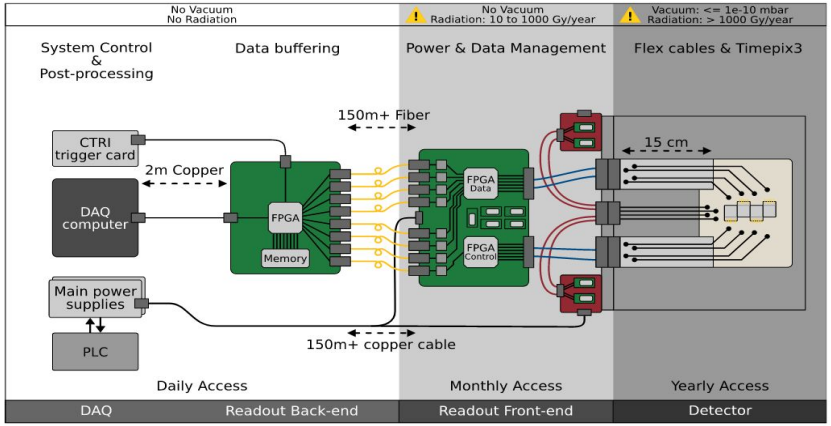
SoC in Beam Gas Ionization Back-End Electronics

- BGI profile monitors based on Timepix3 pixel detectors
- **2 operational monitors** are installed in the PS and **2 monitors** are planned to be installed in the SPS





Courtesy: J.Storey, H.Sandberg

SoC in Beam Gas Ionization Back-End Electronics

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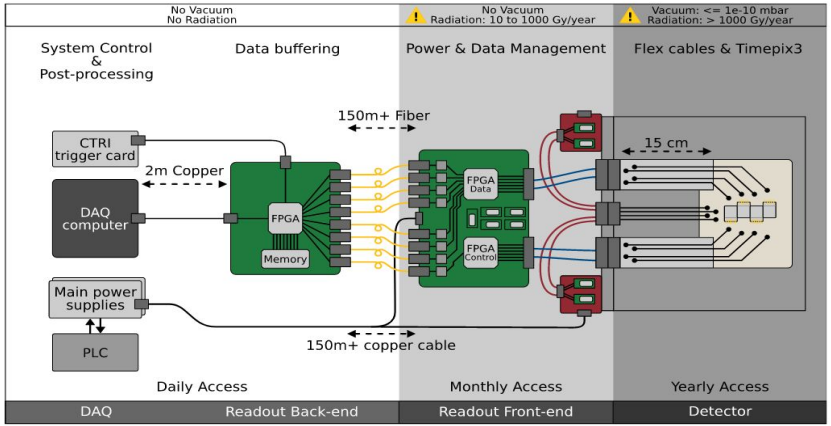
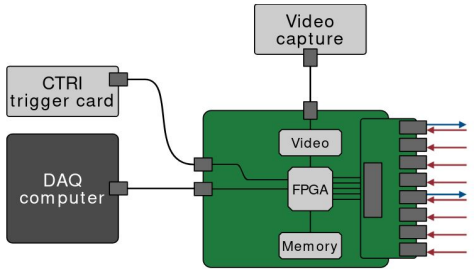
  - Xilinx VC707 FPGA
  - CTRI to controls the acquisition time
  - Video transmitter chip provides a DVI compatible video signal





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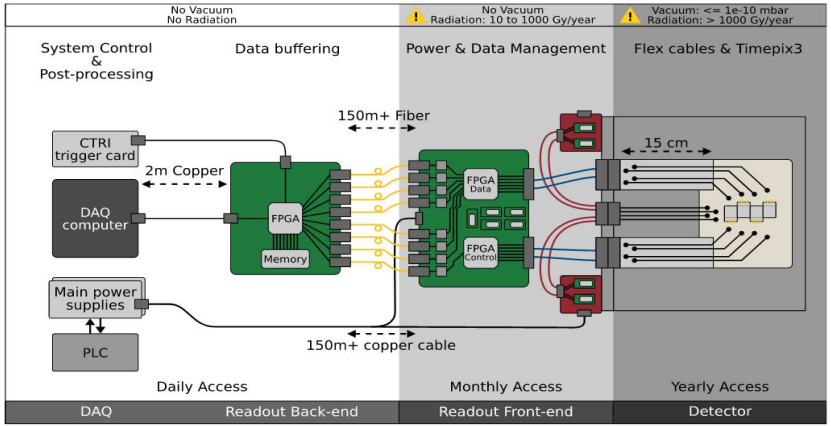
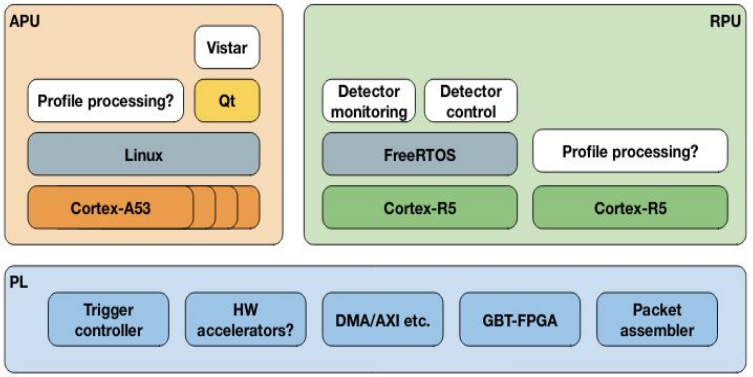
  - Xilinx Zynq Ultrascale+ MPSoC
  - One RPU with a monitoring firmware would run that takes care of the communication with the front-end
  - Other RPU video frame generation complementing Linux in A53





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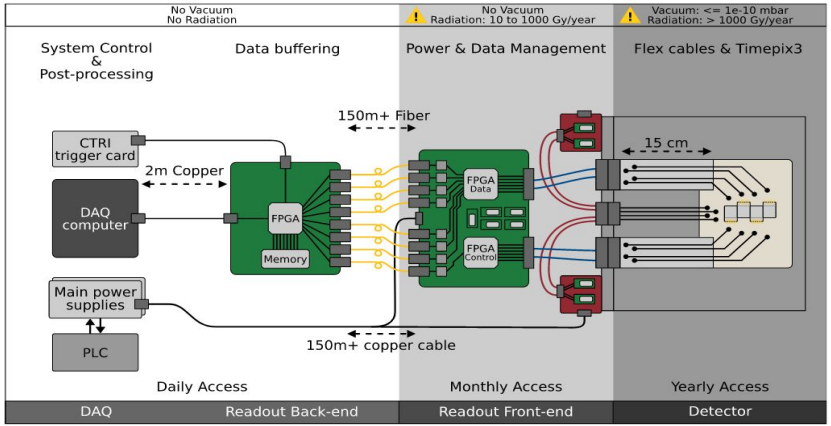
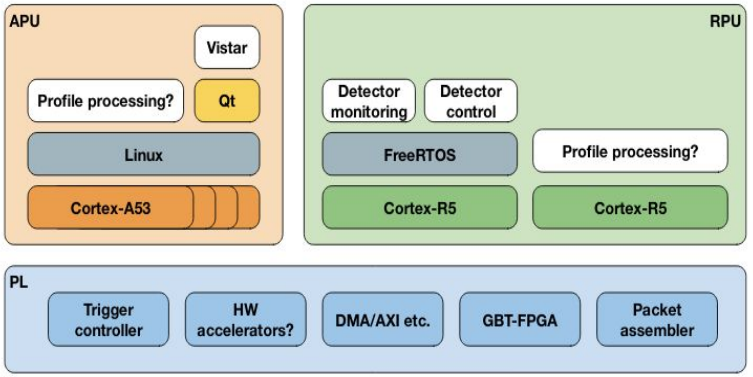
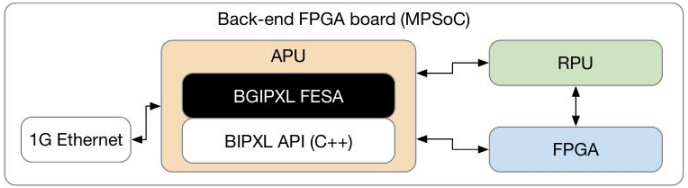
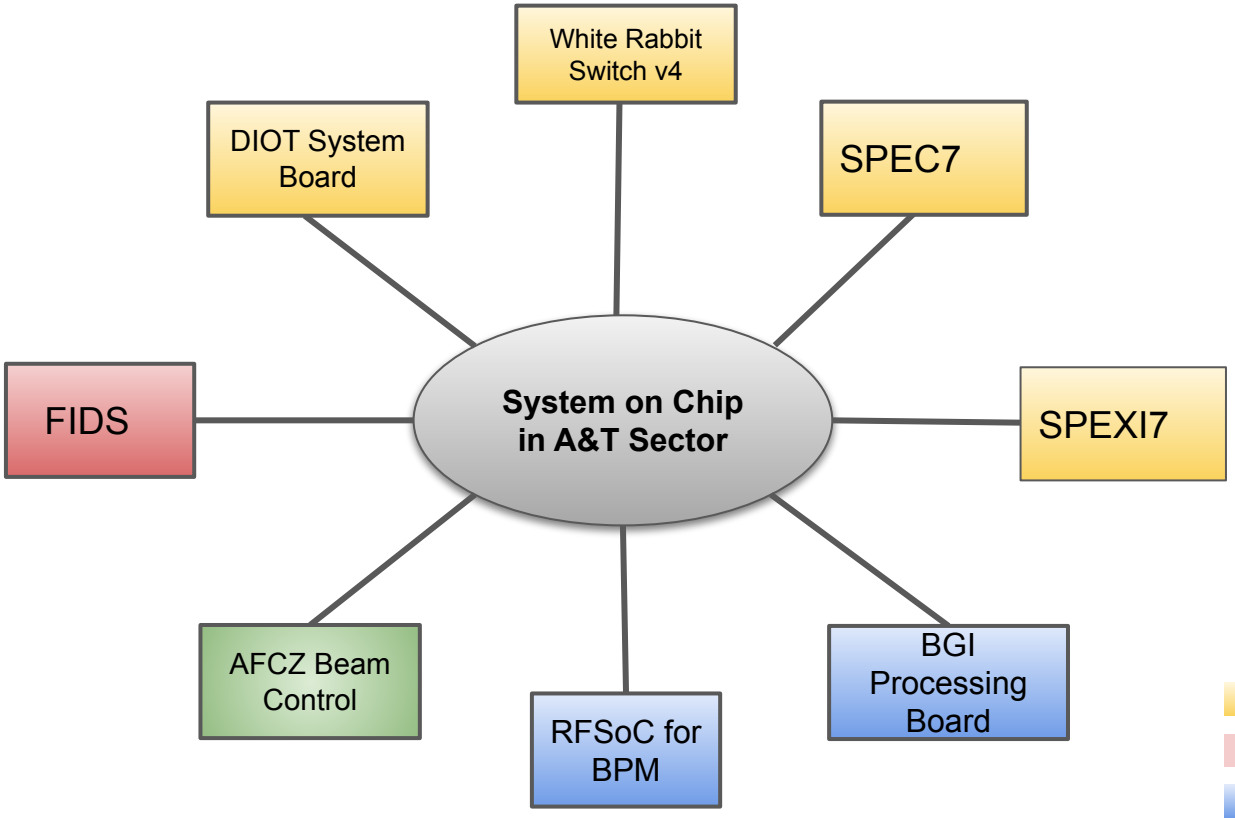






https://bgi.web.cern.ch/bgi/introduction.html

SoC in Accelerator and Technology Sector



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- Approach

Requirements

- Common **toolchains and build environment** to support PS and PL
- **Unified development model**, uniform remote upgrade systems i.e TFTP Server for storing bitstream, kernel image and rootfs
- A common **deployment strategy** over network i.e boot server
- **Safe Upgrade** support
- For some specific projects, a **standard Linux Image with Control services** provided by BE-CEM

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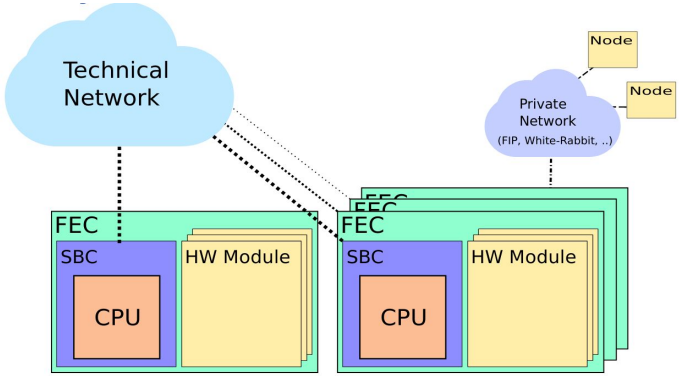
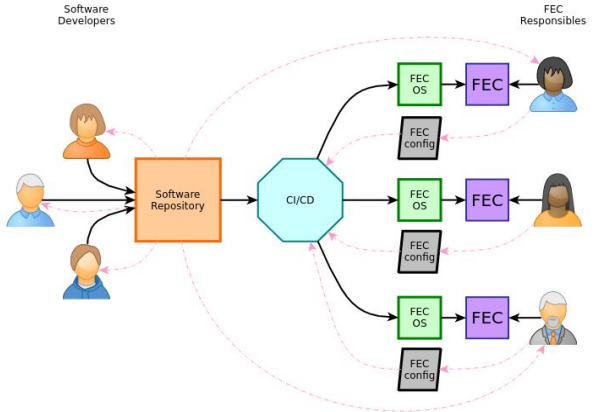
Approach

- **System on Chip Study** conducted to know about the common needs and issues in A &T Sector
- With **FEC Linux Standardization project** - study the possible Linux distributions and recommend an option for the SoC platforms
- Study of **available tools** - Yocto, Buildroot, ELBE, Civil Infrastructure Project
- **CI/CD for gateware** - ongoing effort in BE-CEM and TE-EPC





Courtesy:F.Vaga, K.Blantos

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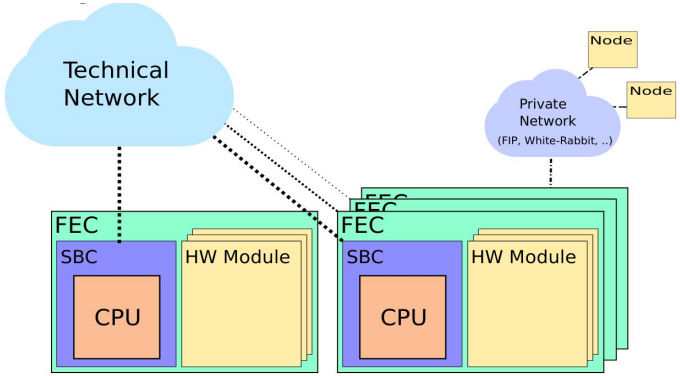
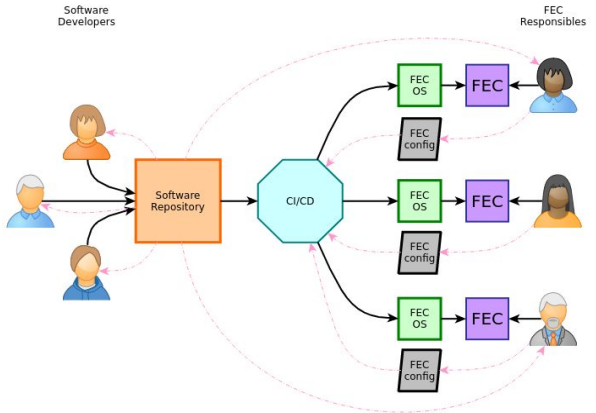
System-On-Chip Support Study, F.Vaga, BE-CO TM





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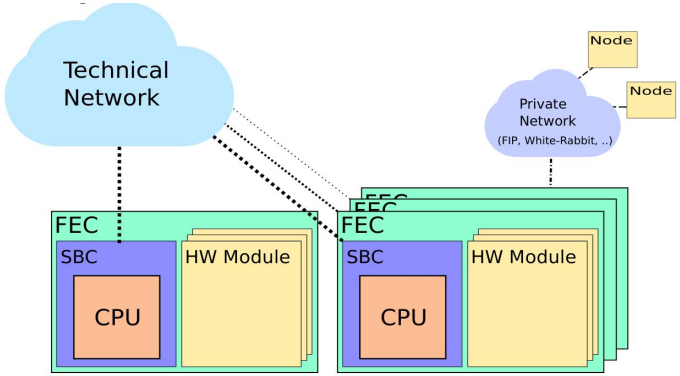
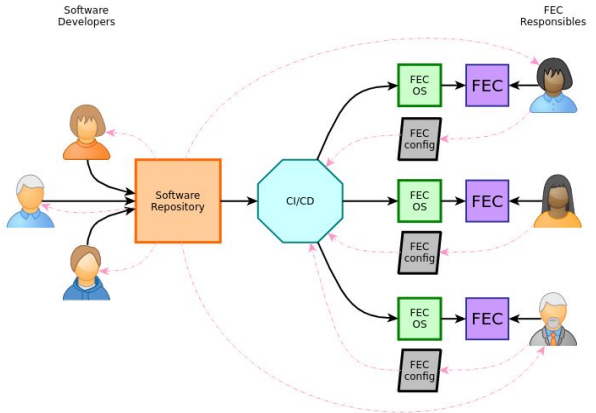
System-On-Chip Support Study, F.Vaga, BE-CO TM

https://gitlab.cern.ch/cce/cce





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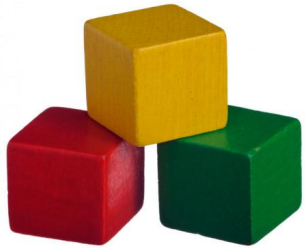
Final Thoughts

- System on chip used in A&T :
  - **Data Acquisition Systems**
  - **Controls and Timing**
  - **Real Time Processing**

- Increase in usage of SoC in A&T from LS2 to LS3 and many more applications in coming future

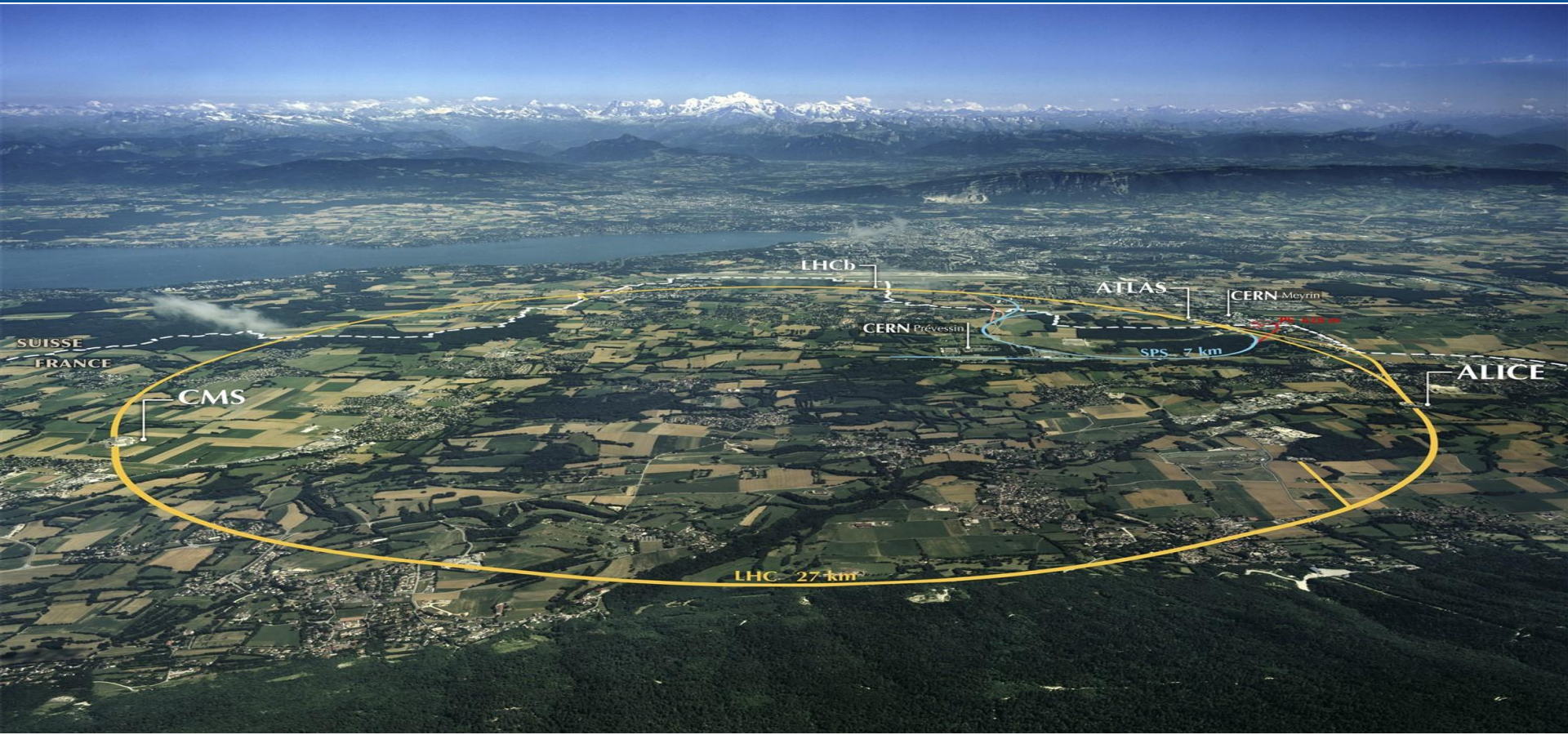
- Main challenges identified as:
  -Need for **unified development and deployment** environment
  -**Integration** with control frameworks

- Looking forward to understand best practices through collaborations



Thank you!

SoC in Accelerator Complex



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