Enclustra

The perfect FPGA based System-on-Module for every application

June 2021

Diana Ungureanu

Manager, BU Standard Platforms

Who is Enclustra?

- Founded in 2004, based in Zurich, >50 employees
- Pioneer in SOM development -> first product in 2008
- Largest offering of FPGA and SOC modules on the market
  - 30+ standard products
  - 90+ product models
  - Three product families
- Over 1000 customers in 69 countries
- Sold over 70 000 modules
- Offering Modules and Design Services
  - Customized to your needs

Who is Enclustra?

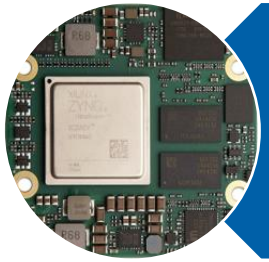
Enclustra Global Offices & Sales Agents

Distribution: Avnet, Digi-Key and Enclustra Partners

Our Value to our Customers

- We help customers to:
  - Reduce time to market (TTM)
  - Reduce total cost of ownership (TCO)
  - Differentiate their products
- We deliver:
  - Highest proven quality
  - Standard and custom-made products
  - One of the largest SOM product offerings on the market

Our Offering



System on Modules

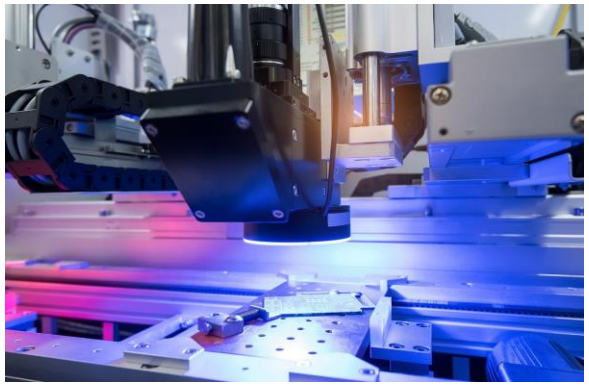
Design Services

IP Cores

SOM Key Target Markets

ROBOTICS

VISION



SECURITY

MEASUREMENT

INDUSTRIAL

MEDICAL

Enclustra Design Services

- Team of 30 highly skilled engineers
- 200+ years of extensive experience in FPGA technology
- Supporting all areas of FPGA system design
  - High-speed FPGA hardware
  - HDL firmware
  - Embedded software
- Wide range of application areas
  - Wired and Wireless Comms
  - Smart camera
  - Drive/Motion control
  - Embedded interfaces

Enclustra IP Cores

Communications/Networking

IP Core		Description	Status
FPGA Manager IP Solution		Enclustra's FPGA Manager solution allows for easy and efficient data transfer between a host and a FPGA over different interface standards like USB 2.0/3.0, Gigabit Ethernet and PCI Express.	**Available now!**
UDP/IP Ethernet IP Core		Enclustra's UDP/IP Ethernet IP core easily enables FPGA-based subsystems to communicate with other subsystems via Ethernet, using the UDP protocol.	**Available now!**

Digital Signal Processing

IP Core		Description	Status
Universal DSP Library		Enclustra's Universal DSP Library provides efficient FPGA implementations of the most common digital signal processing components. It allows building signal processing chains rapidly using Vivado's Block Design GUI, or by direct VHDL.	Available soon!

Motion Control

IP Core		Description	Status
Universal Drive Controller		This IP core enables the independent position and/or velocity control of up to 8 DC, BLDC or stepper motors directly from the FPGA.	**Available now!**

SoPC/Embedded Computing

IP Core		Description	Status
Display Controller		This IP core enables the easy integration of displays into FPGA-based systems. With Linux, even multi-touch displays are supported.	**Available now!**

Miscellaneous

IP Core		Description	Status
Stream Buffer Controller		A versatile stream to memory-mapped DMA bridge.	**Available now!**

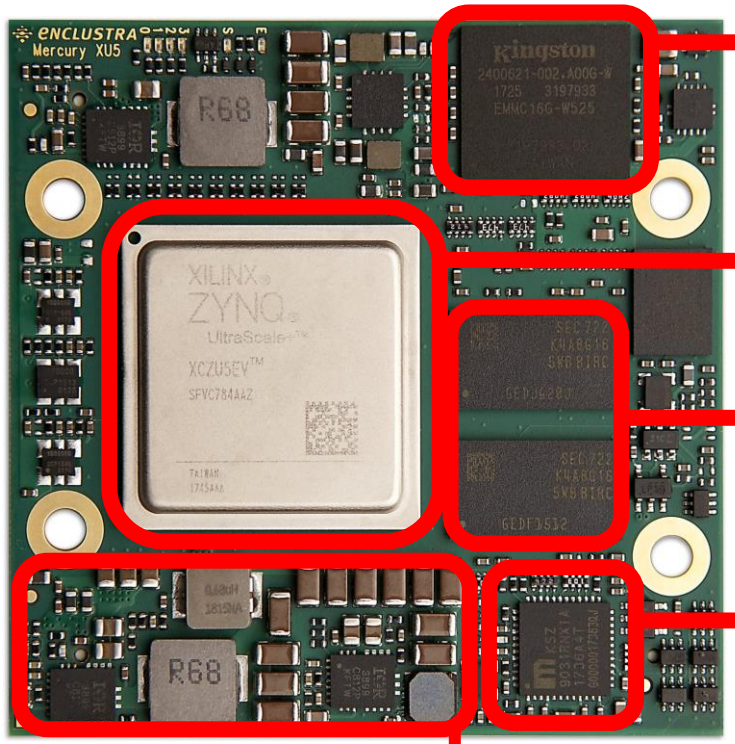
Everything FPGA

Product Overview

June 2021

Enclustra SOM

FRONT SIDE



Flash

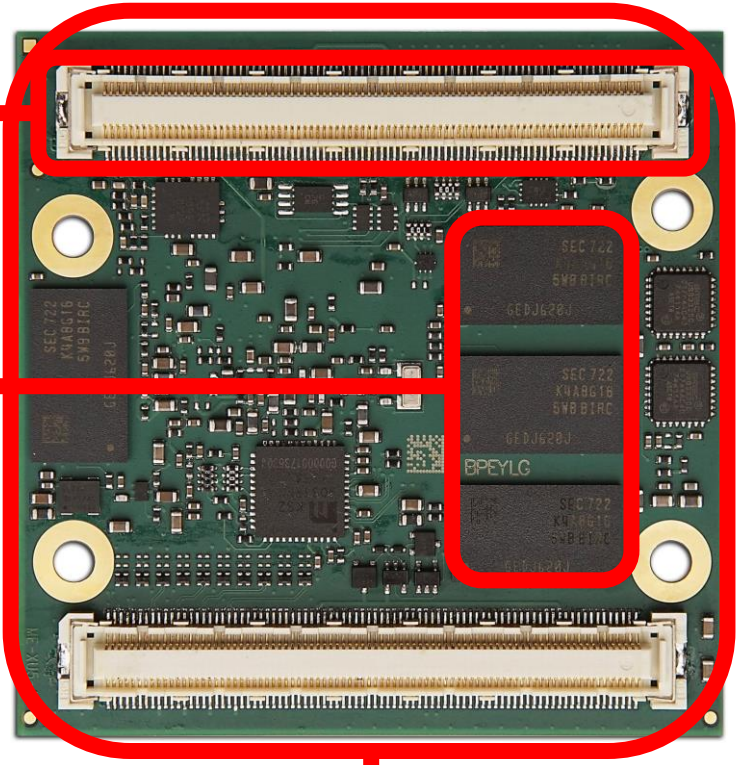
FPGA/SoC
Pre-built Linux and build environment

DDR

Standard interfaces (e.g. Ethernet PHY, USB PHY, etc.)

Power supply
Clock

REAR SIDE

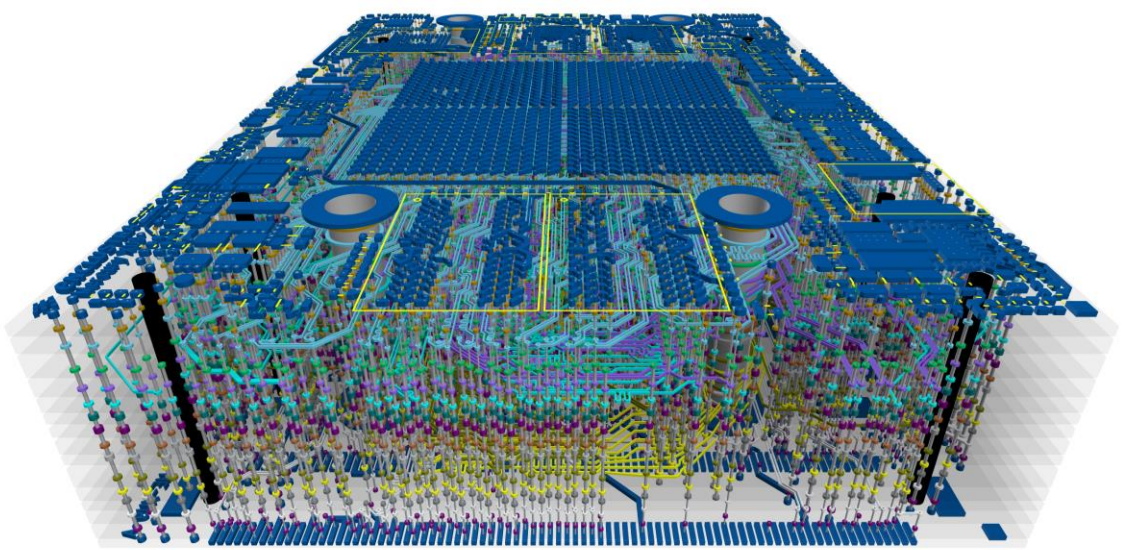


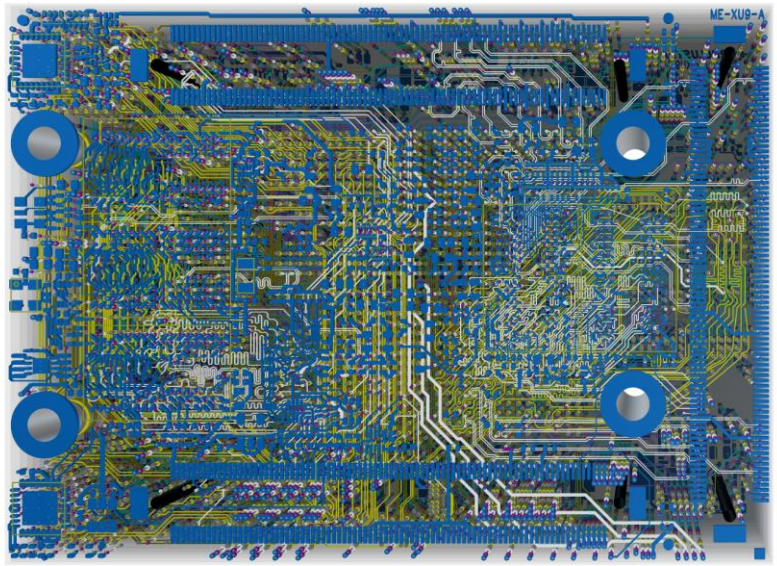
High density connectors

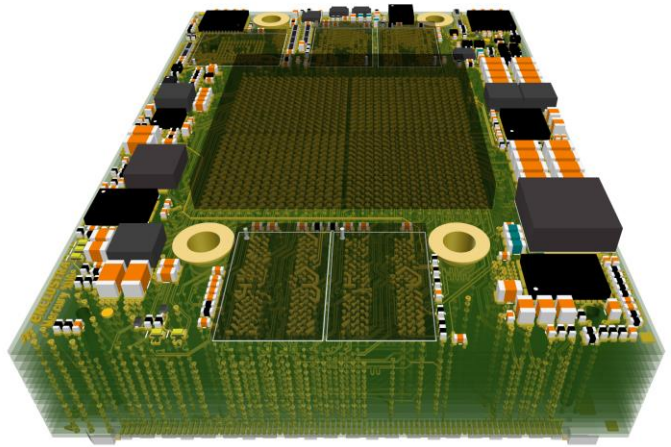
DDR

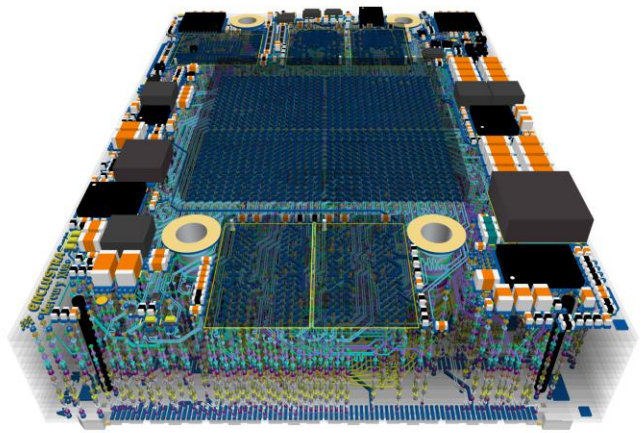
Compact form factor

We Master Complexity in SOM









SOM cross-compatibility and base board support

Increase market share through supporting different FPGA sizes on a single base board

Families

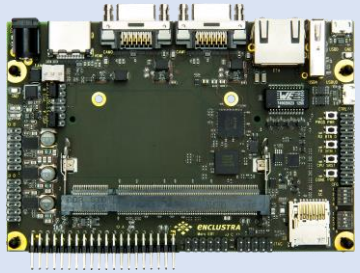
Mars

Mercury

Mercury+

Base Boards

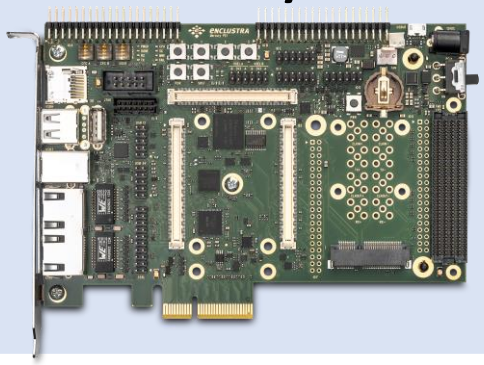
Mars EB1



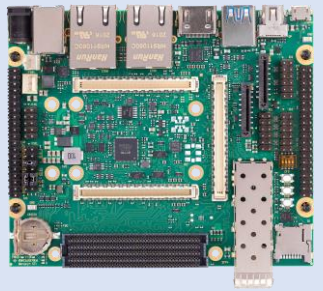
Mars PM3

Mars ST3

Mercury+ PE1



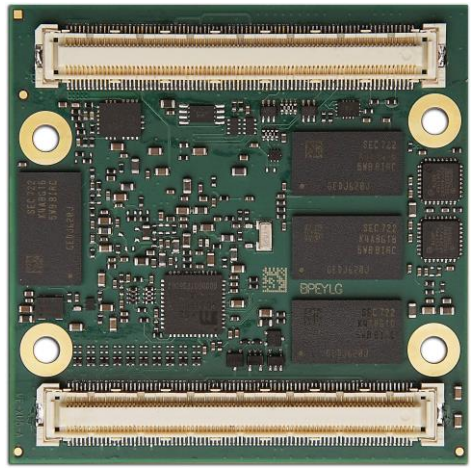
Mercury+ ST1



Enclustra SOM Families

Mars

Mercury



Mercury+

Andromeda

Enclustra SOM Families

	Dimensions [mm]	I/O Pins [max]	Transceivers [max]	Transceiver Speed [max]	SOMs [#]	Models [#]	Baseboard models [#]
Mars	67.6 x 30	108	4	5 Gbps	6	12	3
Mercury	56/64/72 x 54	178	8	15 Gbps	6	21	5
Mercury+	74 x 54	294	16	15 Gbps	8	33	5
Andromeda	56 x 40 68 x 52 80 x 64	780	84	25 Gbps NRZ (56 Gbps PAM4)	1	2	Available soon

Mars SOM

Xilinx

XU3

Zynq Ultrascale+ ZU2-ZU3

ZX3

Zynq 7000 7020

ZX2

Zynq 7000 7010-7020

SoC

AX3

Artix-7 35-50-100

MX1

Spartan-6 45LX

FPGA

Intel SoC

MA3

Cyclone V SoC 5CSXFC6

Mercury/Mercury+ Xilinx SOM

Mercury

ZX5

Zynq 7000

7015-7030

ZX1

Zynq 7000

7030-7035-7045

Mercury+

XU5

Zynq Ultrascale+

ZU2-ZU3-ZU4-ZU5

XU8

Zynq Ultrascale+

ZU4-ZU5-ZU7

XU1

Zynq Ultrascale+

ZU6-ZU9-ZU15

XU6

Zynq Ultrascale+

ZU2-ZU3-ZU4-ZU5

XU9

Zynq Ultrascale+

ZU4-ZU5-ZU7

XU7

Zynq Ultrascale+

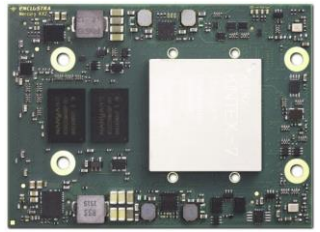
ZU6-ZU9-ZU15

SoC

KX1

Kintex 7

160-325



KX2

Kintex 7

160-410

FPGA

Enclustra Mercury SOM Comparison

Module	XU1	XU5	XU6	XU7	XU8	XU9
ZU+ Devices	6/9/15	2/3/4/5	2/3/4/5	6/9/15	4/5/7	4/5/7
Sys. logic cells (k)	469-747	103-256	103-256	469-747	192-504	192-504
Main DDR4 PS/PL Bus Width (Bits) w/ECC(ECC)	2-8 GB 64(ECC)	1-8 GB 32/64(ECC)	1-8 GB 32/64(ECC)	2-8 GB 64(ECC)	2-8 GB 64(ECC)	2-8 GB 64(ECC)
Secondary DDR4 PL Bus Width (bits), w/out ECC	- 	0.5-2 GB 16	- 	1-4 GB 32	1-4 GB 32	2-8 GB 64
PS MGT (GTR)	4	0/4[2)]	4	4	4	4
PL MGT (GTH)	12/16[1)]	0/4[2)]	0/4	16	16	16
H.264/265 Codec (VCU)	-	-/yes	-/yes	-	yes	yes
PCIe Gen3 Hard-IP	-	-/yes	-/yes	-	yes	yes
PL I/O (+PS I/O)	200[1)] (+14)	144[2)] (+14)	240 (+14)	122 (+14)	122 (+14)	78 (+14)
Availability	now	now	2Q2021	now	now	now

1) XU1-…-G1 Version has 16 MGT but 20 User I/O less (=180)

2) XU5-…-G1 Version has 4 PS + 4 PL MGT but 20 User I/O less (=124)

Mercury/Mercury+ Intel and Microchip SOM

Mercury

SA1

Cyclone V SoC
5CSXFC6

Mercury+

SA2

Cyclone V SoC 5CSTFD6

AA1

Arria 10 SoC

10AS027- 10AS048

Intel SoC

CA1

Cyclone IV

EP4CE75 - EP4CE115

Intel FPGA

MP1

PolarFire SoC
250T - 460T

Microchip SoC
(SOM in development)

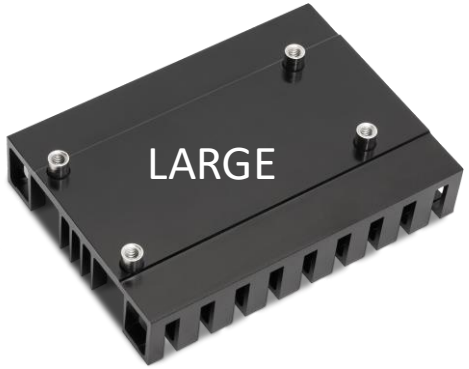
Cooling solutions – Mercury/Mercury+ SOM

Supporting:

Mercury / Mercury+

XU5 – XU6 – ZX1 – ZX5 (Xilinx)

SA1 – SA2 – CA1 (Intel)



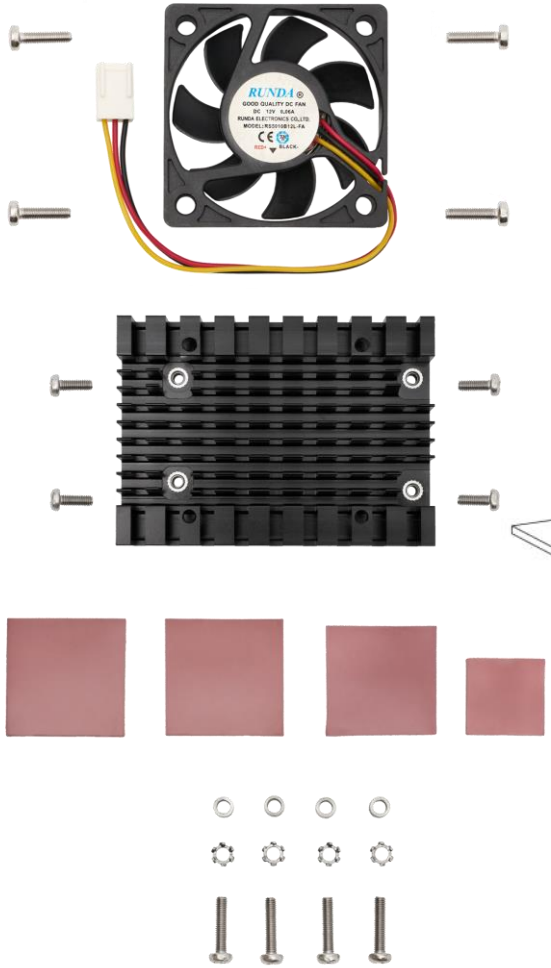
Supporting:

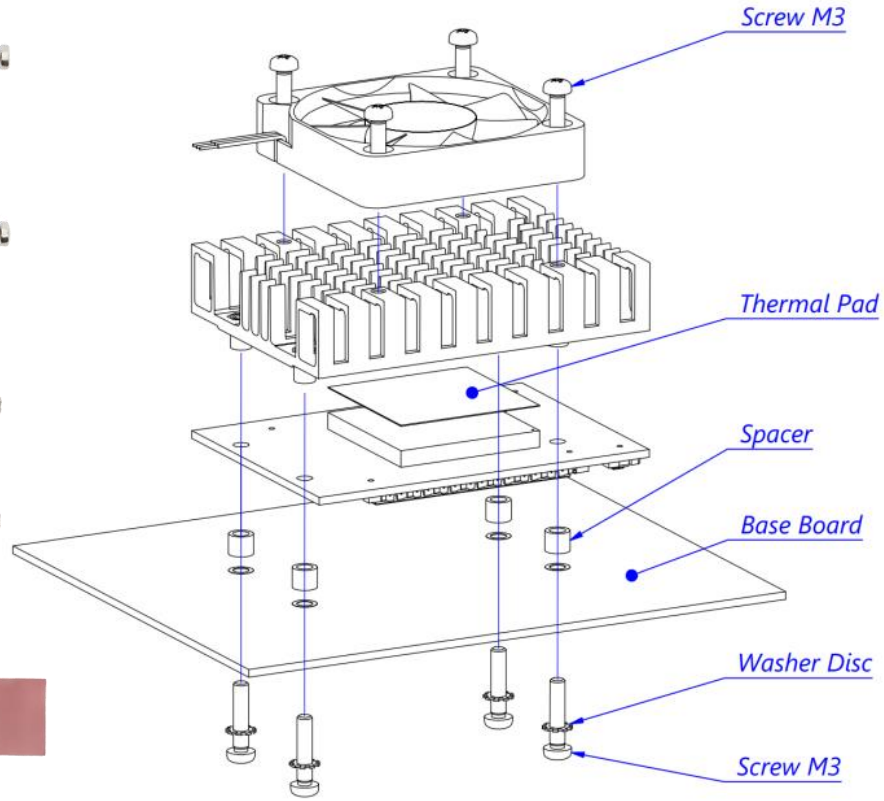
Mercury+

XU1 – XU7 – XU8 – XU9 – KX2 (Xilinx)

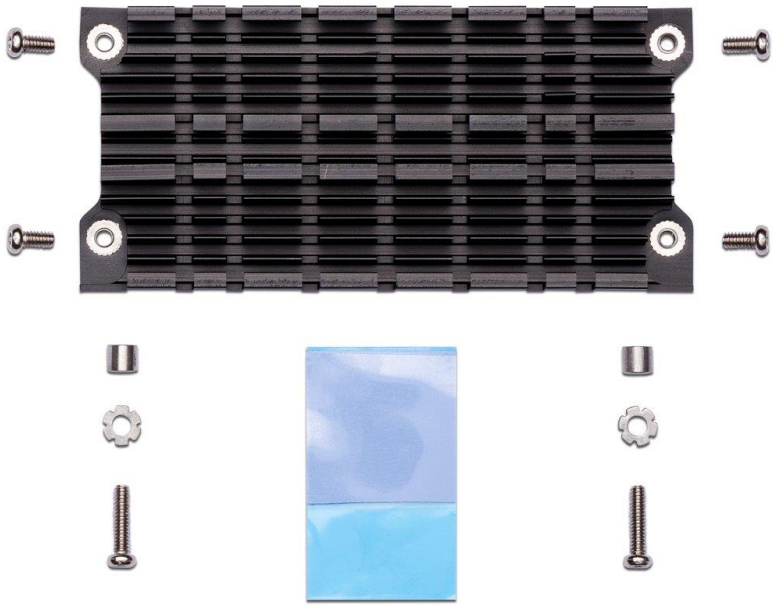
AA1 (Intel)

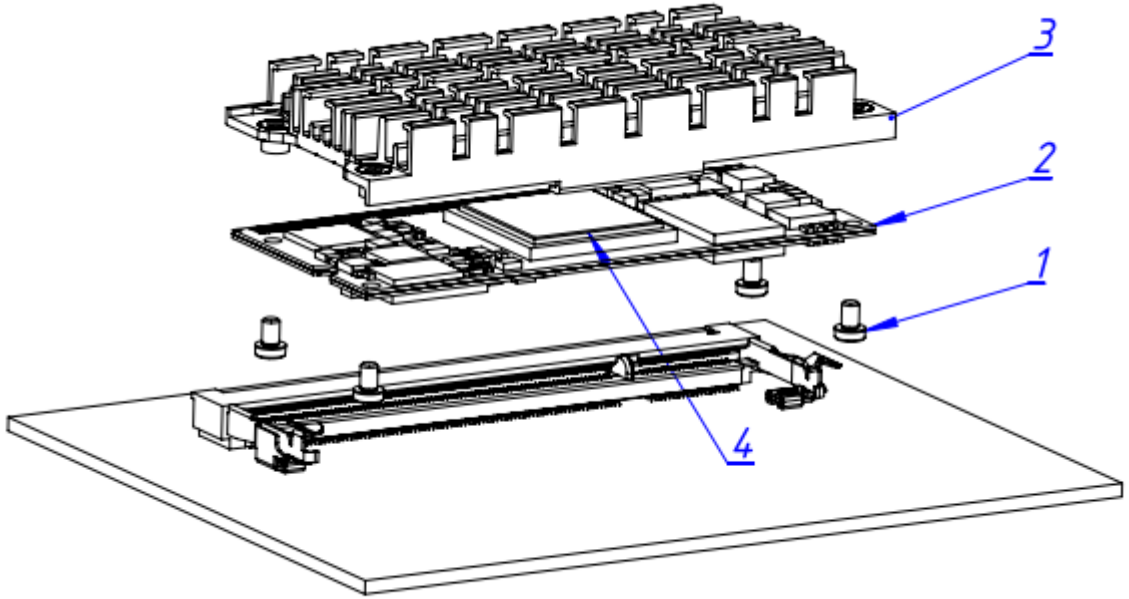
MP1 (Microchip)





Cooling solutions – Mars SOM





Supporting:

Mars

XU3 – ZX2 – ZX3 – AX3 (Xilinx)

MA3 (Intel)

We offer

- User Manuals
- Revision History
- User Schematics
- Pin Connection Guidelines
- 3D Models
- Module footprints for PADS, Altium, Orcad, Eagle
- Reference Designs
- Software (OS, Configuration, etc.)
- Application Notes
- Technical Support
- Design Services (paid service)

ENCLUSTRA FPGA SOLUTIONS

Mercury+ XU9 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury+ XU9 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury+ XU9 SoC module.

Summary

This document first gives an overview of the Mercury+ XU9 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-XU9	Mercury+ XU9 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-463-001	03	16.02.2021

Approval Information	Name	Position	Date
Written by	DIUN, MMOS	Design Engineer	20.05.2019
Verified by	MMOS, GKOE	Design Expert	24.05.2019
Approved by	DIUN	Manager, BU SP	16.02.2021

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2 Module Description

2.1 Block Diagram

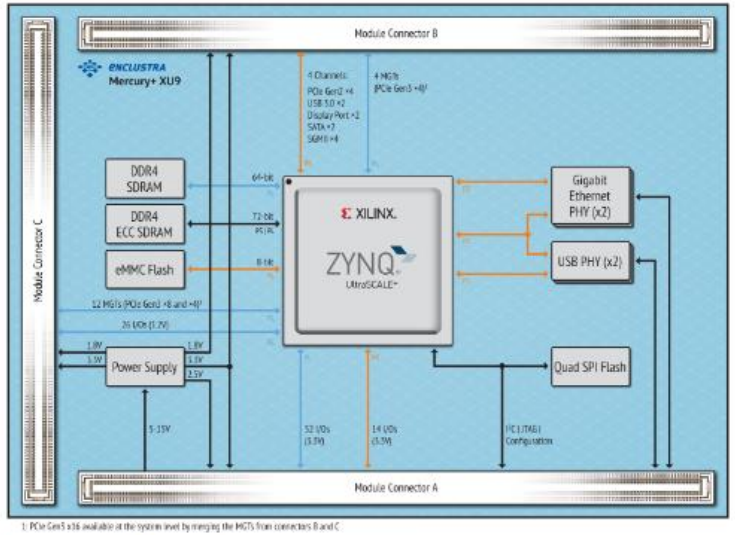

Figure 1: Hardware Block Diagram

The main component of the Mercury+ XU9 SoC module is the Xilinx Zynq Ultrascale+ MPSoC device. All available I/O pins (which are not routed to on-board peripherals) are connected to the Mercury+ module connector, making 92 regular user I/Os available to the user. Further, twenty MGT pairs are available on the module connector, making possible the implementation of several high-speed protocols such as PCIe Gen3 ×16, PCIe Gen2 ×4 and USB 3.0 (simultaneous usage of all the interfaces is limited to the available hardware resources i.e. number of transceivers and lane mapping).

The MPSoC device can boot from the on-board QSPI flash, from the eMMC flash or from an external SD card. For development purposes, a JTAG interface is connected to Mercury module connector.

The available standard configurations include a 16 GB eMMC flash, a 64 MB quad SPI flash, up to 4 GB DDR4 SDRAM with ECC connected to the Processing System (PS) and up to 2 GB DDR4 SDRAM connected to the Programmable Logic (PL).

Further, the module is equipped with two Gigabit Ethernet PHYs and two USB 2.0 PHYs, making it ideal for communication applications.

A real-time clock is available on the Xilinx Zynq Ultrascale+ MPSoC device.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 47 indicates the absolute maximum ratings for Mercury+ XU9 SoC module. The values given are for reference only; for details please refer to the Zynq UltraScale+ MPSoC, DC and AC Switching Characteristics Datasheet [20].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 16	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	0 to 3.6	V
VCC_IO_BN VCC_IO_BO	Output drivers supply voltage relative to GND	-0.5 to 3.4	V
VCC_CFG_MIO	Output drivers supply voltage relative to GND	-0.5 to 3.63	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCO}+0.5	V
Temperature	Temperature range for extended temperature modules (E)* Temperature range for industrial modules (I)*	0 to +85 -40 to +85	°C °C

Table 47: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 48 indicates the recommended operating conditions for Mercury+ XU9 SoC module. The values given are for reference only; for details please refer to the Zynq UltraScale+ MPSoC, DC and AC Switching Characteristics Datasheet [20].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	4.75 to 15.75	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	2.7 to 3.6	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCO}+0.2	V
Temperature	Temperature range for extended temperature modules (E)* Temperature range for industrial modules (I)*	0 to +85 -40 to +85	°C °C

Table 48: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

Product Deliverables – Revision History

ENCLUSTRA FPGA SOLUTIONS

Mercury+ XU8 SoC Module

Known Issues and Changes

Revision 2.1

Purpose

The purpose of this document is to describe the known issues and the revision changes related to the Mercury+ XU8 SoC module.

Product Information	Code	Revision	Name
Product	ME-XU8	Mercury+ XU8 R2.1	Mercury+ XU8 SoC Module

Document Information	Reference	Version	Date	Author
Reference / Version / Date	D-0000-466-001	02	18.11.2019	DIUN, MMOS

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1 Known Issues

In addition to the erratas from the components manufacturers, Enclustra is aware of the following issues with the Mercury+ XU8 R2.1 module.

VCU power consumption limited to 4 A	
Description	The power consumption of the video codec unit (VCU) on the VCC_INT_VCU rail is limited to 4 A. This is due to current carrying limitations of a used component.
Workaround	There is no workaround available.
Status	This issue will be fixed in the next revision (R3).

2 Functional Changes

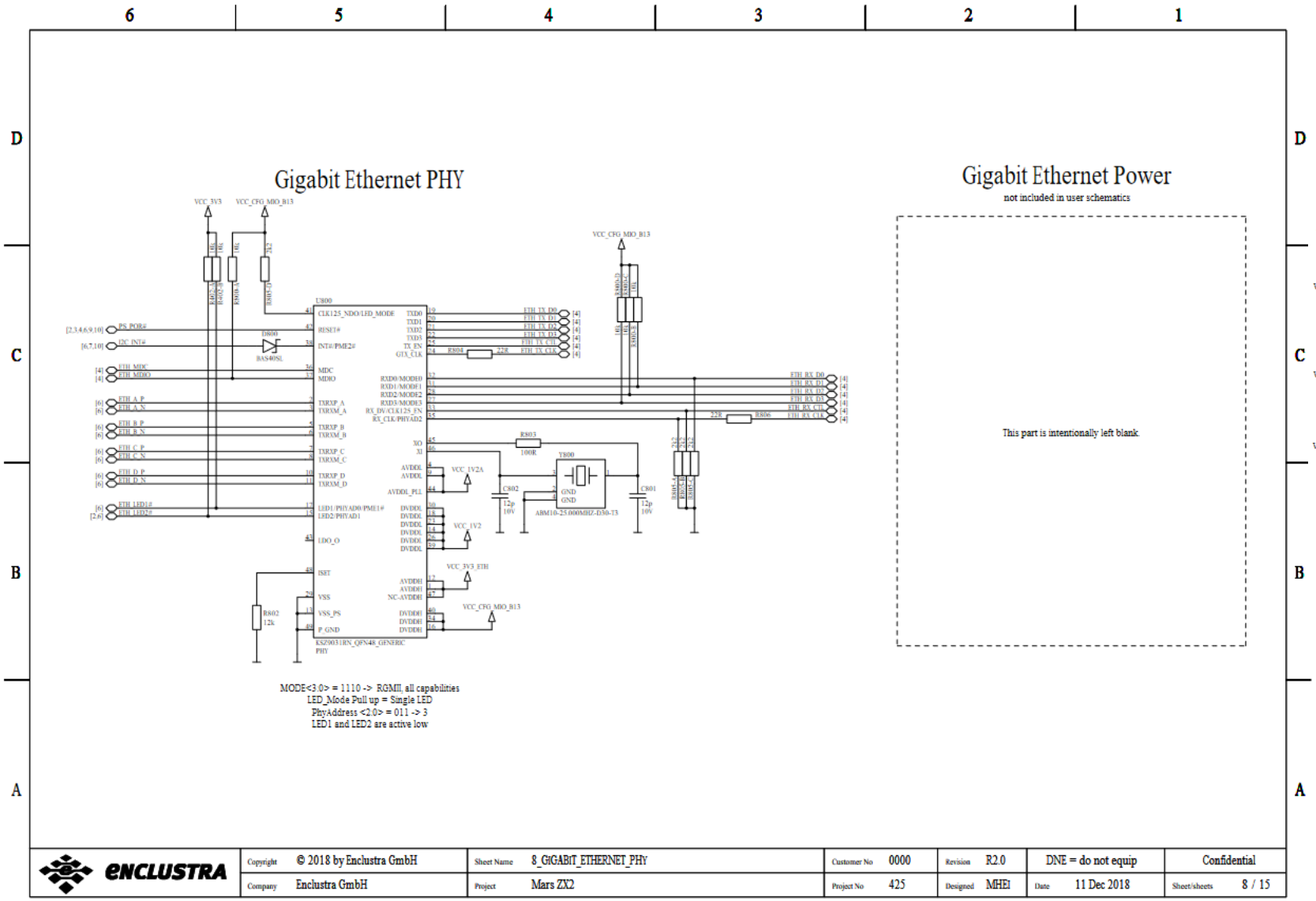
In addition to changes related to manufacturing process optimization and signal integrity improvements, the following functional changes were made from the Mercury+ XU8 SoC module revision R1.1 to R2.1.

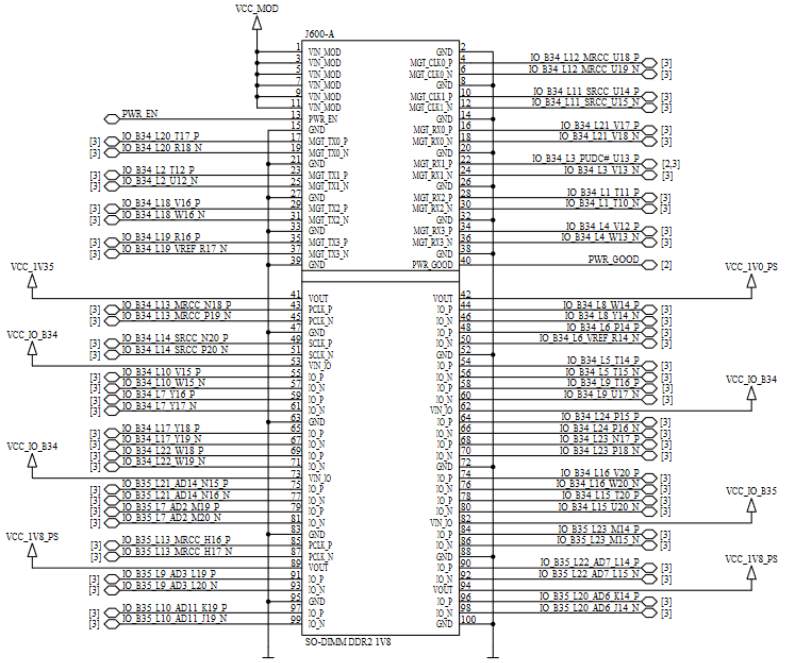
Added voltage monitoring output on module connector C	
Description	A new voltage monitoring output was added on the module connector pin C-8. This can be used to measure the on-board 1.2 V voltage, VCC_1V2.

2.5 V supply is controllable by the PWR_EN signal	
Description	The 2.5 V supply (VCC_2V5) is now controllable by the PWR_EN signal. In this case, no additional power sequencing circuits are required on the base board. Please refer to the Mercury+ XU8 SoC module user manual for details.

Optional JTAG boot mode support	
Description	Starting with revision 2, support for JTAG boot mode has been added to increase the usability of the module with Xilinx tools, for example for flash programming or bitstream loading. Please refer to the Mercury+ XU8 SoC module user manual for details on JTAG boot mode.

Product Deliverables – User Schematics





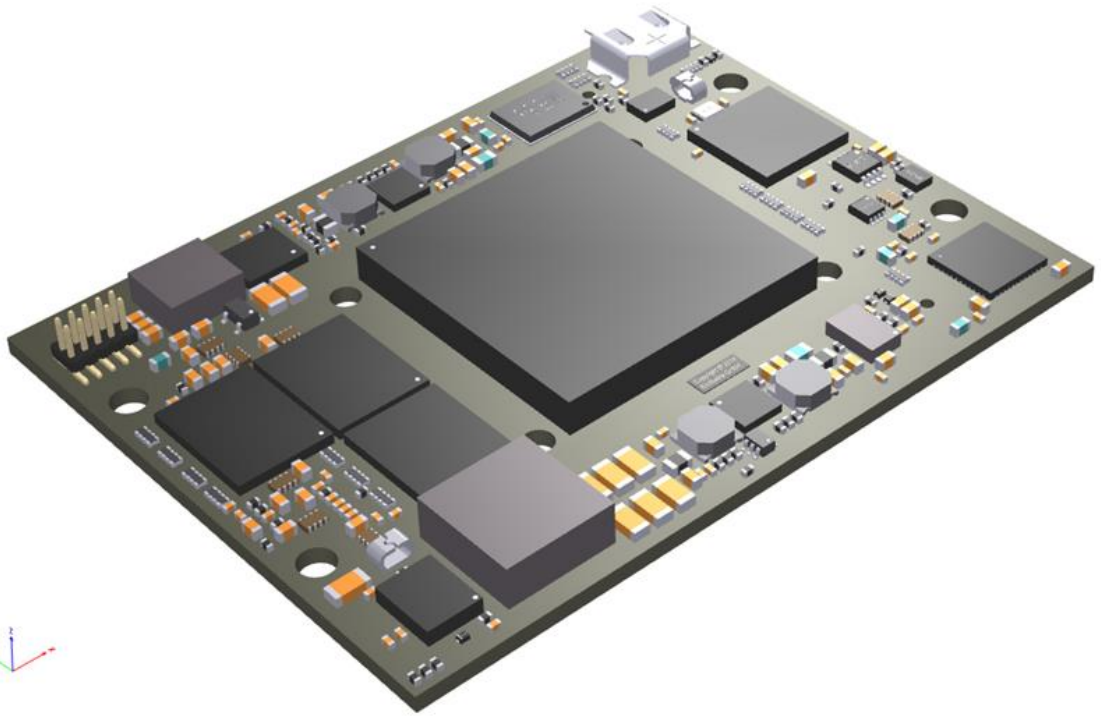
Product Deliverables – Module Pin Connection Guidelines

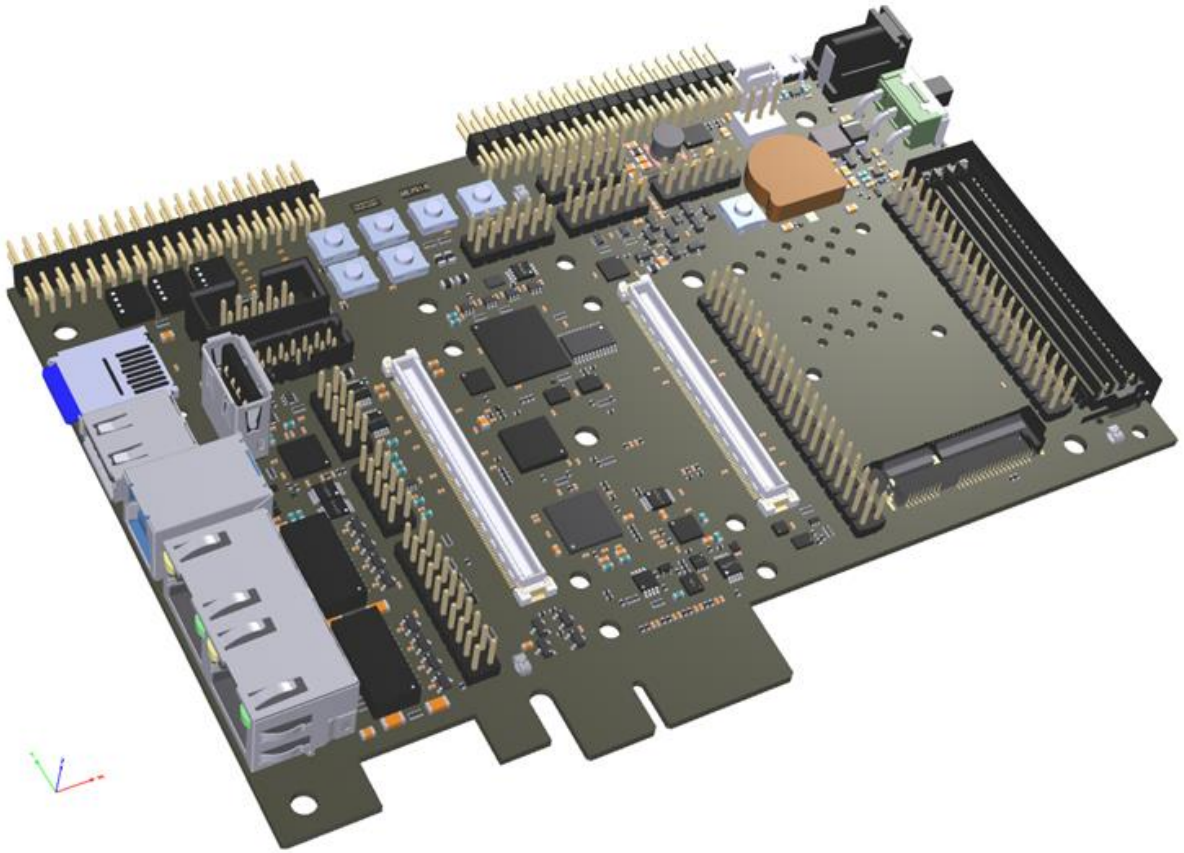
Mercury Mars Module Pin Connection Guidelines

Date Feb 12, 2021

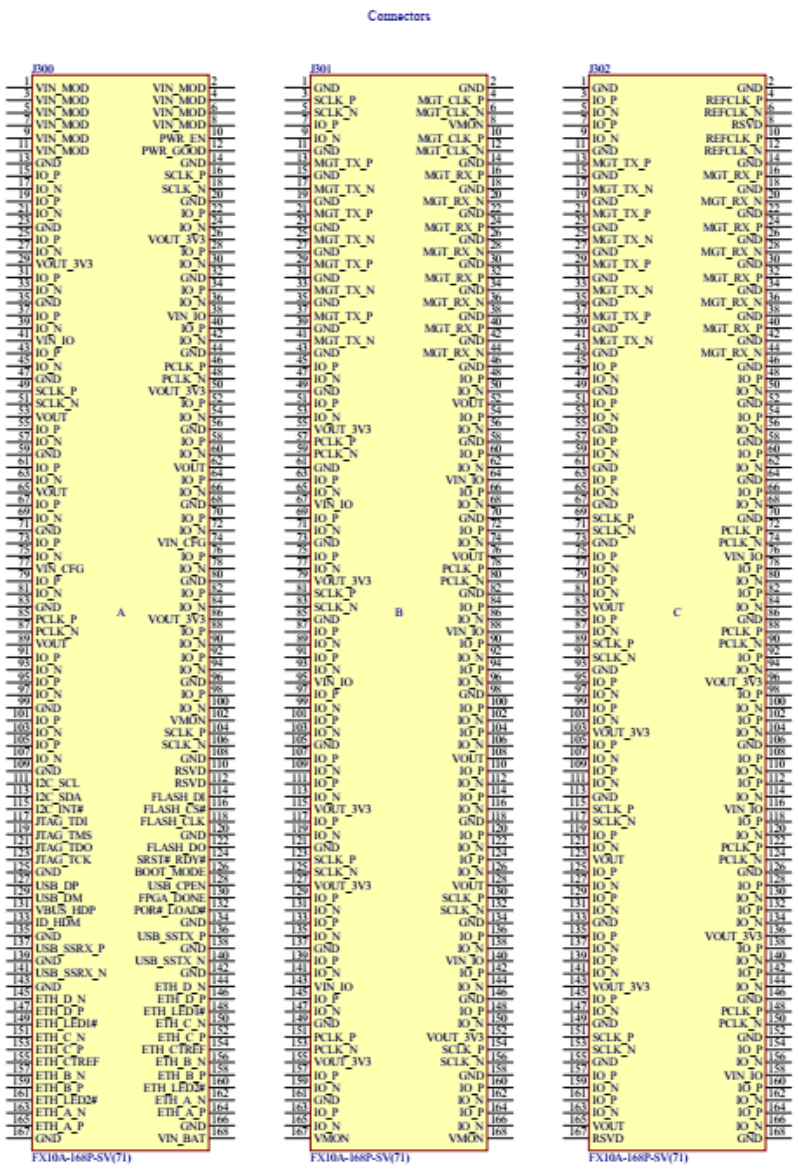
Pin Type	Direction (*1)	Voltage Level	Description	Comments
General				
All pins				Applying a negative voltage or a voltage higher than the specified maximum, even for a short period of time, may damage the module permanently. The module does not have any protection against these hazards.
				The ESD protection level available on each module pin is module- and pin-specific. Enclustra recommends adding ESD protection circuitry to all signals connected to an externally-accessible connector.
User IO pins				
IO_P IO_N	Bidirectional	Bank-specific	FPGA I/O pin	Please check the supported IO standard's compatibility with the FPGA/SoC tools. Some banks may only have a restricted voltage range, e.g. 1.8 V.
				Some FPGA/SoC families have restrictions when LVDS and single-ended signals are placed on the same bank. The FPGA/SoC vendor provides further information. The best way to check your pinout is to perform a full compilation of the FPGA/SoC design using the vendor tools.
				Some user I/O pins may have additional functionalities, such as analog input or PCIe reset, or PUDC, or reference voltage input.
				Some modules may have unconnected pins.
				Some FPGA/SoC architectures may have higher capacitance on some pins (e.g. VREF) and therefore offer lower performance on these pins.
				Some modules may not support differential driver or receiver functionality on all of the IO_P/N pin pairs. They may only be usable for single ended I/O standards.
				Some FPGA/SoC families may not support terminating differential signals on all pin pairs inside the FPGA/SoC. External termination on the base board could be required. This may reduce the performance of such pairs due to the trace stubs slightly.
				Certain modules contain differential termination resistors on the module on some of the IO_P/N pin pairs. These terminations cannot be switched off. The IO_P pin could be used as single-ended I/O with limited performance. The IO_N pin should be tri-stated in the FPGA/SoC design.
				Most modules have pull-ups on all IO_P/N pins before and during configuration. These pull-ups cannot be switched off.
				The voltage on these pins may never exceed the voltage on the corresponding bank supply voltage. Check the FPGA/SoC data sheet for details.
			PUDC pin	Some modules have the pull-up-during-configuration pin exposed to the user connector. Some modules apply a 1 kOhm pull-down resistor during configuration (FPGA_DONE is low).
			Analog I/O pin	Some modules may have analog I/O functionality on some of the IO_P/N pins.
			System I/O pin	Some modules may have system peripheral pins on some of the IO_P/N pins. These pins usually cannot be driven from inside the programmable logic.
PCLK_P PCLK_N	Bidirectional	Bank-specific	Primary clock input	When designing a new module, we try to put global clock input pins on PCLK_P (if single-ended) or PCLK_P/N (if differential) pins.
				The use of PCLK_N as a single-ended clock may not be supported by some FPGA/SoC families.
				Some FPGA/SoC families may not support terminating differential signals on all pin pairs inside the FPGA/SoC. External termination on the base board could be required. This may reduce the performance of such pairs, due to the trace stubs slightly.
				Some FPGA/SoC families may not support using clock input pins as outputs.
			Other pin	On some modules, these pins may not be clock capable. In this case, refer to the description of the IO_P/N pin type.
SCLK_P SCLK_N	Bidirectional	Bank-specific	Secondary clock input	When designing a new module, we try to put any remaining clock input pins on SCLK_P (if single-ended) or SCLK_P/N (if differential) pins.
				Some of these clock pins may only be usable as regional clocks, restricting the location of synchronous elements within the FPGA/SoC.
				The use of SCLK_N as a single-ended clock may not be supported by some FPGA/SoC families.
				Some FPGA/SoC families may not support terminating differential signals on all pin pairs inside the FPGA/SoC. External termination on the base board could be required. This may reduce the performance of such pairs due to the trace stubs slightly.

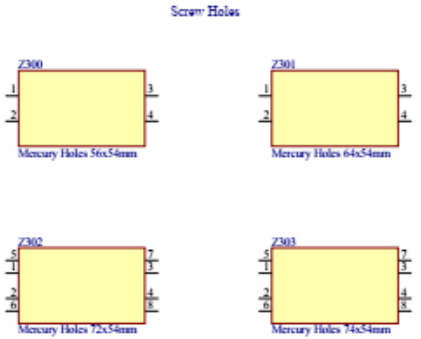
Product Deliverables – 3D Models

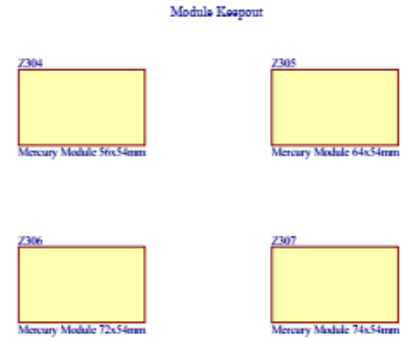


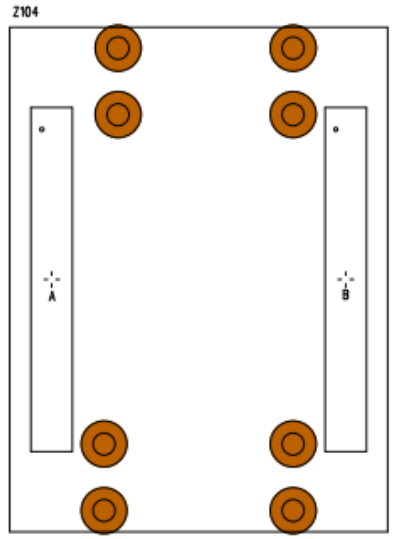


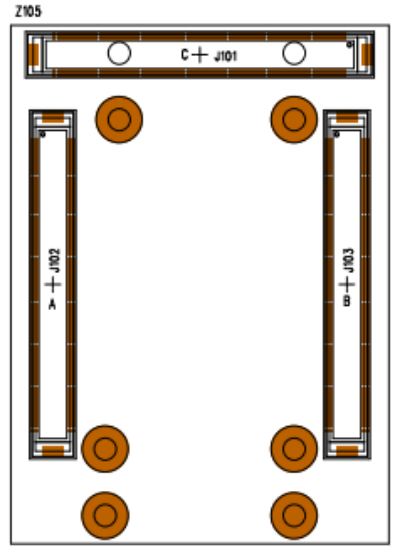
Product Deliverables – Module Symbols and Footprints







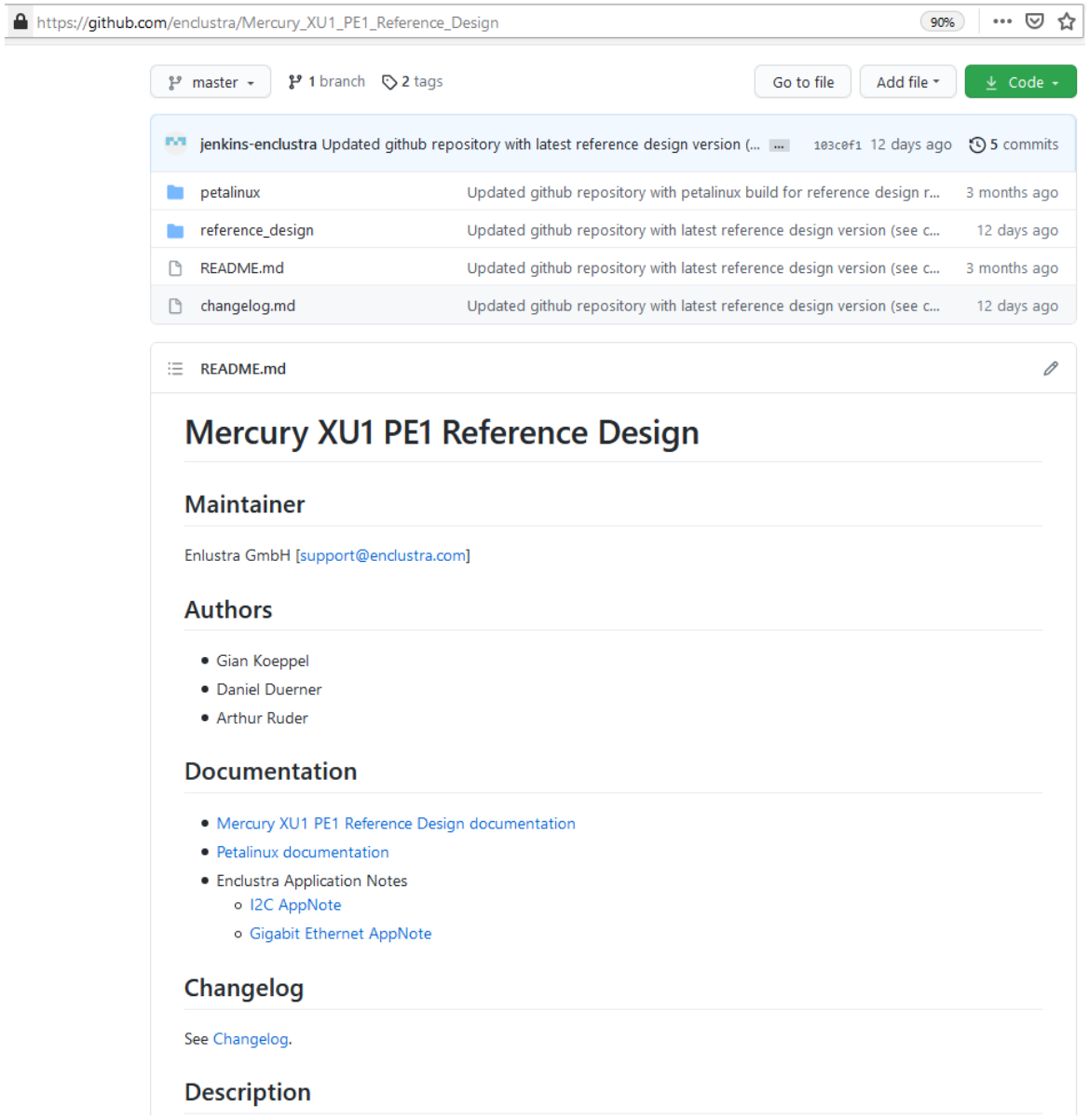




Supporting :

- PADS
- ALTIUM
- ORCAD
- EAGLE

Product Deliverables – Reference Designs



https://github.com/enclustra/Mercury_XU1_PE1_Reference_Design

master · 1 branch · 2 tags · Go to file · Add file · Code

jenkins-enclustra Updated github repository with latest reference design version (... 103c0f1 12 days ago 5 commits

petalinux	Updated github repository with petalinux build for reference design r...	3 months ago
reference_design	Updated github repository with latest reference design version (see c...	12 days ago
README.md	Updated github repository with latest reference design version (see c...	3 months ago
changelog.md	Updated github repository with latest reference design version (see c...	12 days ago

README.md

Mercury XU1 PE1 Reference Design

Maintainer

Enlustra GmbH [support@enclustra.com]

Authors

- Gian Koeppel
- Daniel Duerner
- Arthur Ruder

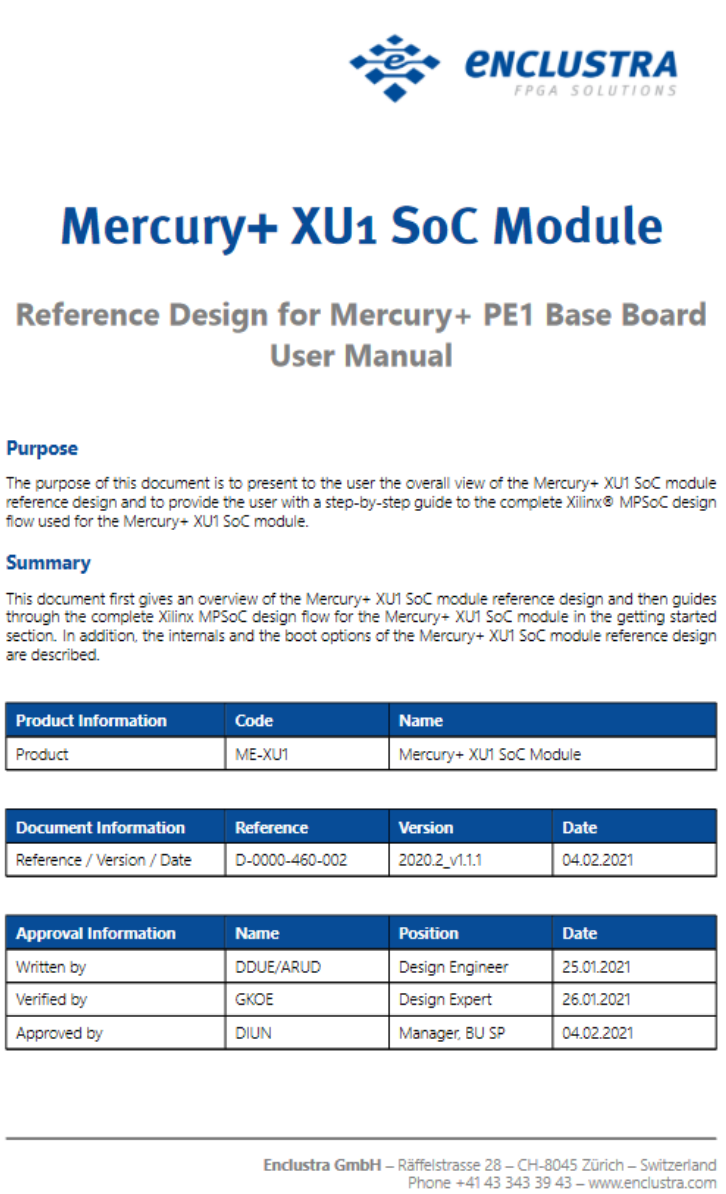
Documentation

- Mercury XU1 PE1 Reference Design documentation
- Petalinux documentation
- Enclustra Application Notes
  - I2C AppNote
  - Gigabit Ethernet AppNote

Changelog

See Changelog.

Description



ENCLUSTRA FPGA SOLUTIONS

Mercury+ XU1 SoC Module

Reference Design for Mercury+ PE1 Base Board User Manual

Purpose

The purpose of this document is to present to the user the overall view of the Mercury+ XU1 SoC module reference design and to provide the user with a step-by-step guide to the complete Xilinx® MPSoC design flow used for the Mercury+ XU1 SoC module.

Summary

This document first gives an overview of the Mercury+ XU1 SoC module reference design and then guides through the complete Xilinx MPSoC design flow for the Mercury+ XU1 SoC module in the getting started section. In addition, the internals and the boot options of the Mercury+ XU1 SoC module reference design are described.

Product Information	Code	Name
Product	ME-XU1	Mercury+ XU1 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-460-002	2020.2_v1.1.1	04.02.2021

Approval Information	Name	Position	Date
Written by	DDUE/ARUD	Design Engineer	25.01.2021
Verified by	GKOE	Design Expert	26.01.2021
Approved by	DIUN	Manager, BU SP	04.02.2021

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- Xilinx SOM reference designs and PetaLinux BSPs available on GitHub

Product Deliverables – Reference Designs

ENCLUSTRA FPGA SOLUTIONS

Mercury+ AA1 SoC Module

Reference Design for Mercury+ PE1 Base Board User Manual

Purpose

The purpose of this document is to present to the user the overall view of the Mercury+ AA1 SoC module reference design and to provide the user with a step-by-step guide to the complete Intel® SoC design flow used for the Mercury+ AA1 SoC module.

Summary

This document first gives an overview of the Mercury+ AA1 SoC module reference design and then guides through the complete Intel SoC design flow for the Mercury+ AA1 SoC module in the getting started section. In addition, the internals and the boot options of the Mercury+ AA1 SoC module reference design are described.

Product Information	Number	Name
Product	ME-AA1	Mercury+ AA1 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-419-002	02	21.02.2018

Approval Information	Name	Position	Date
Written by	DIUN	Design Engineer	29.11.2017
Verified by	GKOE	Technical Expert	16.01.2018
Approved by	RPAU	Quality Manager	21.02.2018

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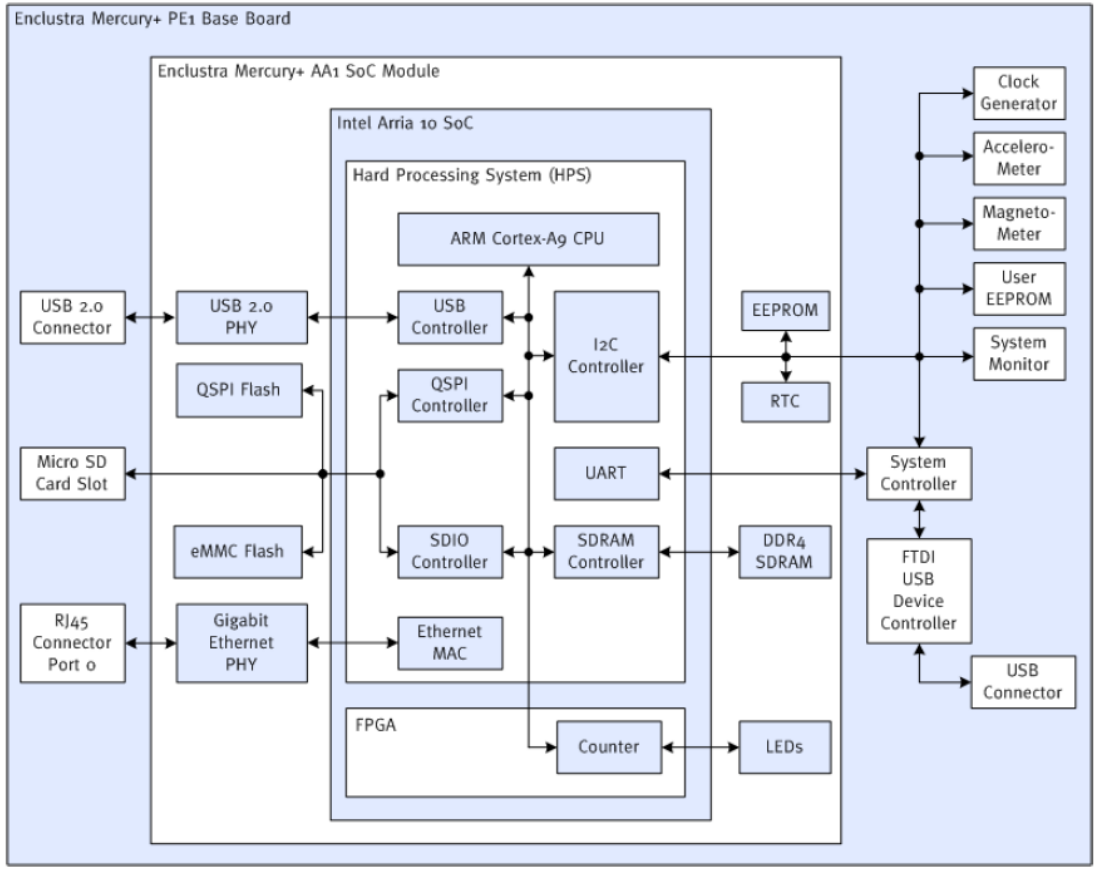

- Intel SOM reference designs available on Enclustra download site

Product Deliverables – I2C Application Note

https://github.com/enclustra/I2CAppNote/blob/master/I2CApplicationNote.md

94 lines (81 sloc) | 7.65 KB

The types of I2C chips used in Enclustra hardware are described in more deta
on Enclustra hardware. The examples include sample code for all I2C devices

Table of contents

Chapter 3 - Bare metal

This chapter describes the usage of the aforementioned devices with the I2C bus and provides sample code snippets for a bare metal application. It is assumed that the hardware used is set up correctly using the corresponding user manual for the hardware in use. The source files for the provided code snippets are also available, e.g. I2cInterface.h.

```
/**
* \brief I2C subaddress modes.
*/
typedef enum
{
    EI2cSubAddressMode_None , ///< No subaddress
    EI2cSubAddressMode_OneByte , ///< One -byte subaddress
    EI2cSubAddressMode_TwoBytes ///< Two -byte subaddress
} EI2cSubAddressMode_t;

/**
* \brief Perform any required initialisation for I2C operations.
*
* @return Result code
*/

EN_RESULT InitialiseI2cInterface ();

/**
* \brief Perform a read from the I2C bus.
*
* \param[in] deviceAddress The device address
* \param[in] subAddress Register subaddress
* \param[in] subAddressMode Subaddress mode
* \param[in] numberOfBytesToRead The number of bytes to read
* \param[out] pReadBuffer Buffer to receive read data
* \returns Result code
*/
EN_RESULT I2cRead(uint8_t deviceAddress ,
    uint16_t subAddress ,
    EI2cSubAddressMode_t subAddressMode ,
    uint32_t numberOfBytesToRead ,
    uint8_t* pReadBuffer);
```

Introduction

The following chapters and sections describe in detail the hardware setup for enabling Gigab
PHY used on all current Enclustra modules is the Microchip KSZ9031RNX.

Table of contents

References

- Microchip KSZ9031RNX data sheet
- Xilinx LWIP App Note XAPP1026
- Xilinx LWIP library
- Enclustra MCT
- Enclustra EBE kernel

2.3 - U-boot

In U-boot the necessary driver needs to be selected which automatically configures the PHY delay registers with the default value stated in the data sheet of the KSZ9031RNX. The driver for the **KSZ9031** PHY chip is located in `Device Drivers -> Ethernet PHY (physical media interface) support -> Micrel Ethernet PHYs support -> Micrel KSZ90x1` family support.

The MDIO registers can also be accessed and written to in U-boot. The commands `mdio` and `mii` provide read and write as well as other utility functions to configure the PHY chip. Please refer to the data sheet of the KSZ9031RNX for detailed instructions regarding writing and reading registers.

An example output for the command listing the present Ethernet PHY devices is shown below.

```
zynq-uboot> mdio list
eth0:
3 - Micrel ksz9031 <--> ethernet@e000b000
zynq-uboot>
```

The command `mii info` gives further information as shown below.

```
zynq-uboot> mii info
PHY 0x03: OUI = 0x0885, Model = 0x22, Rev = 0x02, 1000baseT, FDX
zynq-uboot>
```

With `mii dump` the PHY control registers can be accessed as well.

```
zynq-uboot> mii dump 3 0
0.          (1140)                  -- PHY control register --
  (8000:0000) 0.15     =      0    reset
  (4000:0000) 0.14     =      0    loopback
  (2040:0040) 0. 6,13  =    b10    speed selection = 1000 Mbps
  (1000:1000) 0.12     =      1    A/N enable
  (0800:0000) 0.11     =      0    power-down
  (0400:0000) 0.10     =      0    isolate
  (0200:0000) 0. 9     =      0    restart A/N
  (0100:0100) 0. 8     =      1    duplex = full
  (0080:0000) 0. 7     =      0    collision test enable
  (003f:0000) 0. 5- 0  =      0    (reserved)
```

Product Deliverables – PetaLinux BSP for Xilinx SOM

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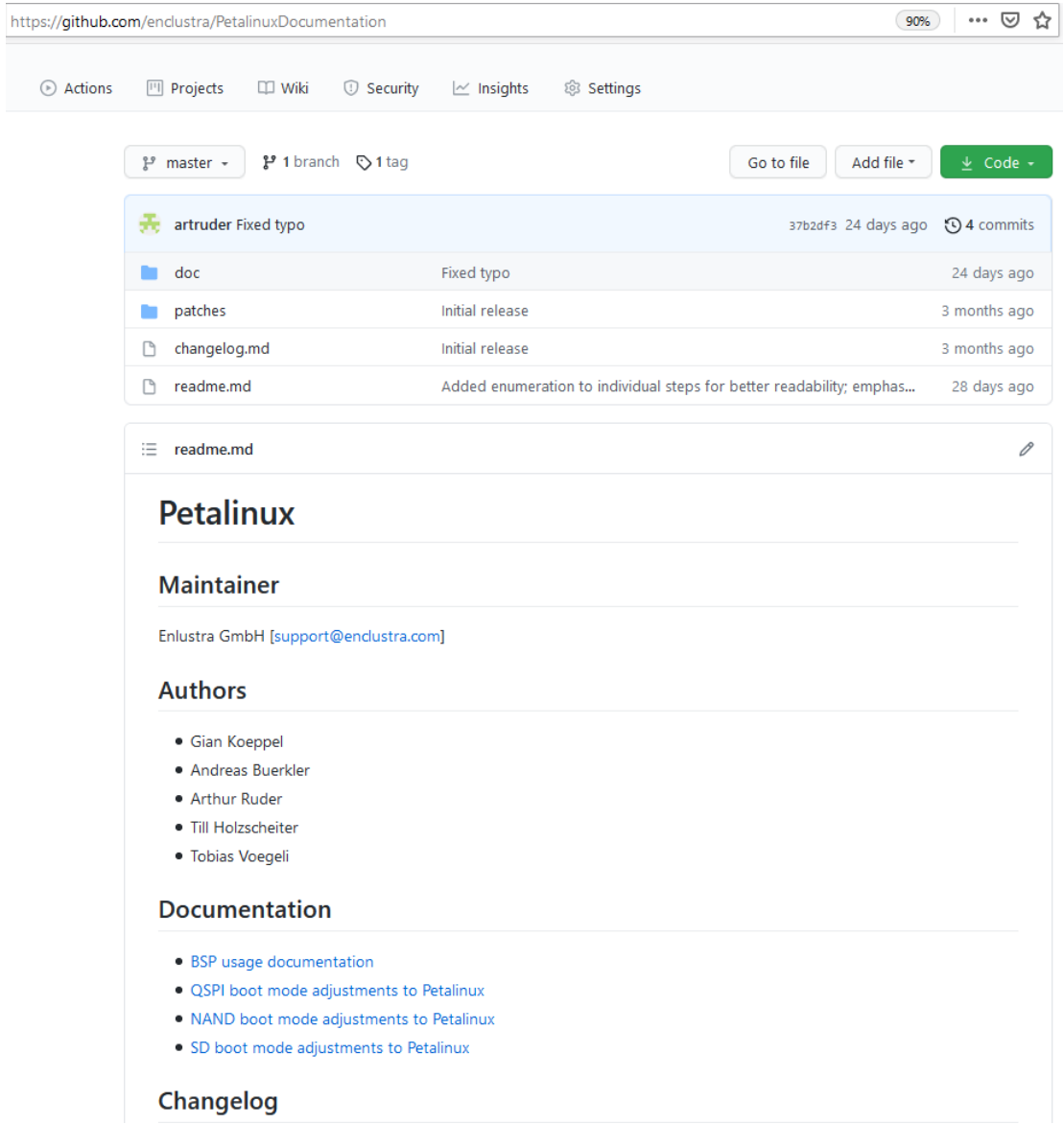
Product Deliverables – PetaLinux BSP Documentation



https://github.com/enclustra/PetalinuxDocumentation 90%

Actions Projects Wiki Security Insights Settings

master 1 branch 1 tag Go to file Add file Code

artruder Fixed typo 37b2df3 24 days ago 4 commits

doc	Fixed typo	24 days ago
patches	Initial release	3 months ago
changelog.md	Initial release	3 months ago
readme.md	Added enumeration to individual steps for better readability; emphas...	28 days ago

readme.md

Petalinux

Maintainer

Enlustra GmbH [support@enclustra.com]

Authors

- Gian Koeppel
- Andreas Buerkler
- Arthur Ruder
- Till Holzscheiter
- Tobias Voegeli

Documentation

- BSP usage documentation
- QSPI boot mode adjustments to Petalinux
- NAND boot mode adjustments to Petalinux
- SD boot mode adjustments to Petalinux

Changelog

BSP usage documentation

- BSP usage documentation
  - Prerequisites
  - Petalinux project creation and build with BSP file
  - Updating the hardware file (.xsa) used by the Petalinux project
  - Accelerating Petalinux builds
  - Changes to Petalinux default configurations
    - Kernel changes
    - U-boot changes
    - Device tree changes
    - Root file system changes
  - CPU frequency

Prerequisites

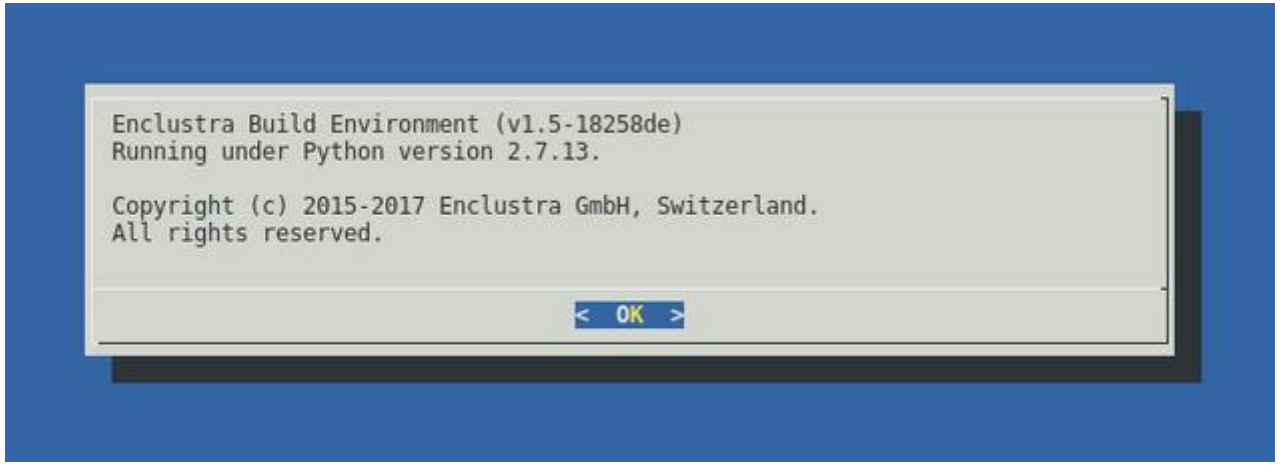
- Supported Linux OS for Petalinux 2020.1
- Petalinux 2020.1 installation and all required packages (for more details please refer to Xilinx UG 1144)

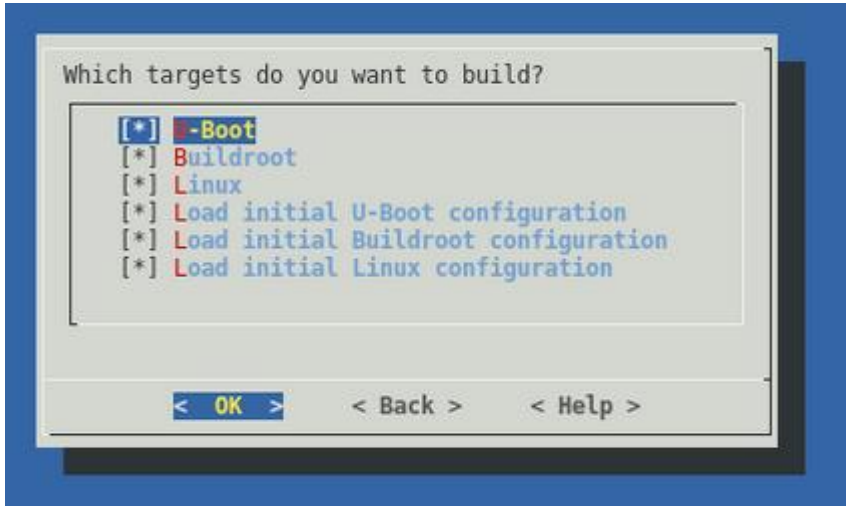
Petalinux project creation and build with BSP file

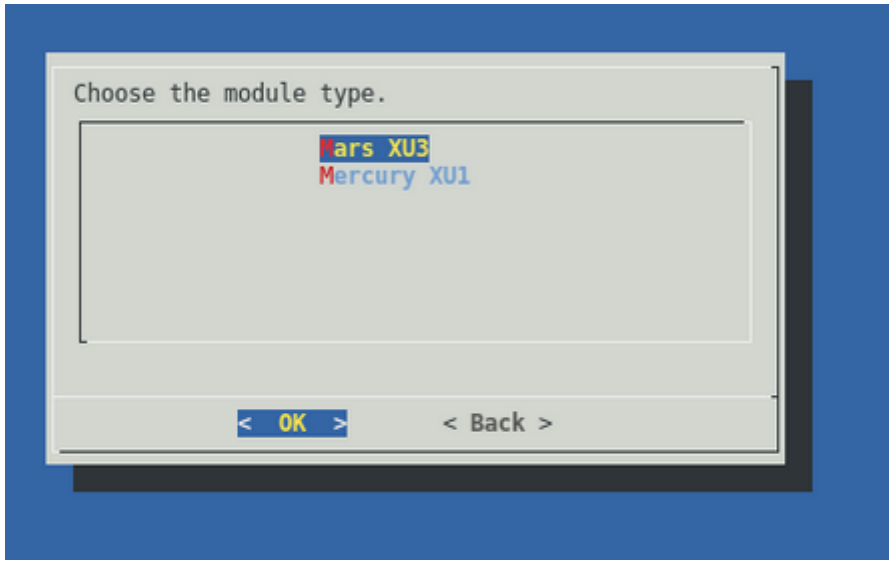
The provided BSP file follows the naming convention of `Petalinux_${MODULE_NAME}_${BASEBOARD_NAME}_${BOOT_MODE}.bsp` (The BSPs themselves are located in the release page of each respective reference design, e.g. Mercury XU5 PE1 release 2020.1_v1.1.0). Using the Mercury ME-XU5-2EG-1I-D11E as an example in combination with the PE1 baseboard and SD card boot mode the file will have the name: `Petalinux_ME-XU5-2EG-1I-D11E_PE1_SD.bsp`

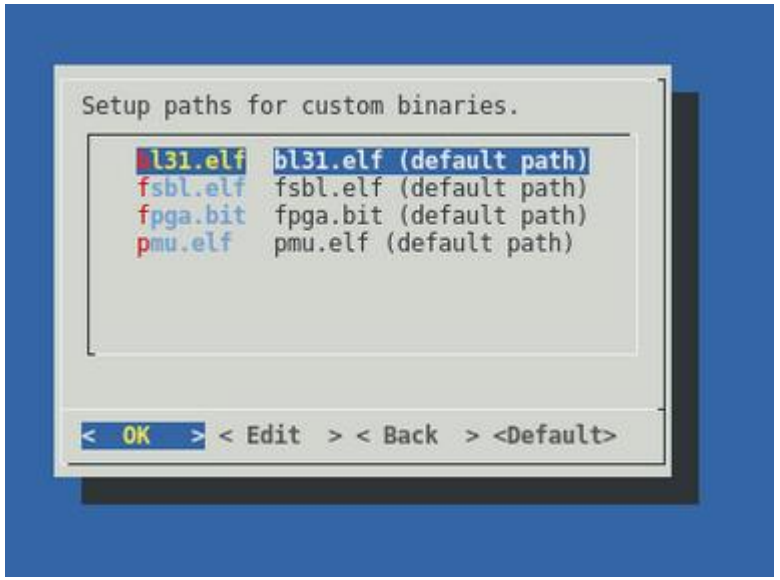
1. Open a console and source the Petalinux environment script: `source /<path-to-petalinux-installation-dir>/settings.sh`
2. To create a Petalinux project from the provided bsp file use: `petalinux-create --type project -s <path-to-bsp-file>.bsp`
3. The created project has the following structure:

Product Deliverables – Enclustra Build Environment (EBE)









Product Deliverables – EBE Application Note

https://github.com/enclustra/EBEAppNote/blob/master/EBEApplicationNote.md

56 lines (48 sloc) | 4.62 KB

Table of contents

4.8 - Debug a custom application

4.8.1 - Start a debug session in Xilinx SDK

Xilinx provides a System Debugger (TCF) which needs a software (tcf-agent) running on the target Linux. This software is built by default when a Linux build is generated in the Enclustra build environment with default configuration. The needed setting can be found in the Buildroot configuration menu in the `Target packages -> Debugging, profiling and benchmark` submenu.

Prepare Target Linux

- Create a Linux build as described in section 4.7.2
- Connect the Enclustra module via Ethernet to the host machine
- Boot Linux on the module
- Configure an IP address. For example:

```
ifconfig eth0 192.168.1.10
```

- Start Xilinx TCF agent:

```
tcf-agent &
```

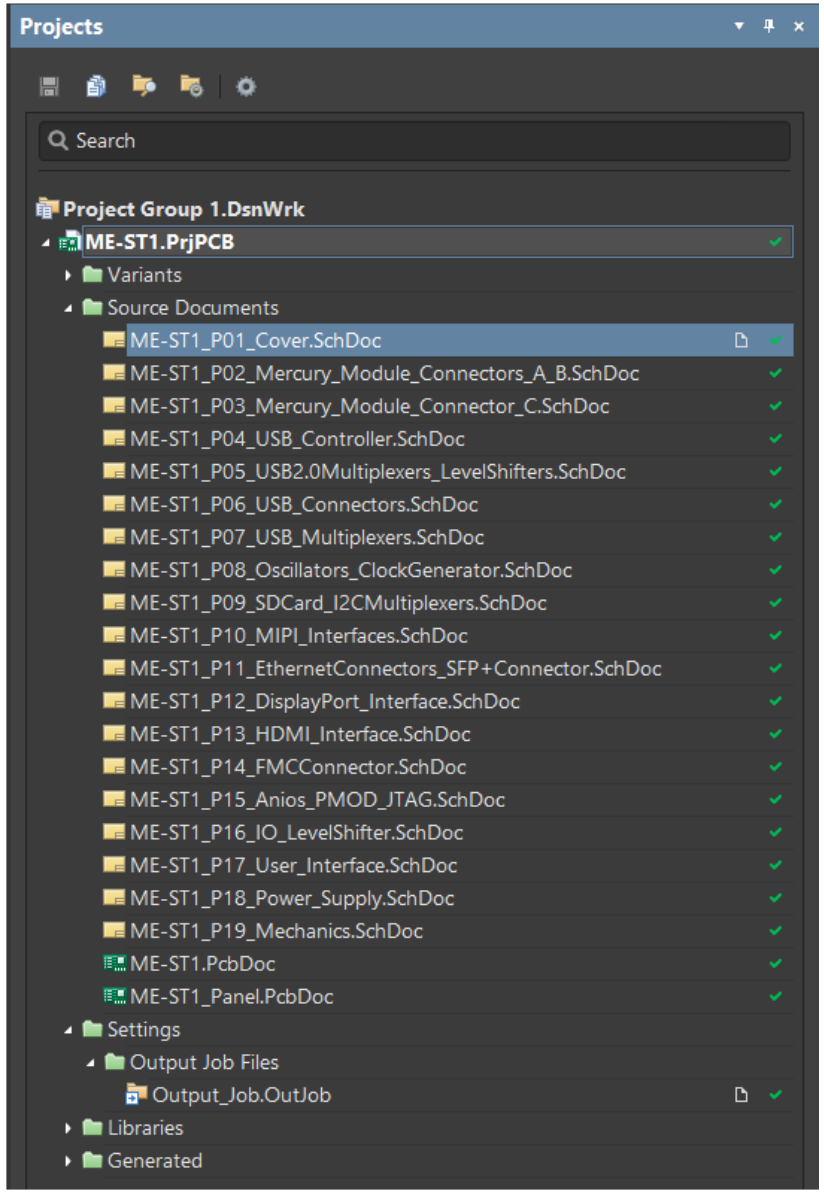
Create Application and Start Debugging

- Open Xilinx SDK
- Create a Linux application as described in section 4.7.2
- Open `Run -> Debug Configurations`
- Click `Xilinx C/C++ application (System Debugger)` to create a new configuration
- Select the `Target Setup` tab
- From the drop down list `Debug Type` select `Linux Application Debug`
- Click `New` to create a new connection
- Enter the IP address of the target module to the `Host` field and set a name for the target. Set the Port to `1534`.
- Click `Test connection` to check if SDK is able to connect to the tcf-agent application running on the target Linux
- Click `Ok` and select the `Application` tab
- Set the project to debug and optionally the working directory (the path to download the application to the target file system)
- Click `Apply`
- Start debugging by pressing `Debug`

4.8.2 - Start a debug session in Intel ARM DS-5

The following example provides instructions on how to start a debugging session in ARM DS-5 using GDB debugger.

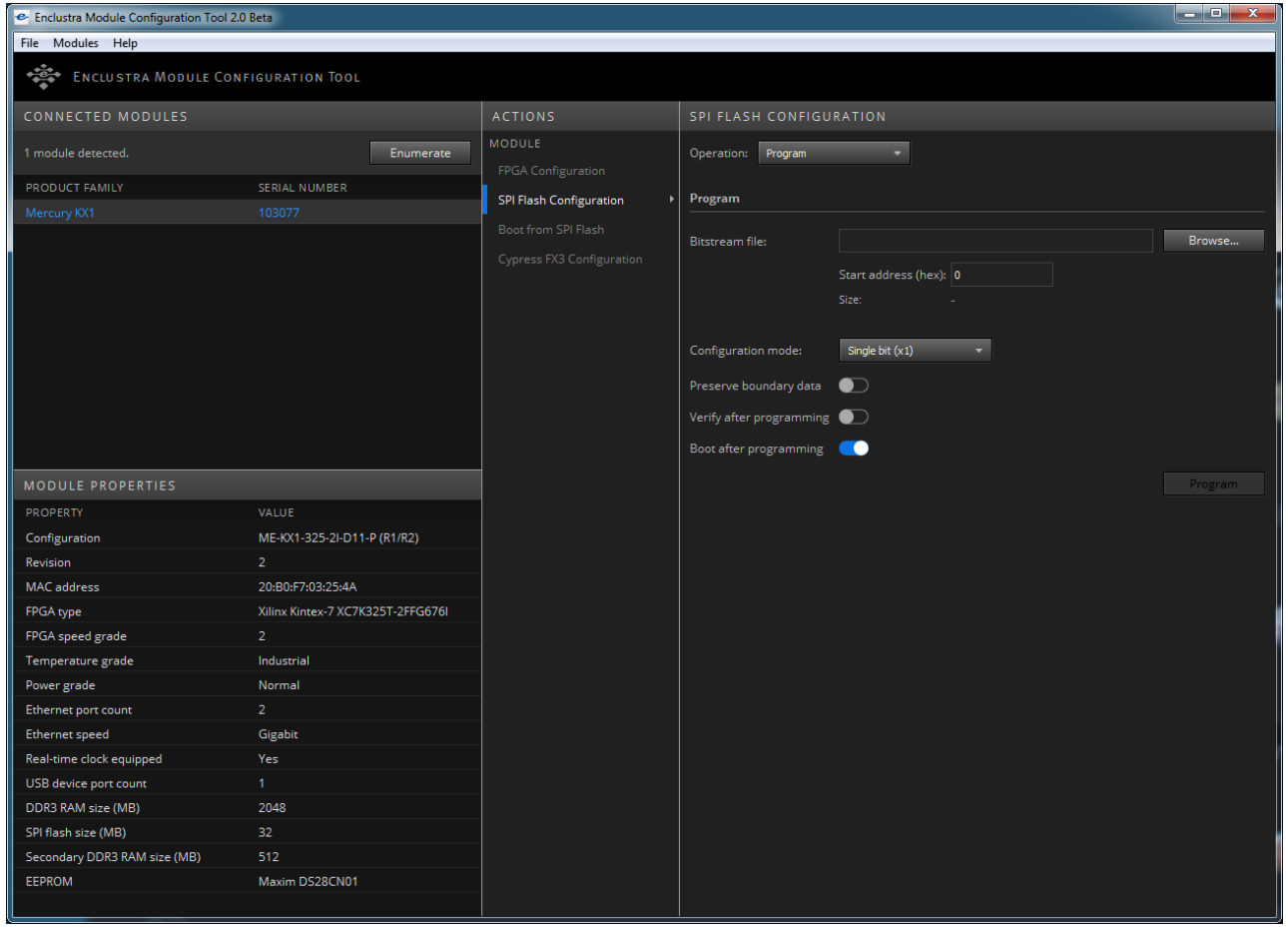
Product Deliverables – Design Files



- For Mercury+ ST1 and Mars ST3 base boards, the Altium design files are available on request by signing a license agreement
- Perfect starting point for a custom baseboard for Enclustra SOM

Filename Extension	Description
*.OutJob	Altium Output Job File
*.PcbDoc	Altium PCB Document
*.PrjPCB	Altium PCB Project
*.PvLib	Altium Pad Via Library
*.SchDoc	Altium Schematic Document
*.pdf	Design Files Release Notes
*.xlsx	BOM Template

Product Deliverables – Module Configuration Tool (MCT)



- Configure Enclustra SOM and base boards via USB without additional hardware
  - Program FPGA
  - Program SPI flash
  - Read EEPROM configuration
  - Configure peripheral devices

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- Custom base board schematics and PCB reviews
- Design-in support
- Custom modules
  - New product models (special assembly variant)
  - New products (SOM co-design)

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