2nd SoC workshop CERN - Minutes – June 7, 2021 - Vendors

https://indico.cern.ch/event/996093

Notes:

- These minutes were collected by S. Haas.
- They provide a record of the questions and answers following the presentations. For the presentations themselves including recordings, please, refer to the indico timetable.

Monday – June, 7th:

- G. Donzel (Avnet Silica), Xilinx:
  - Q: What about FPGA/SoC power utilization?
    A: Power is critical and a challenge for customers. Although semiconductor process evolution from 28 nm to 16 nm and 7 nm reduces dynamic power for a similar design, customers typically want to implement more features. Xilinx has several tools available (Xilinx.com/power): the XPE spreadsheet can provide an early quick estimate of the power requirements, given that interface requirements are usually known (I/O, transceiver number and speed), logic utilization can be estimated. Vivado power analysis gives more accurate results, but requires the FPGA design to be available. Avnet FAEs are available to help, also with the design of the power supply circuitry. They are working closely with Renesas and others.
  - Q: What about the fusion between AMD and Xilinx? What effect will this have on Xilinx SoCs?
    A: From Avnet's perspective it is "business as usual", they do not expect any major issues from the merger. The target markets are different: where AMD targets computers and servers, Xilinx core markets are industrial, scientific, audio/video and aerospace/defense. The data center is a new market for Xilinx, this is a "big cake" and Xilinx managed to get a share, for instance with the Alveo accelerator cards. Xilinx and AMD are two separate teams, although some interesting synergies can be expected in the future.
- S. K. Ramegowda (Intel Corp.), Intel/Altera:
  - No questions
- G. Donzel (Avnet/Silica), Microchip:
  - Q: Product obsolescence, how long will Polarfire, for instance, be available?
  - A: This is a concern that Microsemi addresses, the expected availability for Polarfire devices is 2041. This is detailed in a longevity letter from Microsemi. Longevity was one of the reasons to use RISC-V (the other main one being independent from ARM IPs).
- M. Rohrmüller (Trenz Electronic GmbH), Trenz:
  - No questions
- D. Ungureanu (Enclustra GmbH), Enclustra:
  - Q: What about the long lead times?
    A: This is unfortunately common in the current semiconductor supply situation.

    - Q: What is the typical delay?
      A: Need to contact sales with the specific product. Could be driven by the FPGA/SoC, lead times of 1 year not uncommon.
- Open Session:
    - Q (to Trenz): Do you supply CPLD sources to customers when developing custom carrier boards?
      A: Yes, this is possible. In-house programming with modified firmware is also possible; however, it requires a minimum quantity. Trenz can also program custom clock generator configurations.
    - Q (to Avnet): What about lead times?
      A: We are currently in a very complex situation, which has not happened in the industry previously. Current lead times for FPGA/SoC are from 14 weeks (if you are lucky) up to 52-53 weeks. DDR3 memories from Micron are on allocation, so Avnet cannot even give a delay. This is similar for EMMV and QSPI devices. The recommendation is to place the order as soon as possible to be in the queue.
    - Q (to Trenz): What about lead times?
      A: Waiting times could be over one year due to the semiconductor supply situation. The customers can also supply the SoC devices (in case they managed to get hold of them) to Trenz for assembly in order to speed things up; however, the parts have to come from an official Xilinx distributor.