2nd SoC workshop CERN - Minutes – June 9, 2021 – Projects2

https://indico.cern.ch/event/996093

Notes:

- These minutes were collected by F. Meijers.
- They provide a record of the questions and answers following the presentations. For the presentations themselves including recordings, please, refer to the indico timetable.

Wednesday – June, 9th:

- A. Tanaka, A System-on-Chip-based Front-end Electronics Control System for the Phase-2 ATLAS Thin-Gap Chambers (TGC):
    - Q: Referring to slide 13/20, where is the VME master located?
      A: The VME master is in the same crate (see slide 8/20). It has no embedded CPU. However, it is possible to control the VME via the Sector Logic (see slide 5/20).
    - Q: Concerning the users software running on the JATHub (slide 5/20), mainly the XVC and SVF player; how do you build it?
      A: The source code of XVC is taken from Xilinx examples and the SVF source code is downloaded from their web site. The executables are built as a project in PetaLinux.
- J. D. Hobbs, The ATLAS Smart Rear-Transition Module of the Liquid Argon Calorimeter:
    - Q: Do you see potential usage for the real-time processing unit on the Zynq, because it can be synchronized with the data flow and might be a potential place to put monitoring?
      A: No specific plans, but we have noted that. Had some discussion on synchronization from the RTM to the LAS.
    - Q: Which kind of signals are you routing from the main board to the RTM?
      A: There are several high-speed 10 and 25 Gbps links (see slide 4). Unfortunately, for the few links we see problems with, we do not know if it is the RTM layout or a problem with the FireFly module.
    - Q: You are talking about XUAI links. Are these the ones where you can do 10 Gbps over the backplane? Where do they go out at the end; do they go out of the crate?
      A: Correct. These go from the back plane to a switch in the hub slot, which does both GbE base channels as well as 10 GbE. Canonical example is a real-time scope used for diagnostics.
    - Q: You are raising the question for a common solution for HDL, operating system and user software. Do you have anything in mind for that?
      A: I would not be as ambitious as you implied. So far looking for a solution for each of the three. Looked at HOG for the HDL part. We know SDK is a temporary thing.
- H. Boukabache, J. Hast, Remote Management of SoC-based Radiation Monitors both at CERN and ESS:

    - Q: You are using influx-db. How scalable did you find it (In our experience it becomes quickly limited)?
      A: We have low data rates (1 measurement/s) and there it works quite well. For operation when loading a dataset of a few hours it is workable. If you want to browse datasets of a week, it becomes unusable. The best thing with this system is the web based user interface, which is more practical compared to using virtual desktops behind gateways.
    - Q: You told to have a kind of a recovery mode when booting the Zynq MPSoC. Primarily booting with SD card and then switching to QSPI Flash in case of failure. How are you detecting that it is not booting successfully?
      A: This is implemented with a heartbeat mechanism in hardware (see slide 13).
- D. Gastler, Updates on SoC for the Apollo Platform:
    - Q: You have a nice implementation of a chip-to-chip communication. Is there an easy understanding of the difference between chip-to-chip and DMA, or are they two sides of the same coin?
      A: chip-to-chip is how you extend an AXI bus from one chip to another chip, so we are talking about from a Zynq FPGA to a US+ FPGA. One can use signals or MGT. DMA is how over that AXIbus you send data. We do not use DMA currently; no need yet.
- L. Ardila, ZynqMP-based Board Management Mezzanines for the Serenity ATCA Blades:
    - Q: I find the split boot very interesting and noted you have succeeded with the PS configuration. Which kind of problems have you encountered, in particular the PS register files? Is the source available ?
      A: Biggest challenge was the different exception levels that are needed (see slide 17). We are working in this project to have it in a state that it can be published soon.
    - Q: In the workflow for the minimum configuration, there is PetaLinux and Vitis (see slide 15). Can't you do everything in Petalinux?
      A: The reason for Vitis is that OpenIPMC was built with Vitis. You could do everything in Petalinux.
- N. Karcher, Development Infrastructure for MPSoc/RFSoC Platforms:
    - Q: On slide 11, the plugins are statically built in the firmware or are they dynamically loaded? In the latter case, have you considered partial configurations loading the corresponding IP-core?
      A: Actually, the plugin part is loaded dynamically, but the configuration is fixed. The service hub will find the device tree and then load the plugins, likewise kernel modules for the Linux kernel, but there is no re-configuration happening. It should be possible with device tree overlays.
- J. Tikalsky, APx Embedded Linux Developments:
    - Q: On slide 14, you said the device numeration is not consistent, and there is a hierarchical representation of the I2C bus where also the device tree is represented. You have the opportunity to use the latter.
      A: Yes, that is what we do.

    - Q: Is there a different way to map the GPIO to the device tree?
      A: There are few interfaces available; they all have the issue of how to identify the GPIO I/O pins. We do not have an implementation for that, do not want to edit the device tree and could get out of sync.
    - Q: On slide 13, you mention to not use geographical addressing for the IPMC. What would it take to implement that?
      A: That would require modifications to the IP stack. Not considered so far. Would welcome a patch to support client-ID.
- R. Spiwoks, Software Framework for the System-on-Chip of the ATLAS MUCTPI:
    - Q: Looking further in time, there might be others then ARM, like RISK-V pushed by Micron.
      A: Atlas and CMS are governed by the Phase-2 timescale and developments are done now, all using Xilinx MPSoC. You are right for the longer timescale, there might come others.
- P. Zejdl, CMS DAQ System Software Design Considerations for Zynq-based MPSoCs in ATCA Crates:
    - Q: Comment that SIPL stands for serial interface protocol light, invented by Pigeon point for the IPMC. It is fully IPMI based.
    - Q: Can we have a repository for common items, which are not necessarily linked to the Atlas or CMS specific way of building?