## RAS Working Group meeting 25.03.2021

**Participants:** A. Apollonio, E. van der Bij, T. Cartier-Michaud, J.D.G. Cobas, G. Daniluk, S. Georgakakis, L. Felsberger, B. Fernandez Adiego, C. Gentsos, L. Patnaik, P. Perronard, M. Saccani, V. Schramm, M.R. Shukla J. Serrano, J. Uythoven (chair), P. Van Trappen, W. Vigano, C. Zamantzas

The slides are available on Indico:

https://indico.cern.ch/event/997719/

## Designing, Validating and Demonstrating High Reliability for the DI/OT Hardware Kit - Speaker: Volker Schramm

V. Schramm presented an update on the DI/OT (Distributed I/O Tier) reliability activities with a focus on the system design and validation phases. The DI/OT will be used for a variety of applications within and outside CERN. Hence its reliability will be critical. A Fault Tree Analysis is ongoing for the Powering Interlock Controller (PIC), which is expected to be the most critical application. A bottom-up module analysis in Isograph is ongoing.

Slide 16: P. Van Trappen asked where the derating factors of the capacitors were taken from and if they are the same across capacitor technologies. V. Schramm answered that the factors were taken from the book "Reliability Engineering: Theory and Practice" Alessandro Birolini and that the factors are capacitor technology dependent.

W. Viganò suggested to use even more conservative factors. For ICs with a rated temperature of 105 °C he attempts to avoid temperature increases due to internal dissipation exceeding 30 °C on top of an assumed ambient temperature of 40 °C. For capacitors for applications of 5 V he uses capacitors rated for 50 V. The added stress due to radiation leads to such large derating factors.

V. Schramm answered that the stated derating factors should be seen as limits and that in most cases the components are derated further.

Slide 18: V. Schramm explained that two transistors were close to their margin or above, which triggered a detailed FMECA.

Slide 22: V. Schramm added that Ansys Sherlock is used to assess the effect of mechanical failure mechanisms caused by mechanical stresses, but also temperature cycles. Here it is to be assessed if it can be used to simulate the long-term reliability of soldering and provide design guidelines for optimisation.

Slide 28: V. Schramm said that the components are divided in two component classes: The first one is properly derated electronics operating at low stress without expected lifetime limitations. The second class consists of power electronics with wear out expected within the required 20 years of lifetime.

Slide 29: W. Viganò commented that radiation should be added as factor for determining the lifetime.

Slide 31: J. Uythoven added that the requirement for end-of-life testing and preventive maintenance depends on the types of failure modes encountered. If the systems fail in a safe manner and redundancy is maintained, then it is acceptable to have failures. However, blind failures are problematic.

W. Viganò added that radiation has to be accounted for when performing end of life testing. Power electronics damaged by radiation may continue to work, but at a lower efficiency which causes increased heat emission and this results in significant lifetime reductions of the damaged system as well as surrounding systems.

G. Daniluk commented that such additional effects are in principle considered in the foreseen testing strategy. Furthermore, the radiation dose is logged.

L. Patnaik commented (in the chat) that the extra heating is in the order of < 5 % (at full load) from radiation testing and has been taken into consideration in the thermal design of Radiation Tolerant Power Supply RaToPUS.

W. Vigano asked L. Patniak what the total dose target was.

L. Patnaik replied: Target 500 Gy. AC/DC stage already reached this target. DC/DC stage has currently reached 375 Gy, failure modes at 375 Gy are investigated.

S. Georgakakis asked if similar studies are done for the non-radiation-tolerant PSUs and when conclusions will be available. V. Schramm answered that it is being worked on. A list of potential PSUs exists and testing will be performed. G. Daniluk added that conclusions should be available by 2022 as this is when they will be bought.

W. Viganò commented that given the wide range of applications of the DI/OT it is important to issue constraints for the validity of the reliability findings depending on the system usage. Future users of the DI/OT should be asked to perform validation and acceptance tests for their use-cases.

Slide 32: E. van der Bij asked V. Schramm to elaborate on his experience on the burnin experience with the VFC-HD. V. Schramm explained that two percent of the systems could be screened and that a decreasing failure rate could be observed over time. The identified failures were related to production problems except one single component failure.

Slide 34: E. van der Bij asked whether the analysis of operational data could be performed for existing systems as a dry run to see what information is coming back from maintenance. V. Schramm answered that this is already being discussed with Ioan Kozsar and Eve Fortescue-Beck using InforEAM, but that the currently available data for existing systems are not sufficient. For the DI/OT operation it is planned to log the required operational parameters, including application and environmental parameters.

After the presentation, S. Georgakakis explained that for his use case 30 DI/OT units will be produced ahead of the BE-CEM schedule. He pointed out that it would be good to regularly exchange on the intended testing plan so that their DI/OT testing is in line with BE/CEM.

B. Fernandez commented that the presented methodology focuses on hardware and asked whether a methodology exists for ensuring the reliability of the firmware and software. G. Daniluk answered that such a methodology is being developed and that a Continuous Integration infrastructure exists, which will be expanded in collaboration with S. Uznanski from SY-EPC-CCE.