CERN

Designing, Validating and Demonstrating High Reliability for the DI/OT Hardware Kit

RASWG Meeting 25/03/2021

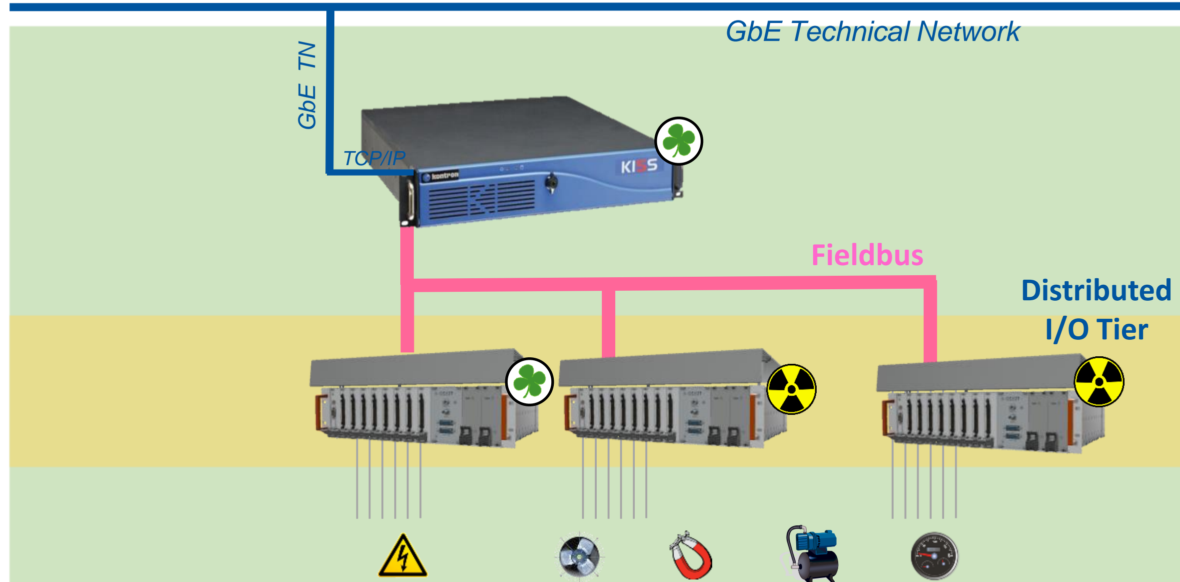
V. Schramm on behalf of and with many inputs from the DI/OT team:

G. Daniluk, C. Gentsos, E. Gousiou, L. Patnaik, A. Patsouli, M. Rizzi, J. Serrano

Agenda

- The Distributed I/O Tier Hardware Kit
- DI/OT Dependability Methodology
- Ongoing and Future Efforts
- Summary & Outlook

DI/OT - Front End Hardware Tier



- Newly supported tier
- Extension of CO services
- For rad-exposed applications

G. Daniluk & E. Gousiou, BE-CO TM 04.06.20

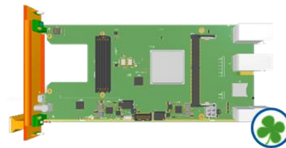
The DI/OT Platform

Courtesy of G. Daniluk

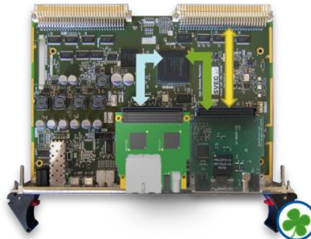
- Modular
- Low-cost
- Standards-compliant
- Reliable
- High-performance
- Open hardware

platform for custom electronics

Non-rad Peripheral Board



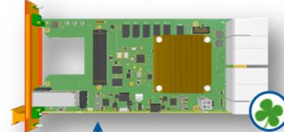
ProFIP



COTS PSU

RaToPUS

Non-rad System Board

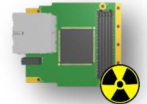


Rad-tol System Board

White Rabbit

Profinet

WorldFIP



Powerlink

DI/OT Platform (2)

Courtesy of G. Daniluk

3U Crate

19'' rack variant

Backplane

Redundant PSUs

System Board

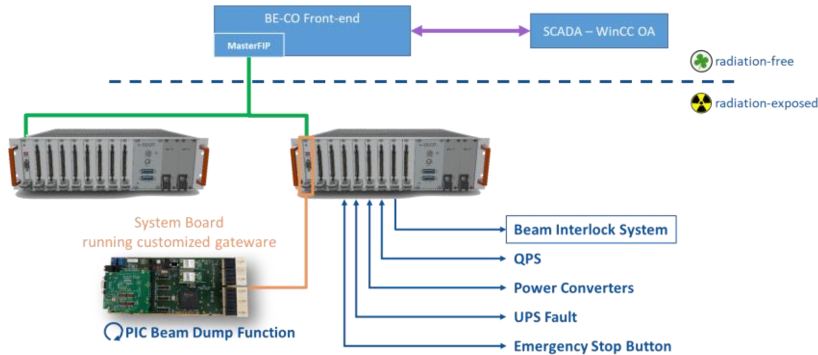
Peripheral Boards
- Application-specific

Front Panel
- Power Cycle Request BNC
- Fan Tray Connector

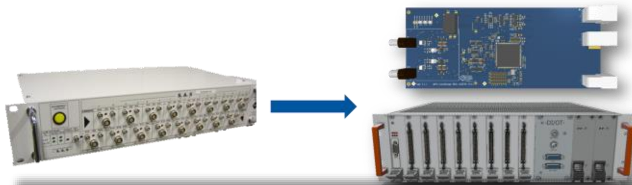
DI/OT Applications

G. Daniluk & E. Gousiou,
BE-CO TM 04.06.20

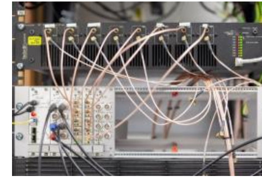
1) Powering Interlock Controller *TE-MPE*

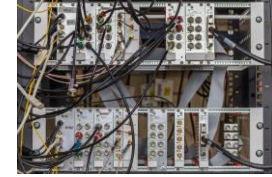


2) Full Remote Alignment System *EN-SMM*



3) Quantum Computing *Creotech Instr. S.A., PL*

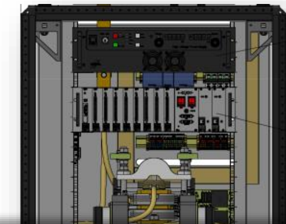


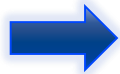


4) Fast Interlocks *TE-ABT*

5) Coupling Loss Induced Quench System (CLIQ)

TE-MPE





- How will the DI/OT perform?
- How to ensure high performance for different applications in varying environments?
- How to ensure a successful: Design? Testing? Production? Installation? Operation?

DI/OT in a nutshell

- Operation in various HL-LHC systems, including critical systems
  - ➢ Customisable to fulfill a variety of requirements
- Dependable operation required (functionality; low failure rate; high availability; long lifetime; efficient maintenance; good support; user-friendly; ...)

Existing dependability efforts (design specs):

\+ PSU redundancy

\+ Design according to standards

\+ Monitoring capabilities

\+ Rad-tol design & irradiation tests

± **1 DI/OT - several applications**

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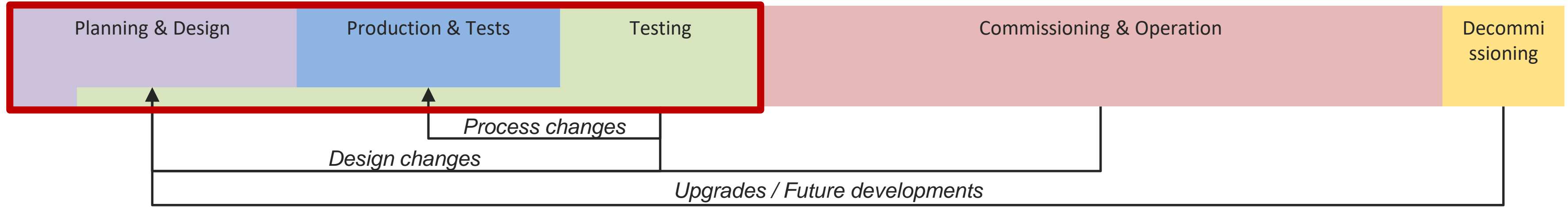
The DI/OT Lifecycle



Dependability goals

Quality Assurance

Remaining lifetime?

Operational validation

Screening, reliability demonstration

Dependability analyses and assessment

Refurbishment?

Dependability monitoring & analysis

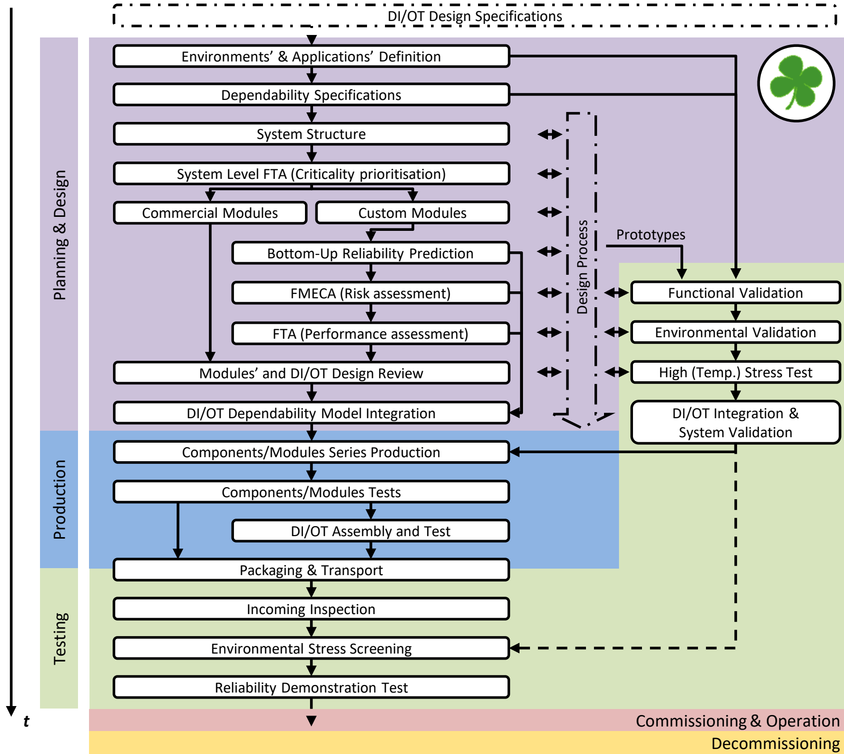
Reviews, Audits

Operational support & maintenance

Dependability validation

Dependability management

DI/OT Dependability

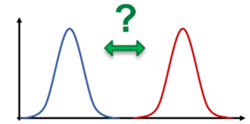


Planning phase:

- Specifications
  - Design, Environment, Application, Dependability

Design phase:

- Analysis methods (qualitative/quantitative)
- Design reviews
- System dependability model & prediction
- FEA simulations
- Prototype testing and validation

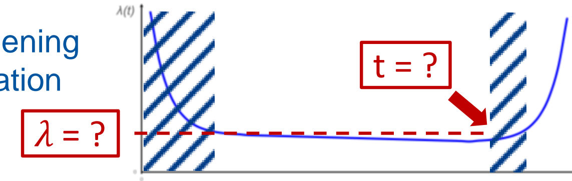


Production phase:

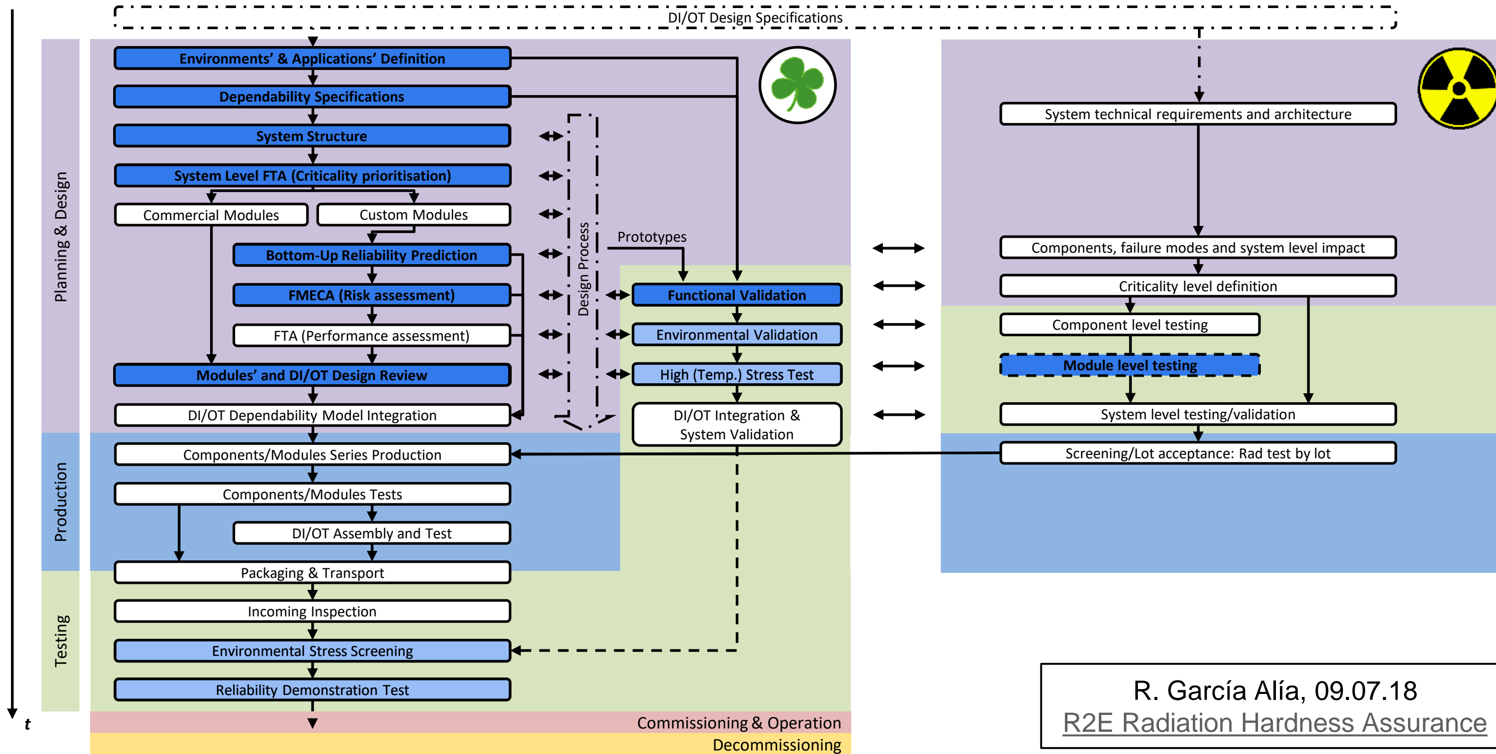
- Process control and Quality Assurance
- Production Test Suite (PTS)
- Packaging and Transport

Testing phase:

- Early life failure screening
- Reliability demonstration



DI/OT Dependability



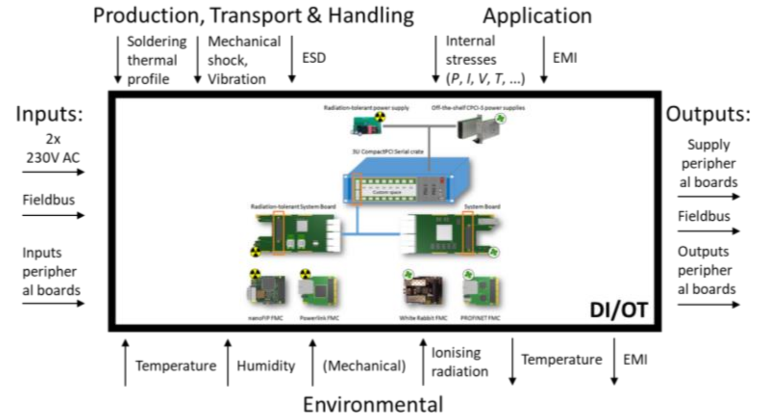
Radiation Hardness Assurance (RHA)

R. García Alía, 09.07.18
R2E Radiation Hardness Assurance

Specifications

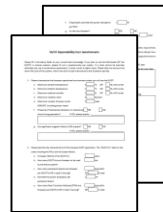
Defining specifications – Black Box Approach:

- Design specifications as input
- Definition of I/Os
- Life cycle environments



Dependability specifications (→ methodology):

1) General requirements
2) Design & Validation
3) Production
4) Handling, Packaging & Transport
5) Testing after production
6) Installation & Operation



User questionnaires

Input for:

- Dependability model
- Life cycle & performance simulation
- Validation tests definition

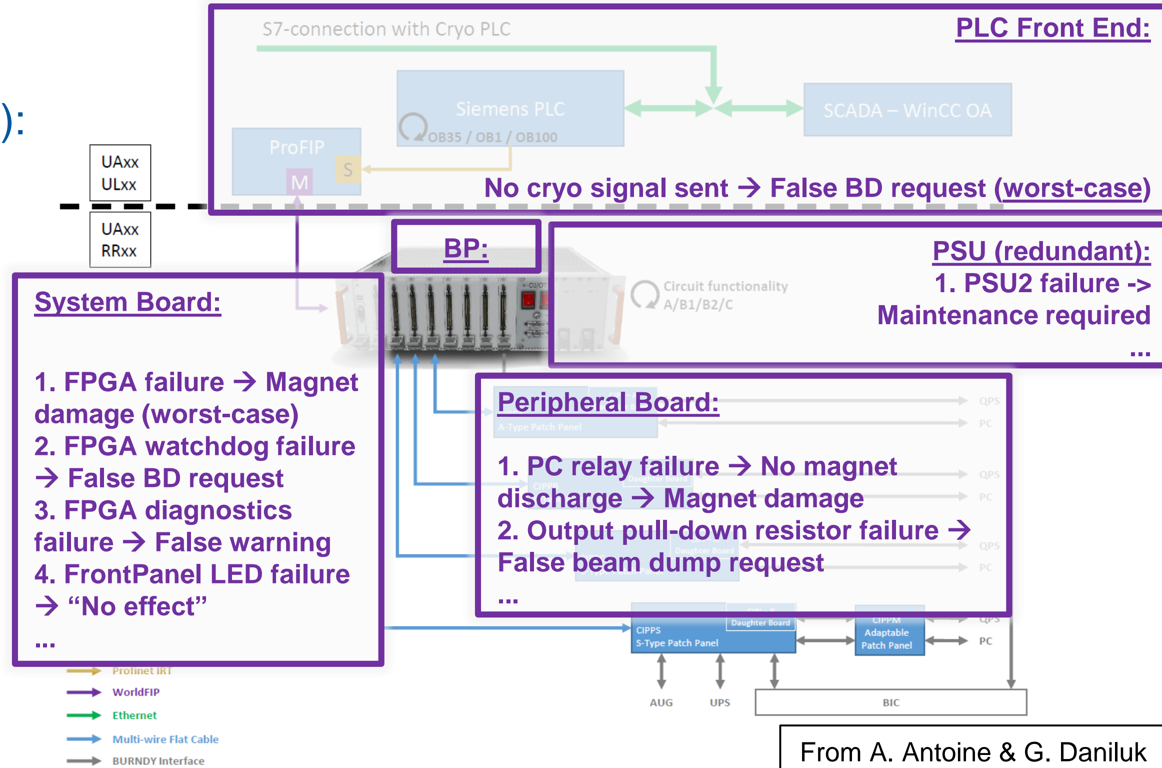
DI/OT for PIC - FTA

Ongoing & non-comprehensive !

Top-level end effects (Severity ranks):

6) A) Magnet damage (missing to switch off PC)
   B) Magnet damage (missing to trigger magnet energy extraction)
   C) Magnet damage (missing to trigger beam dump request)
5) False beam dump request
4) Maintenance required - after LHC fill
3) Maintenance required - to be scheduled
2) False warning generation
1) "No effect"

➢ Assign to functional blocks (Worst-Case approach)



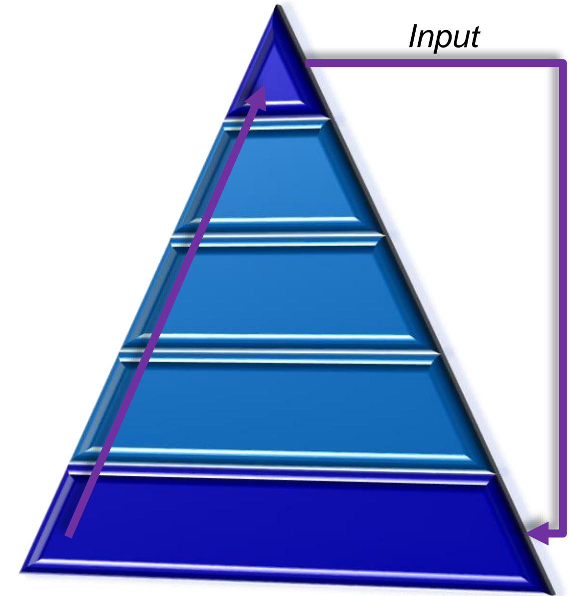
From A. Antoine & G. Daniluk

Presented during: BE-CO Technical Meeting, 08.10.20

Top-Level DI/OT Analysis

Ongoing

1) Top-level failure effects analysis (↔ FTA)
   - Definition of 8 generic DI/OT top level failure effects:
     8) False/erroneous fieldbus communication
     7) False/erroneous peripheral board communication
     6) Loss of peripheral board communication
     5) Loss of fieldbus communication
     4) "Degraded" operation - immediate maintenance required
     3) "Degraded" operation - scheduled maintenance required
     2) False warning generation
     1) "No effect"
   - Assign failure modes and effects to 14 top-level modules
2) Perform FMECA for individual modules bottom-up
   - Module top-level failure effects as input



Bottom-Up Module Analyses

Ongoing

1) System structure & reliability prediction:
- Radtol System Board -

1.1.1.1:RadTol System Board:FR=1E+03
1.1.1.1.1:Power:FR=388
1.1.1.1.1.1:Always-on P3V3 power:FR=25.2
1.1.1.1.1.1.1:Capacitor 100uF:FR=10.5
1.1.1.1.1.1.2:Capacitor 10uF:FR=0.776
1.1.1.1.1.1.3:Capacitor 10nF:FR=1.32
1.1.1.1.1.1.4:Linear Regulator IC5:FR=0.
1.1.1.1.1.1.5:Resistor 10k:FR=0.652
1.1.1.1.1.1.6:Resistor 4k7:FR=0.652
1.1.1.1.1.1.7:Resistor 1k:FR=0.652
1.1.1.1.1.1.8:Capacitor 10nF:FR=0.543
1.1.1.1.1.1.9:Capacitor 10uF (0.52 ra
1.1.1.1.1.2:12V0 power cleanup:FR=27.6
1.1.1.1.1.2.1:Capacitors 100uF (0.6 ra
1.1.1.1.1.2.2:Conductor L1:FR=0.436
1.1.1.1.1.2.3:Fuse F1:FR=0.59
1.1.1.1.1.2.4:Capacitor 100nF Ratin
1.1.1.1.1.2.5:Resistor 2k:FR=2.46
1.1.1.1.1.2.6:Resistor 0R05:FR=0.964
1.1.1.1.1.2.7:LED LD1:FR=0.14
1.1.1.1.1.2.8:Header J8:FR=2.01
1.1.1.1.1.3:P1V2 power:FR=5.45
1.1.1.1.1.3.1:Connector J9:FR=2.01
1.1.1.1.1.3.2:CERN Radtol 10W DCDC
1.1.1.1.1.3.3:Resistor 4k7:FR=0.922

Block Properties - 1.1.1.1.1.1.1 : Capacitor 100uF 217 Plus Capacitor

General | Parameters | Rate/Pi Factors | Tasks | Notes | Hyperlink

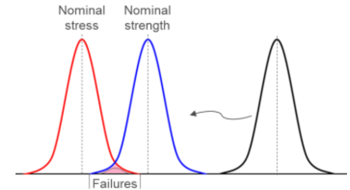
Quantity:	1
Adjustment Factor:	1
Year of Manufacture:	2020
Duty Cycle:	0.99
Cycling Rate:	365
Ambient Temp, Operating:	25
Ambient Temp, Non-Op.:	25
Capacitor Type:	Ceramic
Capacitance (Micro F):	100
Elec Stress Calc Mode:	Calculated
Voltage Stress Ratio:	0.5
Operating Voltage (V):	5
Rated Voltage (V):	10
Ambient-Case Temp Rise:	10

Stress= | Temp= | OK

Isograph Reliability Workbench

2) Bottom-up FMECA in blocks (Isograph)

Stress derating of components:



$$Stress\ ratio = \frac{Applied\ Stress}{Rated\ Stress}$$

Capacitors (MLCC):

name	derating	voltage	rating	pin1	pin2	tc
C34	0.793651	5	6.3	GND	P5V0_A	X5R
C35	0.793651	5	6.3	GND	P5V0_A	X5R
C193	0.75	12	16	GND	P12V0	X5R
C213	0.75	12	16	GND	P12V0	X7R
C194	0.52381	3.3	6.3	GND	P3V3	X5R
C116	0.52381	3.3	6.3	GND	PPERIPH	X5R
...						
C20	0.48	12	25	GND		
...						
C57	0.075	1.2	16	GND		

$$\frac{V_{applied}}{V_{rated}} \leq 0.5$$

C. Gentsos:
extract_cap_derating

ICs:

			Imax [A]	I_q [A]	Vdrop max [V]	P_Diss [W]	RJAmax [°C/W]	ΔTmax [°C]	Tjmax Datash. [°C]	Package
Linear Regulator IC5	TPS7A4901DGNT	IC5	2.00E-02		1.7	0.034	63.4	2.2	125	TSSOP8
CERN Radtol 10W DCDC	PCBM_CERN_FEASTMP_V	PCBM1			10.8	0		0.0		
Low Dropout Regulator	LT3083EQ#PBF	IC2	1.00E+00		0.8	0.8	16	12.8	125	5-Lead Plastic
Diode D1	1N4148WS	D1	2.00E-03		12	0.024	650	15.6	150	SOD-323
Zener Diode D2	BZX84B10V	D2	2.00E-03		12	0.024	420	10.1	150	SOT-23
Transistor T1	BC817-25	T1	1.00E-03		2.5	0.003	500	1.3	150	SOT-23-3
Transistor T2	BC817-25	T2	1.00E-03		2.5	0.003	500	1.3	150	SOT-23-3
Low Dropout Regulator IC3	LT3083EQ#PBF	IC3	1.00E+00		0.7	0.7	16	11.2	125	5-Lead Plastic
Linear Regulator IC4	TPS7A4901DRB	IC4		0.0165	8.2	0.135	47.7	6.5	125	VSON
Voltage Regulator IC29	TPS7A4533DCQ	IC29	1.50E-02		1.7	0.026	50.5	1.3	125	SOT-223
IGLOO2 FPGA	M2GL090T-FGG676I	IC1			3.3	0	14.52	0.0	100	676-BGA
N-channel MOSFETs with Diode T4-6,	MGSF1N02LT1G	T4-6, T23	1.00E-03		5	0.005	300	1.5	150	SOT-23
SPI Flash memory	AT25DN512C-SSHF-B	IC6			2.5	0		0.0	125	SOIC-8
Voltage Translators IC10,11,12,30	SN74LVC2T45DCTT	IC10...	1.00E-03		2.5	0.003	184	0.5	150	8-Pin SM8
N-channel MOSFETs with Diode T3	MGSF1N02LT1G	T3				0	300	0.0	150	SOT-23

$$\frac{T_{junction}}{T_{rated}} \leq 0.7$$

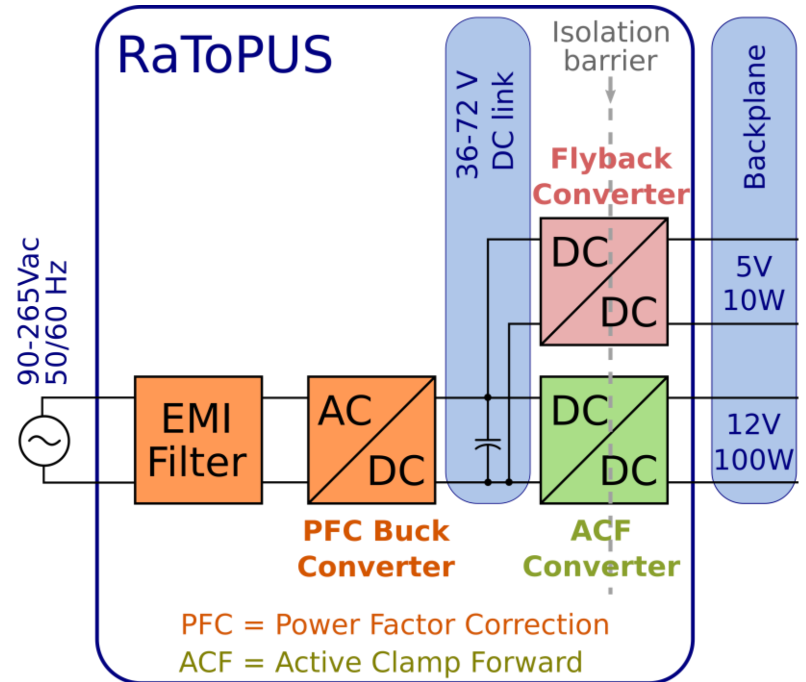
Radiation Tolerant Power Supply

RaTоPUS:

- Radiation tolerant PSU using COTS
  - AC/DC: 230Vac to 48Vdc
  - 12V DC/DC: 48Vdc to 12Vdc
  - 5V DC/DC: 48Vdc to 5Vdc

AC/DC demo board

12V DC/DC demo board



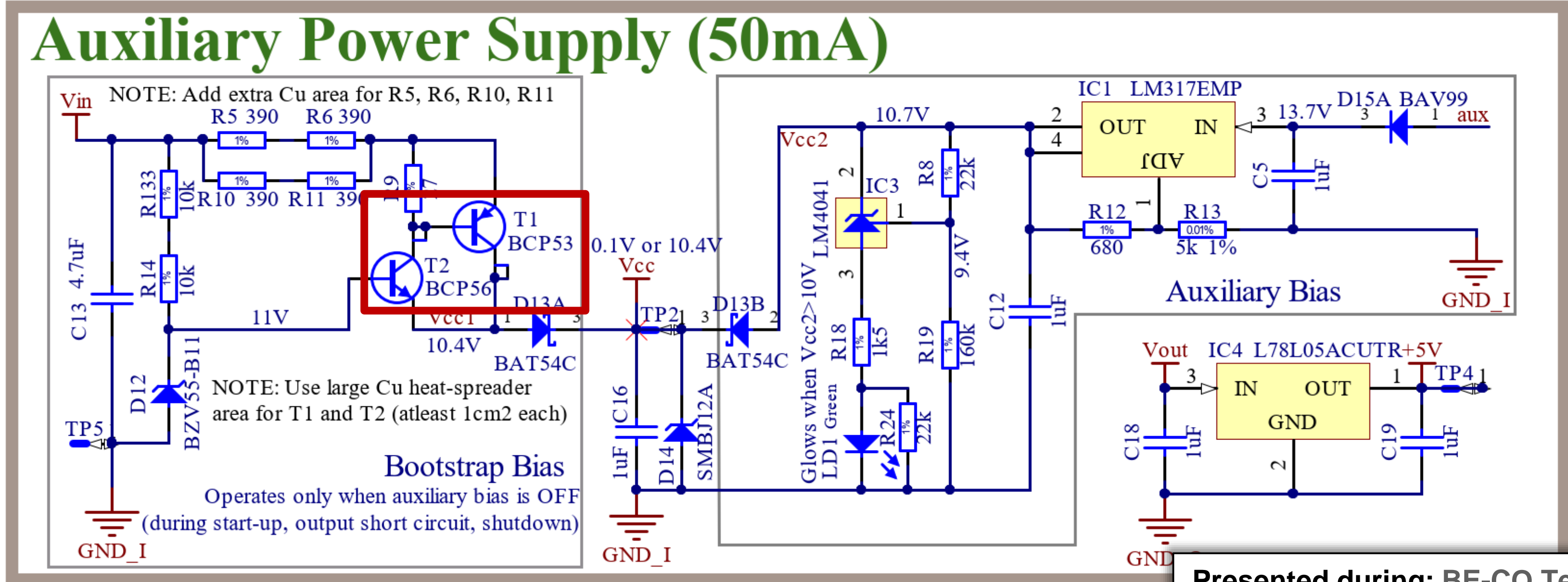
L. Patnaik, 25.06.20
R2E status of RaToPUS

RaToPUS - FMECA example

Ongoing design and analysis

12V DC/DC stage v1: Auxiliary Power Supply → Powering of control circuits

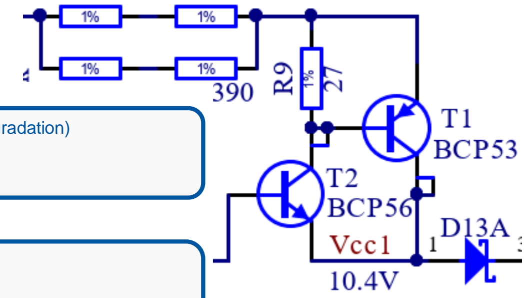
Work of L. Patnaik



Presented during: BE-CO Technical Meeting, 08.10.20

RaToPUS - FMECA (2)

Ongoing design and analysis



1. Schematic analysis

- If V_{in} = 72V (48V nominal) and V_{out} = 0V: $P_{diss,max}$ (T1), $P_{diss,max}$ (T2) ≥ 1W (conservative assessment for 50mA load current after 12 years radiation degradation)
  - Datasheets - Absolute Maximum Ratings: T1: $\mathbf{P_{max}}$ **= 1W;** T2: $\mathbf{P_{max}}$ **= 0.96W**
  - For steady operation: ΔT_{rise} = 125°C → $\mathbf{T_j \geq T_{j,max}}$

2. Function analysis

- Function T1, T2: Switch if $V_{BE} > V_{threshold}$ → Function Bootstrap Bias (Aux PS): Power RaToPUS control circuits if V_{out} ≠ 12V (at start up)
  - >< Malfunction: No control circuits powering
- During nominal operation: T1, T2 only active for 5ms during start up

3. Failure analysis

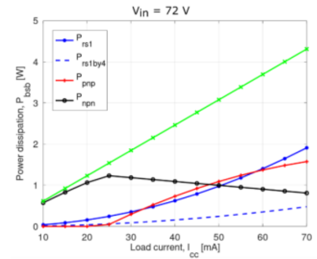
- Potential Failure Causes: 1) P_{diss} > Absolute max. ratings 2) $T_j > T_{j,max}$ If V_{in} = 72V and V_{out} = 0V, either caused by an external PSU shutdown or a short at the output
- Potential T1, T2 primary Failure Modes: 'Short' or 'Open' circuit → No switching
- 2 pot. Failure End Effects: A) 1 RaToPUS (single shorted output): 1) No control circuits powering → 2) No RaToPUS output voltage → 3) Loss of DI/OT PSU redundancy (Maint.)
  B) 2 redundant RaToPUS (external shutdown): … → 3) Loss of DI/OT powering (Comm. loss)

4. Risk assessment

A) Loss of PSU redundancy for DI/OT → Severity: Low (3) - Loss of redundancy; maintenance required Occurrence probability: Low → Criticality: Low
B) Loss of DI/OT powering → Severity: High (6) - DI/OT failure; Periph./FB communication loss Occurrence probability: Low → Criticality: **High**

5. Optimisation

Various options: (ongoing & yet to be decided)
1) Increase T1,T2 copper area to improve cooling
2) Add additional series resistors before transistors to reduce T1, T2 power dissipation
3) Potential use of other transistors
4) Connect existing, unused OTP circuit to detect and reduce overheating
5) Diagnostic parameters monitoring (MoniMod)
6) Design changes to reduce predicted radiation degradation (30 to 40mA increase over 12 years)
7) Reduce current consumption using the available 2nd loop compensation (however potential stability problems)
8) [Take design precautions to reduce the risk of a short at the output induced by environment factors]
9) [Remodel the sink current in the bootstrap bias by increasing the model accuracy (previous conservative assessment)]

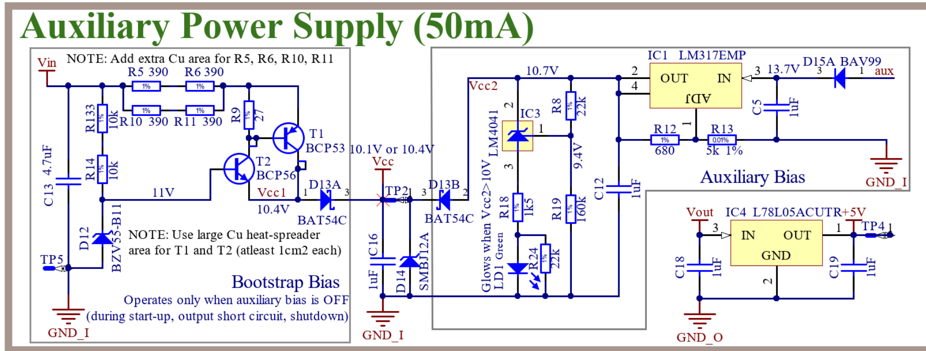


Input from L. Patnaik

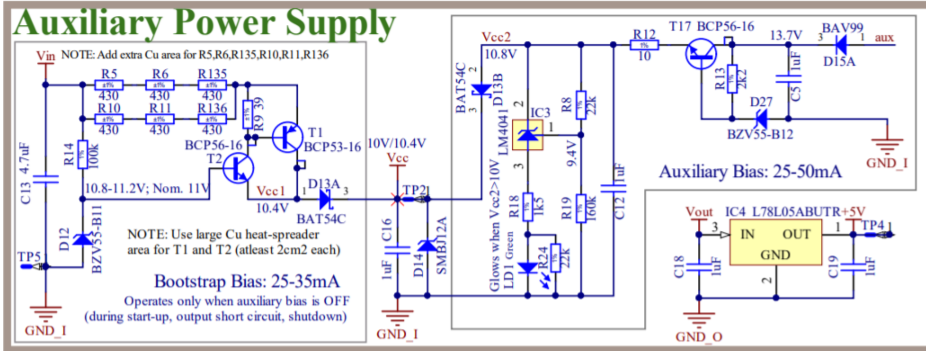
Presented during: BE-CO Technical Meeting, 08.10.20

RaToPUS - Some v2 Optimisations

V1:



V2:

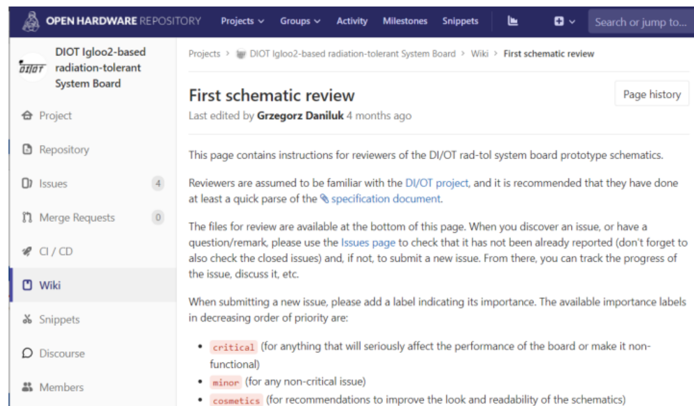


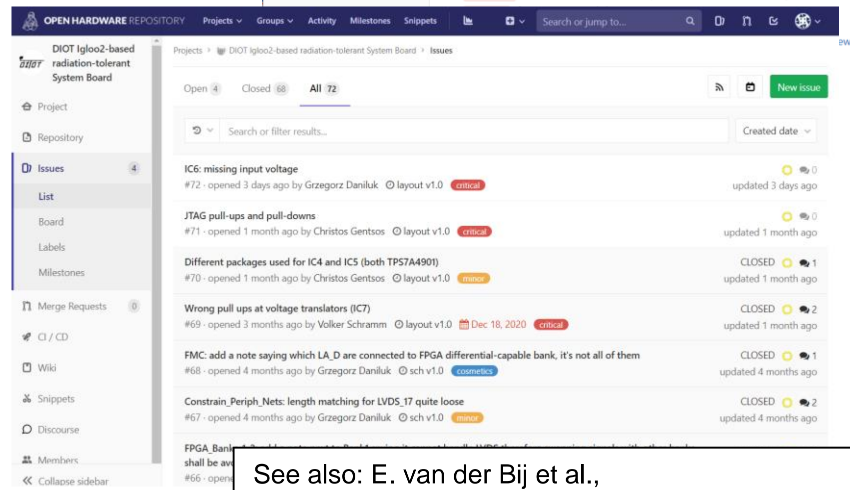
- Divert heating from T1 and T2 to the series resistors using more resistors with larger series resistance
- Change R9 from 27Ω to 39Ω to employ T1 at lower I_{CC}
- Increased T1, T2 copper areas to improve thermal management
- Efficiency improvements:
  - Single 100kΩ resistor for R14+R133 (10kΩ) to reduce standby power
  - Zener-BJT-based solution for auxiliary bias to reduce voltage reference drift

Work of L. Patnaik

Design Reviews

- Long existing practice within BE-CEM (BE-CO)
  - V1.0 → Review invitation to experts
  - Feedback: Issue creation on OHWR
  - Communication via issues
  - Follow-up meeting after deadline
- e.g. Radtol System Board (C. Gentsos):
  - Feedback within 72 issues:
    - Critical
    - Minor
    - Cosmetics
    - Question





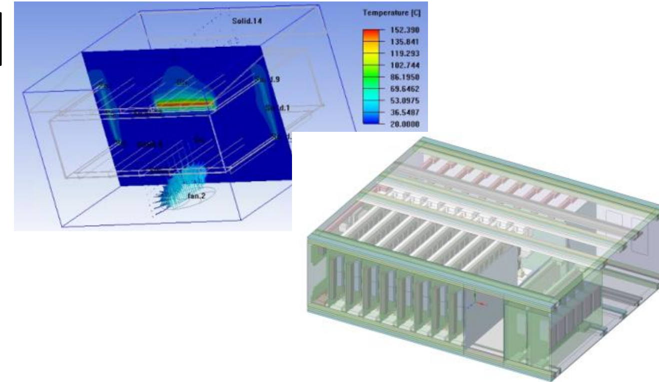
See also: E. van der Bij et al.,
https://ohwr.org/project/ed/wikis/Schematics-design-reviews

Simulation

Ongoing & TBD

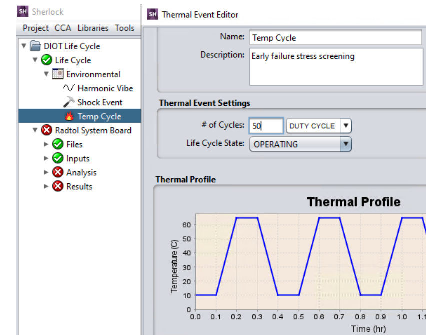
1) Thermal simulations using Ansys Icepak
   - PCB assembly level
   - Full DI/OT crate

Work of C. Gentsos



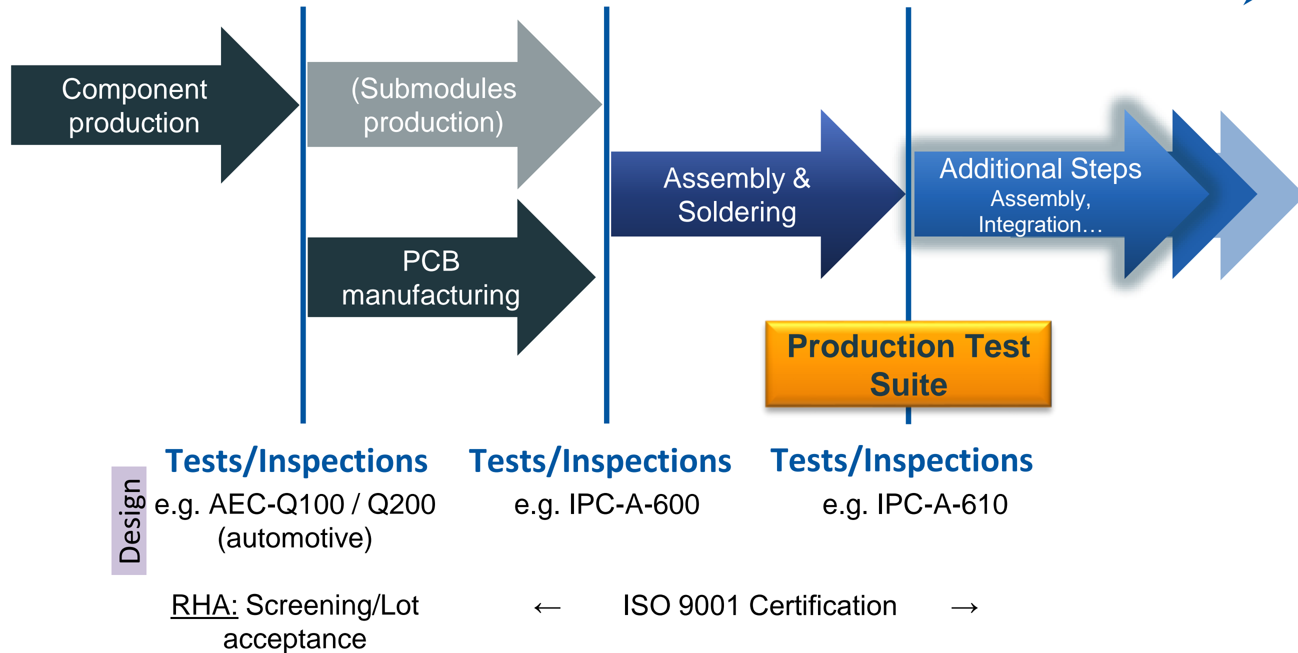
➡ Optimisation + Reliability prediction input

2) Life cycle reliability simulation using Ansys Sherlock
   - Temperature Cycles (Stress Screening)
   - Mechanical Shock
   - Vibration



Production Phase - 1 slide

~> 2022



- Quality Assurance:
  - Applicable standards
    - ISO 9000 family
    - Acceptance criteria: IPC & JEDEC framework
  - Process Control
    - Process FMEA
    - Inspections & tests
  - Handling & transport

BackUp - CERN Resources for Production

https://ohwr.org/project/ed/wikis: Erik van der Bij et al.

- Template "Technical Specification for assembled PCB products"; other IPT templates
  - Applicable standards
  - Functional Test(s): Production Test Suite (PTS)
  - Traceability
  - Packaging, Storage, Transport, Documentation,
- Best Practices for Quality
- Quality Control and Assurance

3.9.3 International Standards

For the manufacturing of PCBs:

- IPC Standards IPC-4552, IPC-4101/94, IPC-4562/3 CU-E3 class 2, IPC-TM-650, IPC-DR-572, IPC-4761, IPC SM 840 class H, J-STD-609, IPC-2221 and IPC-2222 type 3 class2, IPC-A-600 class 3, IPC-6011 and IPC-6012 class 3, IPC-TM-650.

For the assembly of PCBs:

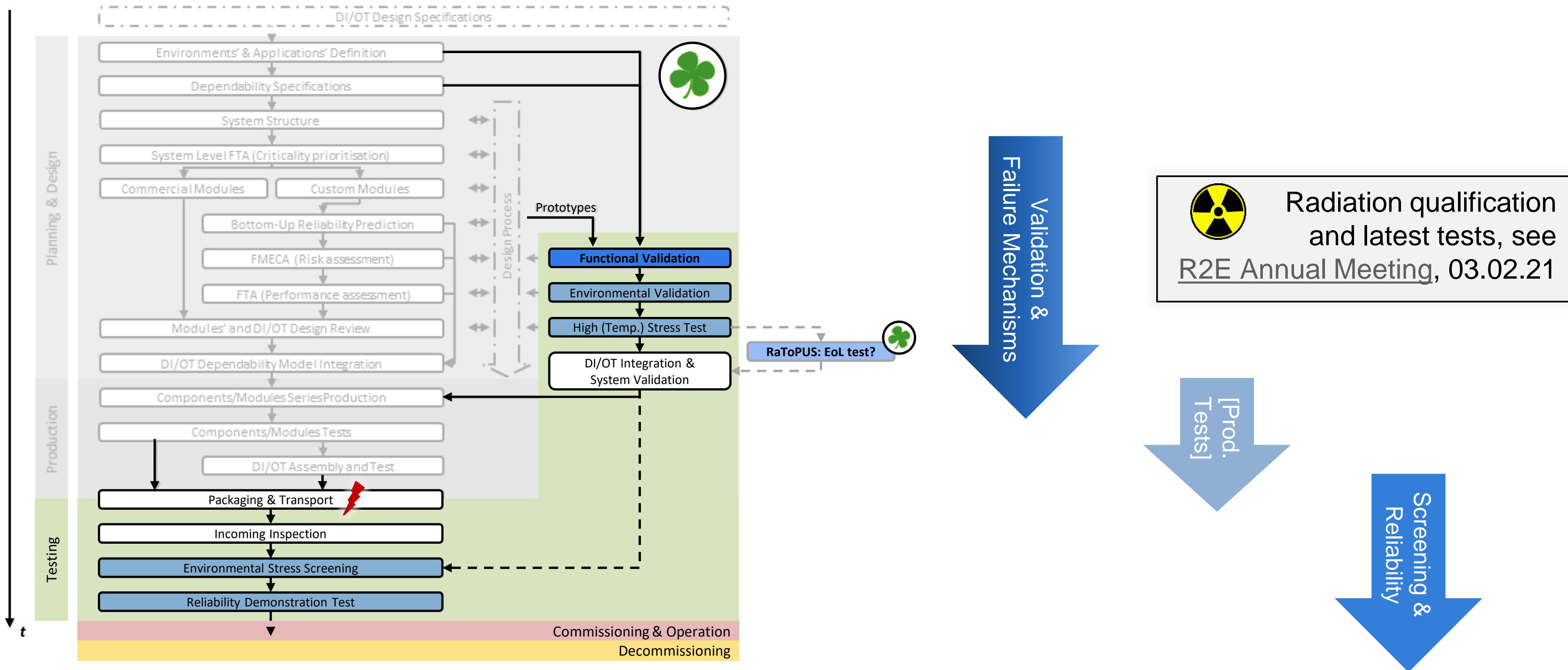
- IPC Standard IPC-A-610 (Class 2);
- IPC Standard IPC/EIA J-STD-001 (Class 2);
  - Cleanliness Designator C-22 (both sides of assembly to be cleaned; test for ionic residues required on 10% of the boards produced).

In case of conflict, IPC-A-610 takes precedence over IPC/EIA-J-STD-001.

Design Review (checklists):

- OHWR (E. van der Bij et al.)
- EDMS (B. Todd et al.)

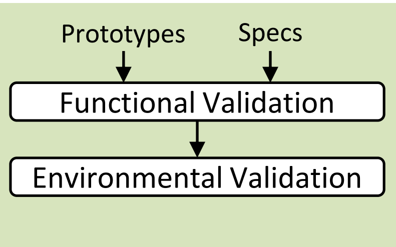
Testing Phase



Radiation qualification and latest tests, see R2E Annual Meeting, 03.02.21

Testing Phase:

Validation & Failure Mechanisms



- Validate all modules' and system functionalities at top performance
- Validate potential operational and life cycle environments

User survey: (operation)

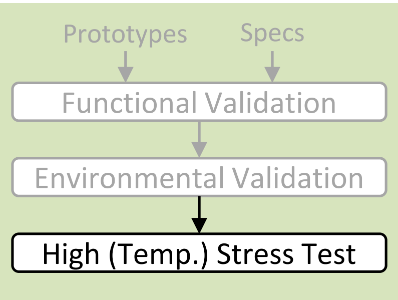
Parameter	Value
$T_{a,max}$	40°C
$T_{a,min}$	10°C
RH_{max}	80%
$Dose_{max}$	500 Gy; 25 Gy/a
$P_{diss,max}$(only periph.b.)	50 W
Max. power cycles	360/a (tbc)
Max. mating cycles	<5/a
Mech. stress	No
Magn. fields/EMI	No

- Constant T; RH
- Cycling T; RH
- TBD: Power cycles
- TBD: Combined T + RH + PC

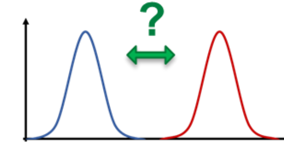
- Mechanical Shock/Vibration → Only Ansys Sherlock simulation (tbd)
- Radiation → RHA

Testing Phase:

Validation & Failure Mechanisms

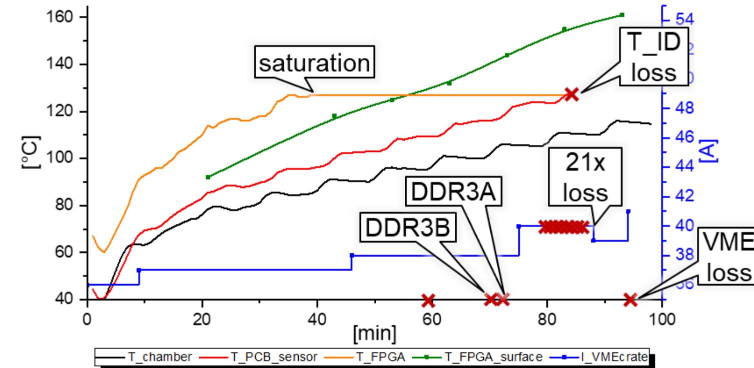


- Trigger potential design weaknesses & (wear out) failure mechanisms
- Determine design robustness
- Feedback/validate production process



- Increasing <u>temperature</u> in steps until failure (destructive)
- Distinction between:
  - Functional errors (tolerance/robustness) &
  - Hardware failures (wear out)

e.g. VFC-HD high temperature test 27.11.2018:



Testing Phase:

Wear out?

Required DI/OT lifetime: 20 years

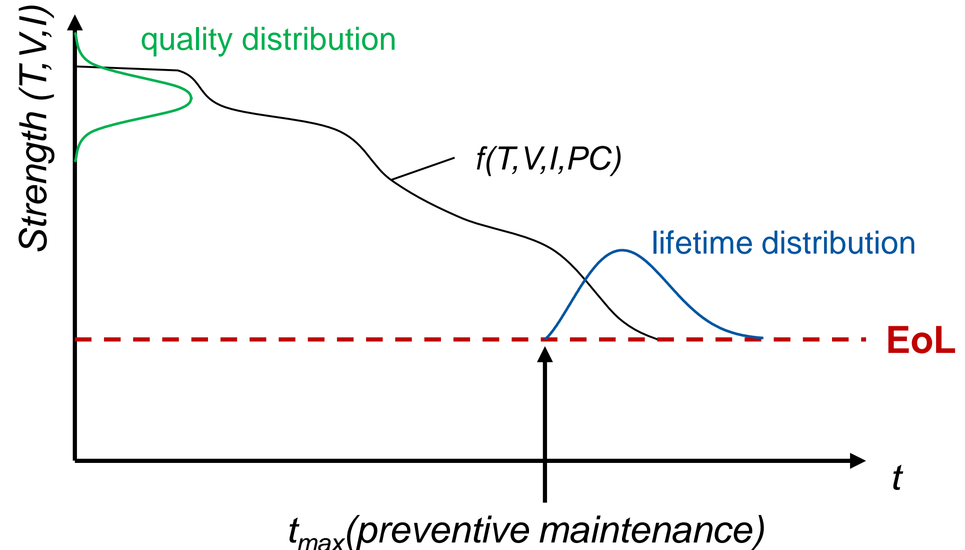
PSU lifetime benchmark: << 20 years

Testing Phase: Validation & Failure Mechanisms → EoL Test?

TBD !

High (Temp.) Stress Test

RaToPUS: EoL Test?

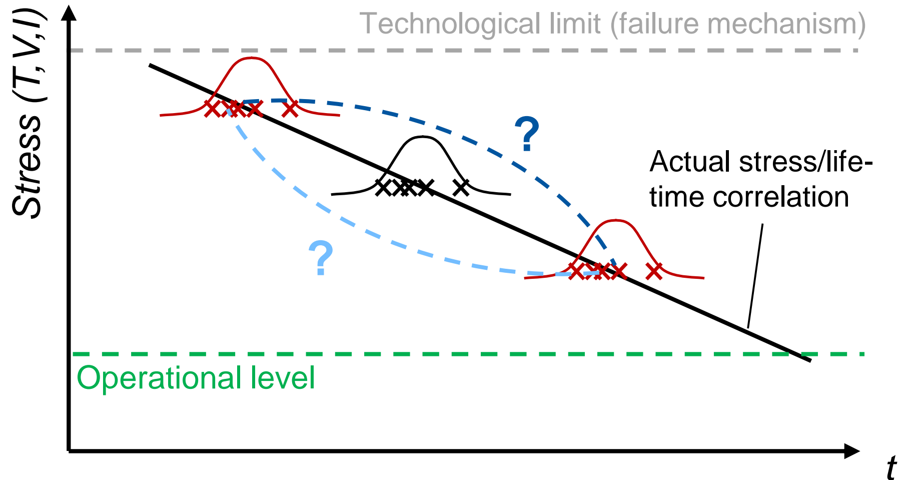


Goals:

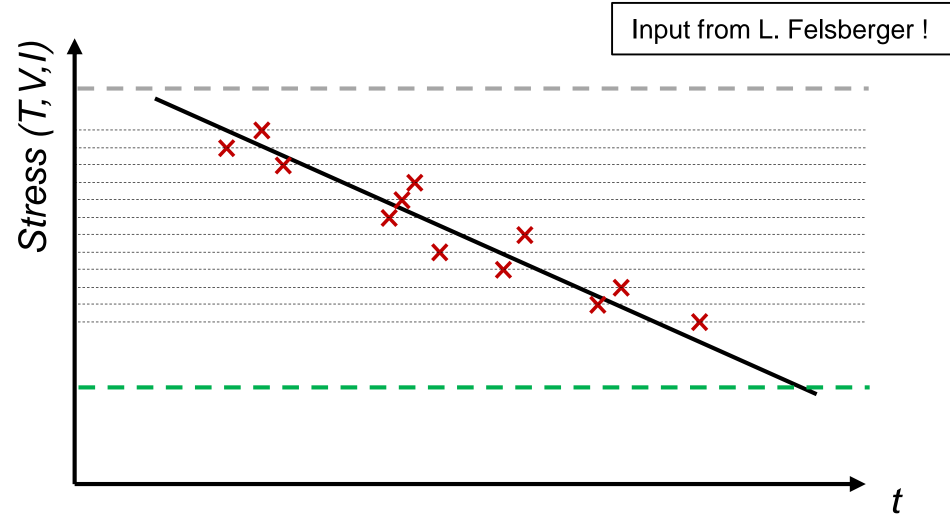
- Determine EoL failure mechanism(s) &
- Determine *t(EoL)* for preventive maintenance

TBD !

EoL Test - 2 Approaches



Input from L. Felsberger !



Some challenges (both approaches):

- Failure mechanisms and stressors are yet unknown
- New failure mechanisms triggered at high stress?
- Available acceleration model?
  - Several stressors and combined effects?
    - ➢ Radiation dose effects?
- Extensive resources (samples etc) required:
  - Testing for potential failure mechanisms
  - Tests to determine technological limit
  - Several stress levels to be tested
  - Tests to overcome statistical spread
- ...

EoL Test - Alternative

TBD !

1) EoL determination

+ Precise EoL time for efficient preventive maintenance
+ Low operational risk (wear out)

2) No EoL test, only high stress test

+ Existing PSU redundancy !
+ EoL failure mechanisms can be identified by high stress test (focus on critical components)
+ MoniMod may be able to diagnose parameter degradation in operation (*V*, *I*); even before first failure

- Higher operational risk
- EoL determination based on operational failures
- Degradation on field level unknown
- 100% failure monitoring and analysis during operation necessary !

Testing Phase:

Screening & Reliability

~> 2022

Series production

Environmental Stress Screening

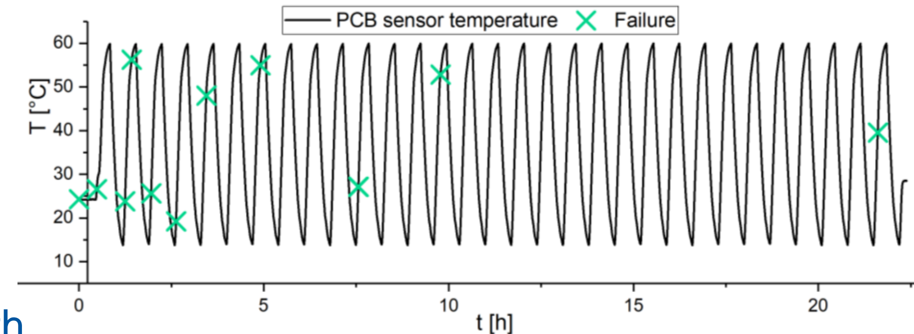
Reliability Demonstration Test

Goals:

- Trigger potential latent defects and surpass early failure period
- Elevated stress to reduce testing time

Definition & Execution:

- Stress = temperature cycles
    - Very efficient stress
    - Good experience with VFC-HD (22h; 5...50°C; 90% RH-peak)
- Inputs:
    - Acceleration models / Screening strength
    - Previous high stress tests data
    - Component datasheets: T_{max}, T_{min}



VFC-HD temperature cycle screening

Testing Phase:

Screening & Reliability

~> 2022

User survey:

Min. MTTF	36/92/106/176/**877 kh**
$T_{a,max}$	**40°C** [NanoFIP 50°C]

Series production
↓
Environmental Stress Screening
↓
Reliability Demonstration Test

Goals:

- Demonstrating an upper failure rate for λ=const. (2nd bathtub region)
  - Wear out modules → Preventive maintenance !
- Additional confidence of surpassing the early failure period

Achievable MTTF:

CL=90%; $T_{nominal}$=25°C **0-failure** [1-failure]	MTTF [kh]	MTTF(Arrhenius, E_a=0.3eV) [kh]
Test temperature	25°C	40°C
200 DI/OT; 2 weeks	29 [17]	50 [30]
200 DI/OT; 4 weeks	**58** [34.5]	101 [60]
200 DI/OT; 6 weeks	87 [51.5]	152 [90]

e.g.

MTTF 200x 22h ESS*: 1.9kh
MTTF 200x 4 weeks Run In: + 58.1kh
MTTF 4 weeks commissioning: + (58.1kh)

60kh (118kh)

= Maximum 1 failure every 6.8 (13.5) years

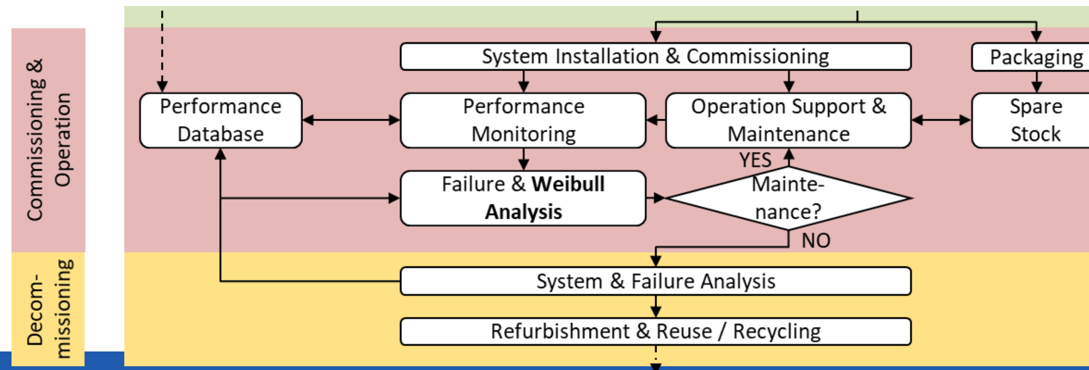
*failure mechanisms successfully triggered and/or remedied

Operation Phase

- Performance monitoring using InforEAM:
  - Operational validation (extended Run In)
  - Failure mechanism identification and analysis

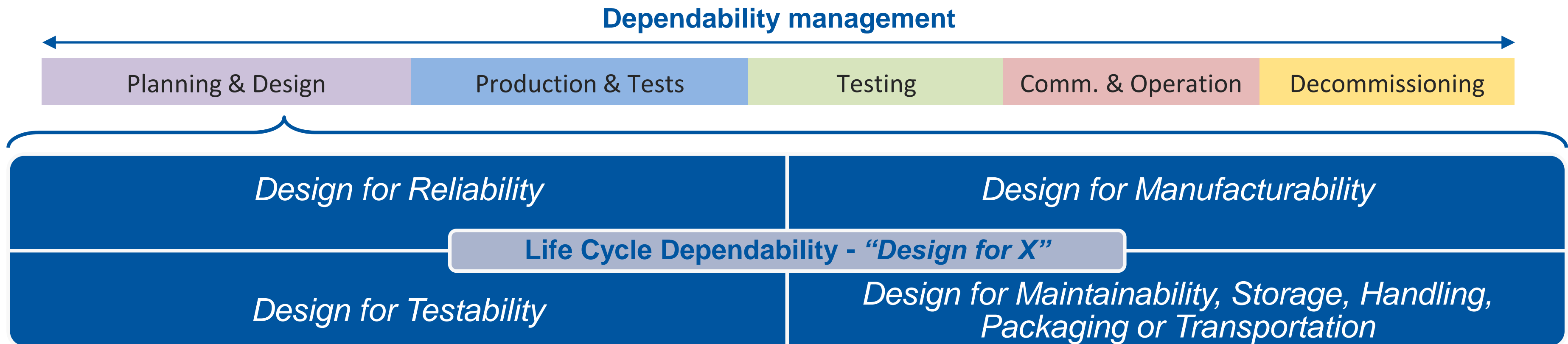
    → Weibull Analysis (not only RaToPUS)
- Maintenance strategy & spare management

Parameters to be tracked:
- ID, production batch, …
- PTS result(s)
- Inspection steps
- Screening + Run In results
- Location/Time of installation(s)
- Maintenance interventions
- Repairs
- Operational parameters

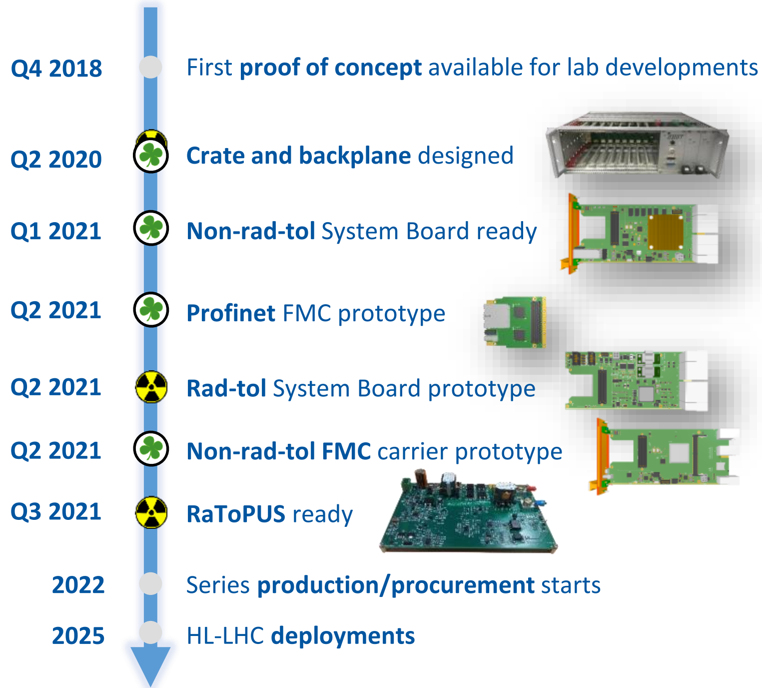


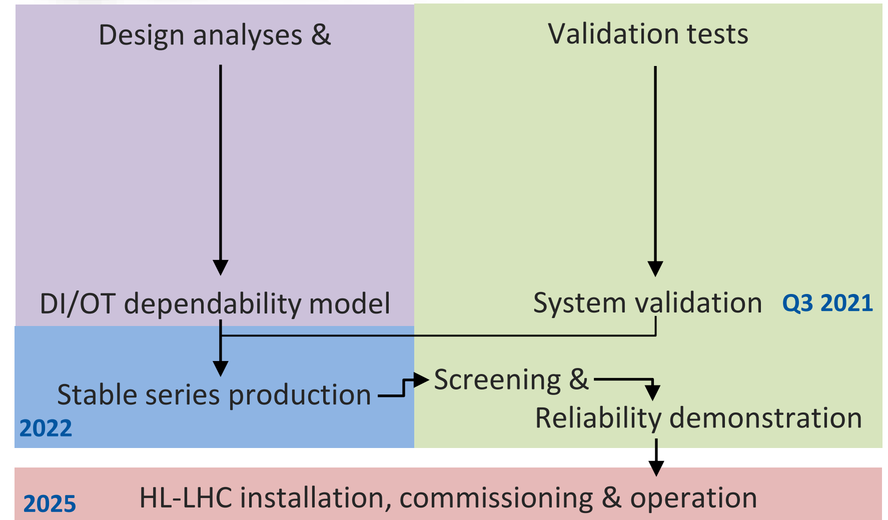
Summary

- Methodological approach to assure dependability throughout the entire life cycle
  - ➢ Adressing the entire life cycle already during the ongoing design phase:



Outlook





Thank you for your attention !

Questions?