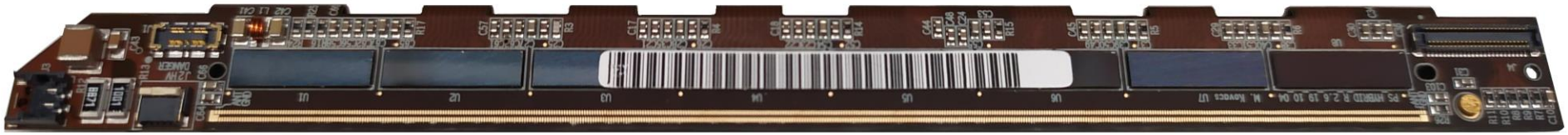
A Tracker detector module for particle discrimination: Hybrid design challenges



A PS-FEH-R18 prototype

Mark Istvan Kovacs on behalf of the Hybrid Working Group

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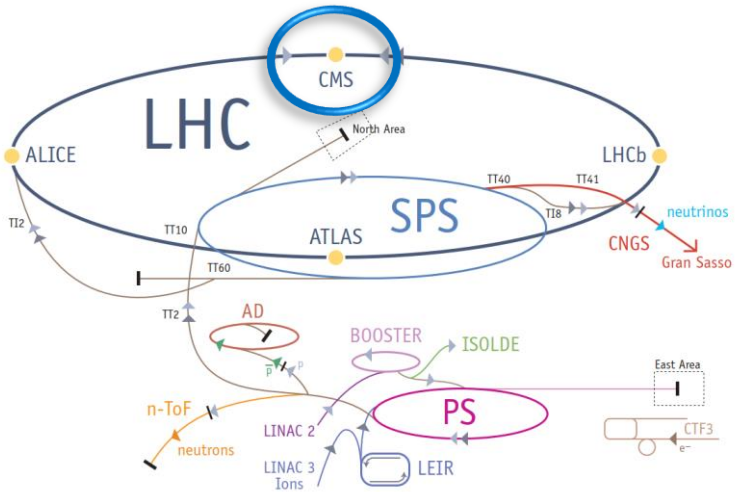
Outline:

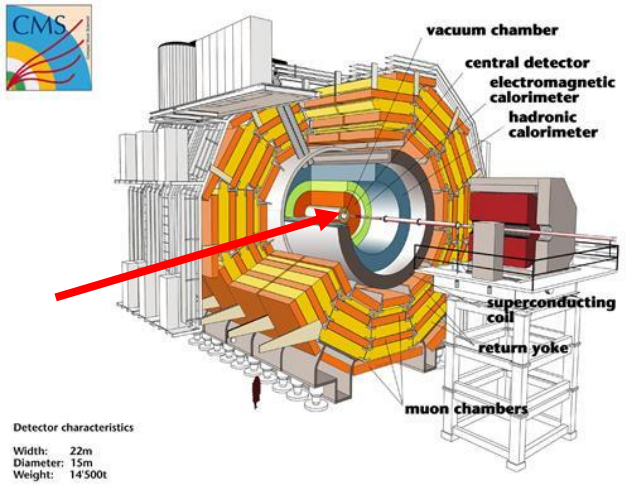
1. Introduction of CMS Phase-2 upgrade
2. Introduction of hybrids, architecture, build-up and design practices
3. History of hybrid prototypes, tests, prototype issues and solutions
4. Current hybrid designs for the pre-production
5. Hybrid testing, test system, test cards and system verification
6. Co-design example, conclusion of hybrid part

CMS: Compact Muon Solenoid; **PS**: Pixel-Strip type module; **PS-FEH-R18**: PS Front End Hybrid, right 1.8 mm spacing

The Compact Muon Solenoid (CMS) is a general-purpose detector designed to cover the widest possible range of physics at the LHC, from the search for the Higgs boson to supersymmetry (SUSY) and extra dimensions.



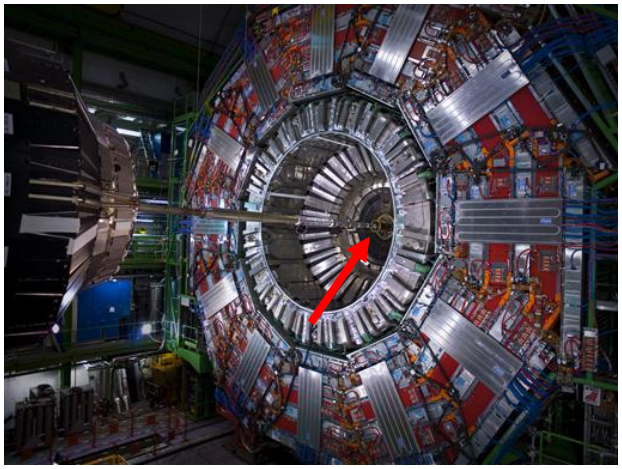
The collider complex of CERN



3 dimensional cross section of CMS

Size	46 m long, 25 m high and 25 m wide
Weight	7000 tonnes
Design	barrel plus end caps
Material cost	540 MCHF
Location	Meyrin, Switzerland.

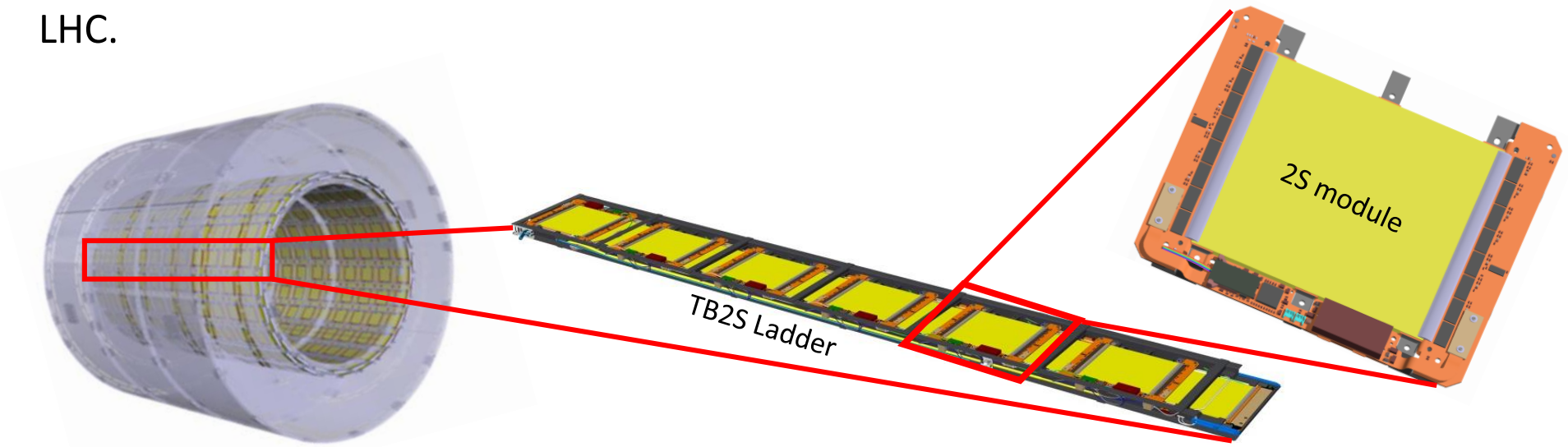
CMS technical parameters



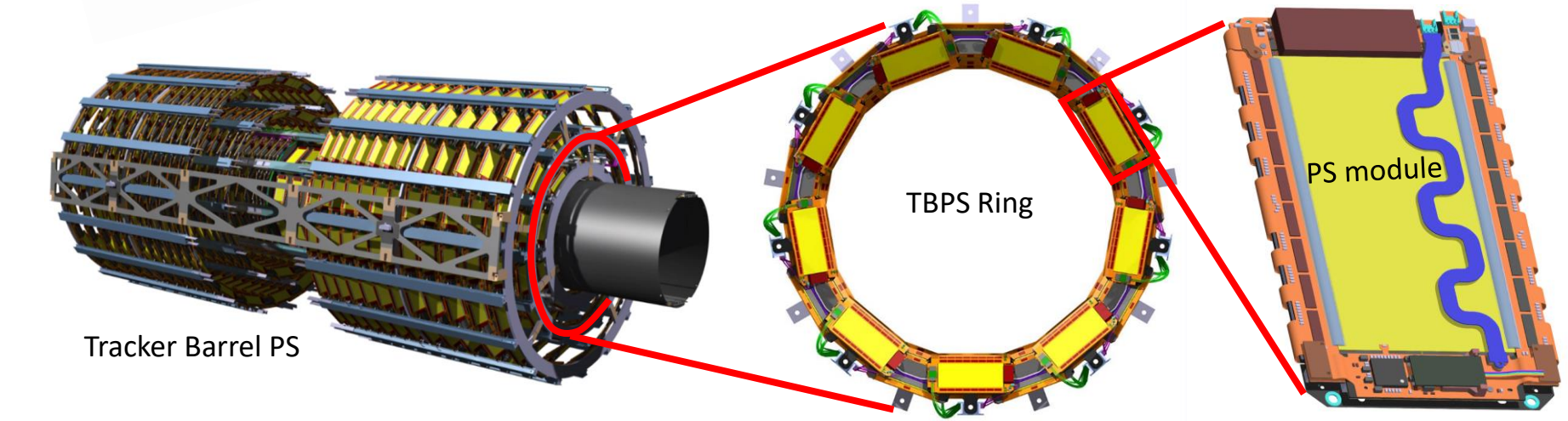
CMS in real, location of the Tracker

HL-LHC: High Luminosity Large Hadron Collider;

The CMS Tracker Phase-2 Upgrade is required to adapt the CMS detector to the 3000 fb^{-1} total integrated luminosity and 14 TeV centre-of-mass energy of the HL-LHC.



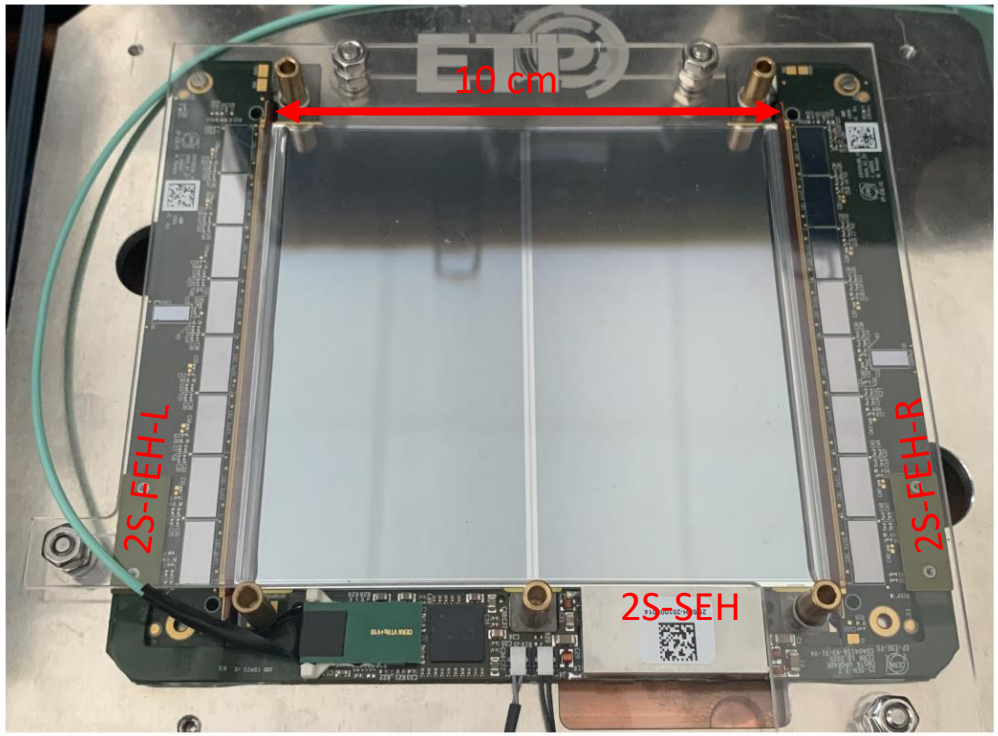
Tracker Barrel 2S



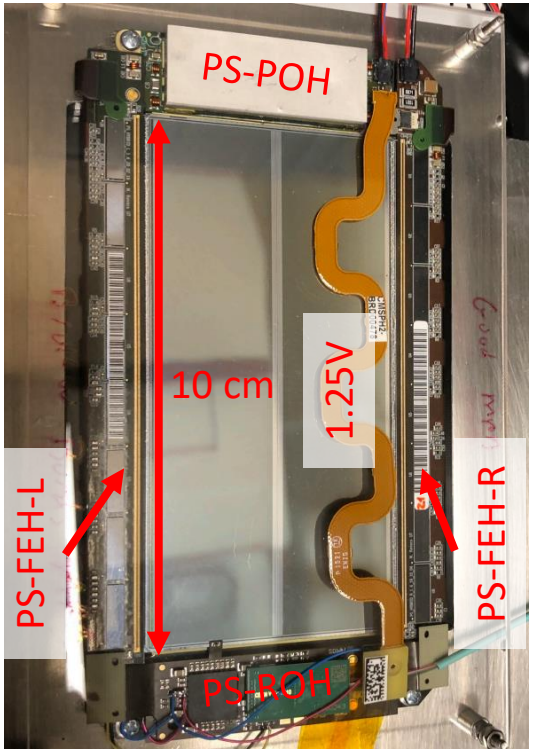
Tracker Barrel PS

TB – Tracker Barrel; **2S** – Strip-strip module; **PS** – Pixel-Strip module

Sensor module prototypes are assembled from multiple pieces, including hybrids, sensors, spacers and stiffeners, in order to validate the ASICs, circuit design and the module design.



A Strip-Strip (2S) module prototype constructed from the latest hybrid prototypes.

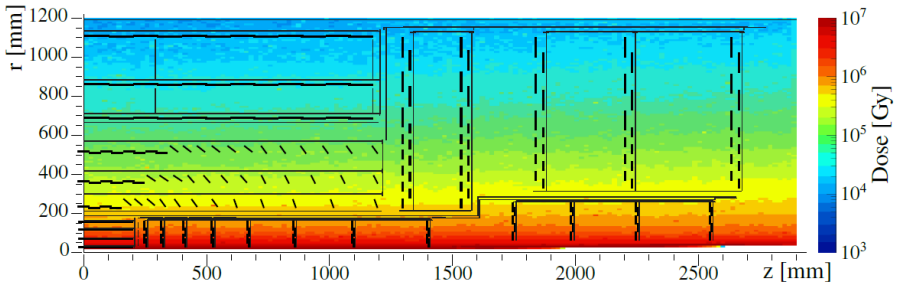


A Pixel-Strip (PS) module prototype constructed from the latest hybrid prototypes.

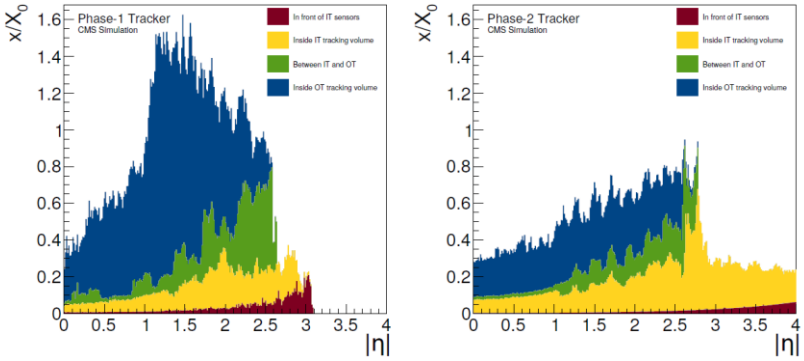
SEH: Service Hybrid; **ROH** – Read-Out Hybrid; **POH** – Power Hybrid; **FEH** – Front-End Hybrid

The requirements for the electronics are the following:

- Tolerate radiation (max. 77 and 14 Mrad expected for PS and 2S respectively).
- Reduce mass and size as much as possible.
- Reliable operation for 15 years.
- Low power consumption (~5.4W per 2S module; 7.8W per PS module[1]).
- Operation in cold, minimize heat transfer to sensors.
- Total number of modules planned: PS: 6730, 2S: 9140

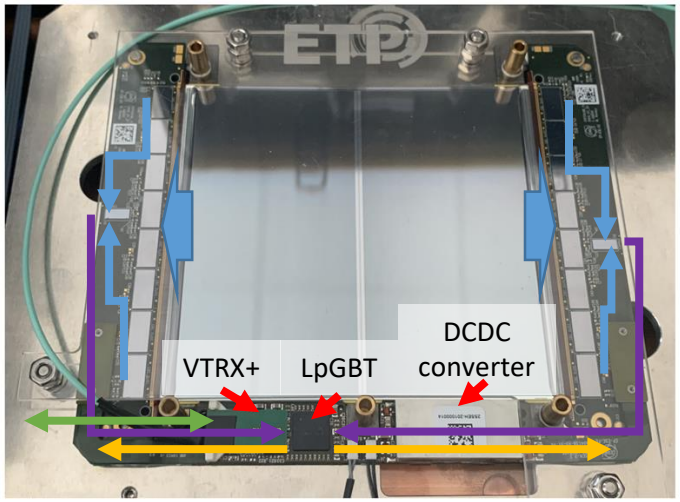


Expected radiation levels in the CMS PH-2 tracker [1]



Estimated material in the upgraded CMS tracker [1]

[1]: The Phase-2 Upgrade of the CMS Tracker Technical Design Report CMS-TDR-17-001



Strip sensor

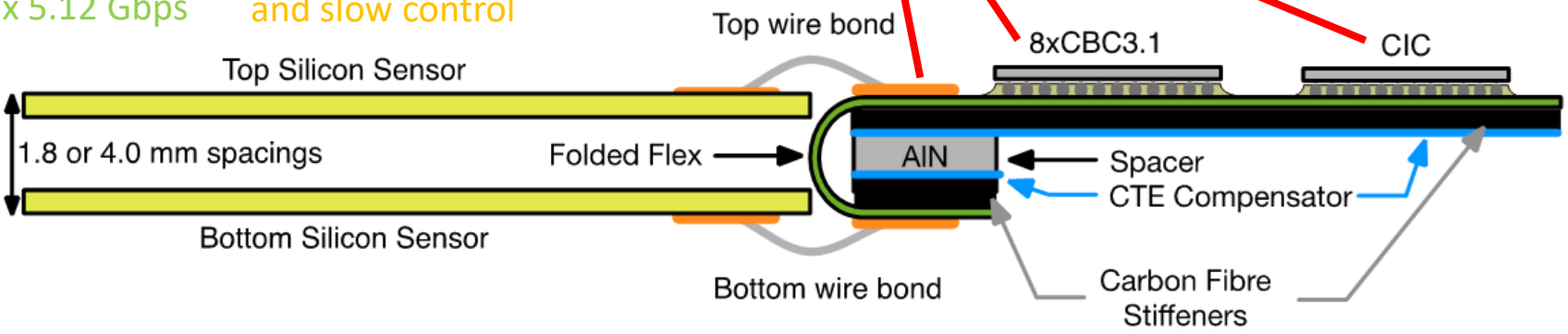
Analogue signal

Sparsified data from the CIC to the Service hybrid

Unsparsified data lines 8 x 6 @ 320 Mbps

Optical interface @ max 5.12 Gbps

Fast command, clock and slow control

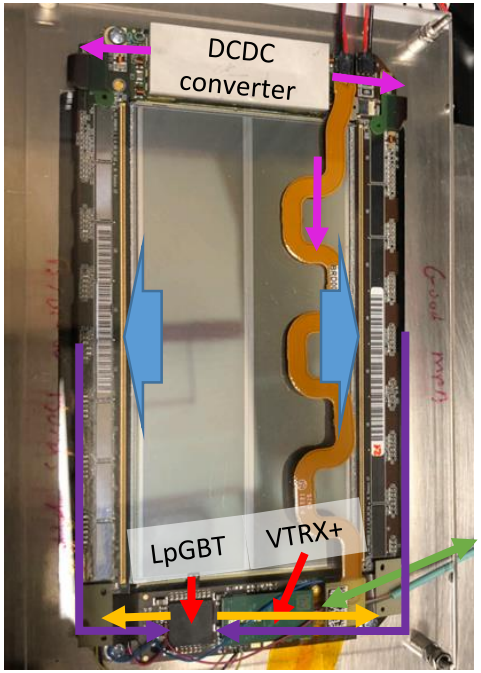


Cross section view of the 2S front-end hybrid construction in a module

CBC3.1 – CMS Binary Chip; **CIC** – Concentrator ASIC; **LpGBT** – Low Power Gigabit Transceiver; **VTRx+** – Versatile Link Plus Transceiver module

2. System architecture of the PS module

Power is provided by the PS-POH

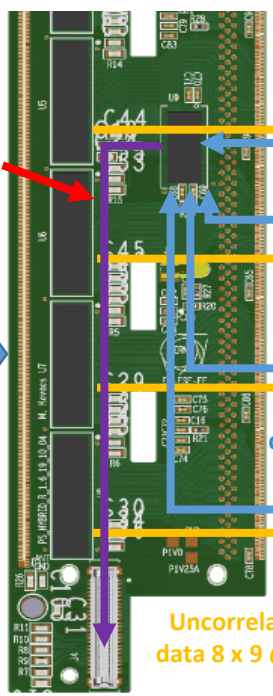


Sparsified digital data Read-out

Strip sensor

Analogue signal

Sparsified digital data Read-out



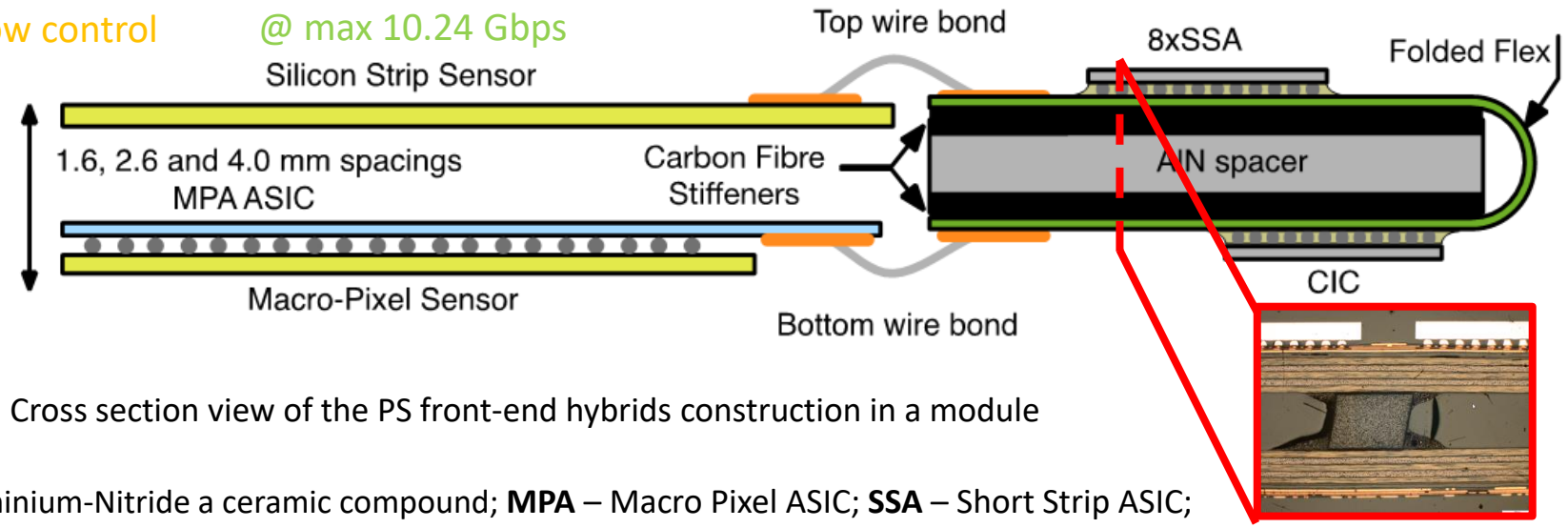
Correlated digital data 8 x 6 @320 Mbps

Uncorrelated digital data 8 x 9 @320 Mbps

Pixelated strip sensor with MPA

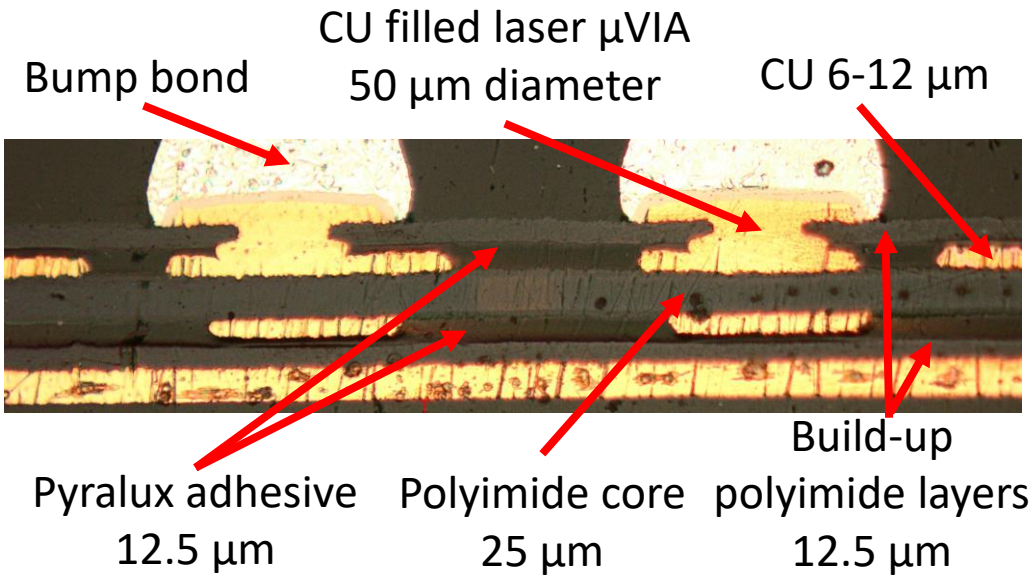
Fast command, clock and slow control

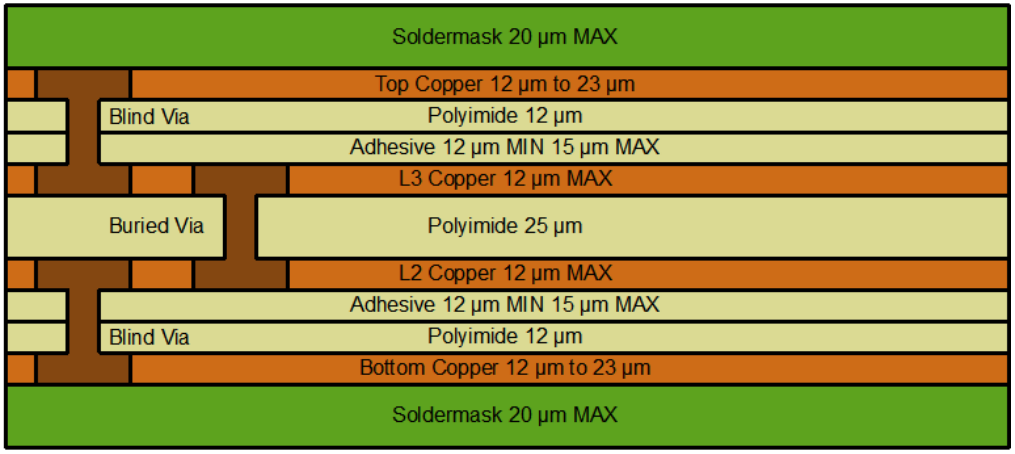
Optical interface @ max 10.24 Gbps



Cross section view of the PS front-end hybrids construction in a module

ALN – Aluminium-Nitride a ceramic compound; **MPA** – Macro Pixel ASIC; **SSA** – Short Strip ASIC;

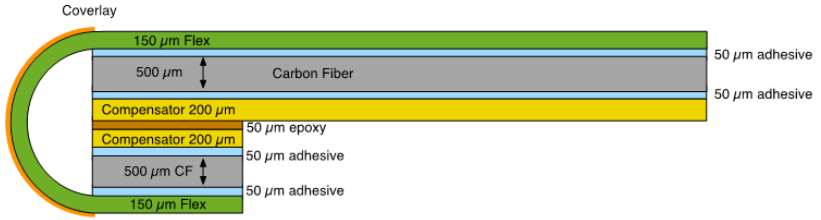




Build-up specification of the 2S-FEH, PS-FEH and PS-ROH

Details:

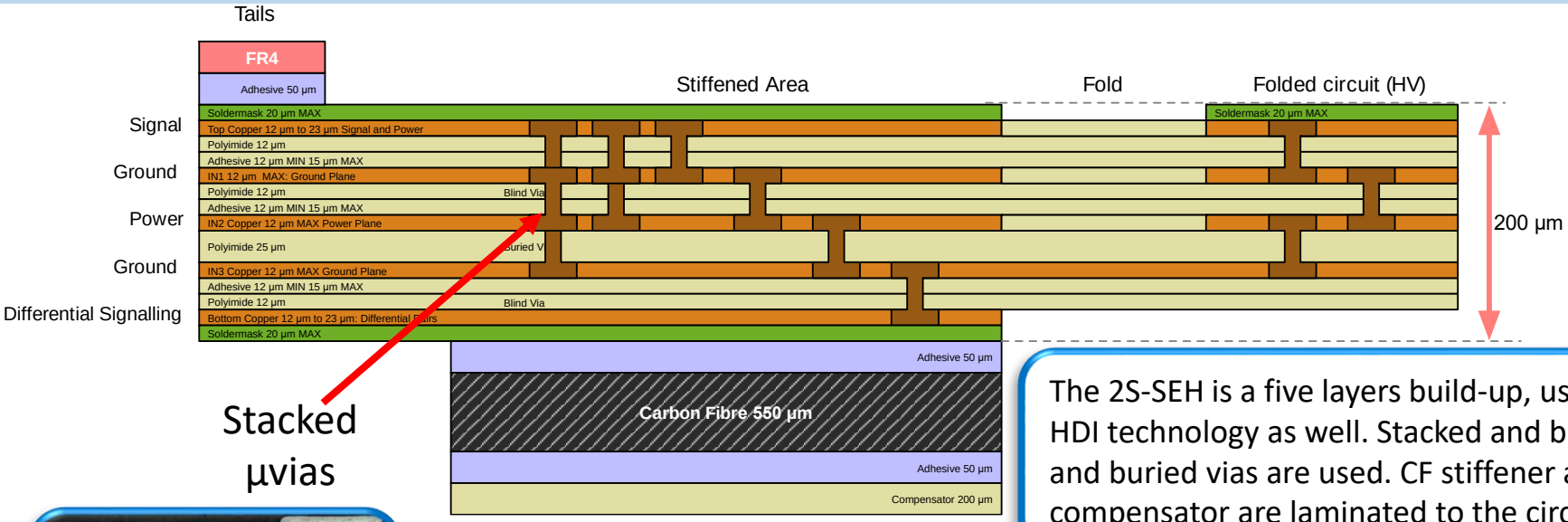
- 4 layers flex circuit
- HDI interconnect technology
- Linewidth and spacing 45/45 µm
- Laser µVias with 25-50 µm drill and 110 µm capture pad
- Carbon fibre reinforced with CTE compensation layer
- Flip-chip ASICs for reduced size and quick assembly
- Folded in order to match sensor wirebonding level



Build-up specification of the folded 2S-FEH

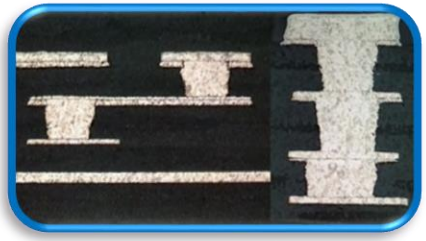
HDI – High Density Interconnect; **CTE** – Thermal Expansion Coefficient; **MPA** – Macro Pixel ASIC; **SSA** – Short Strip ASIC; **CIC** – Concentrator ASIC;

2. Build-up of the 2S-SEH and the PS-POH

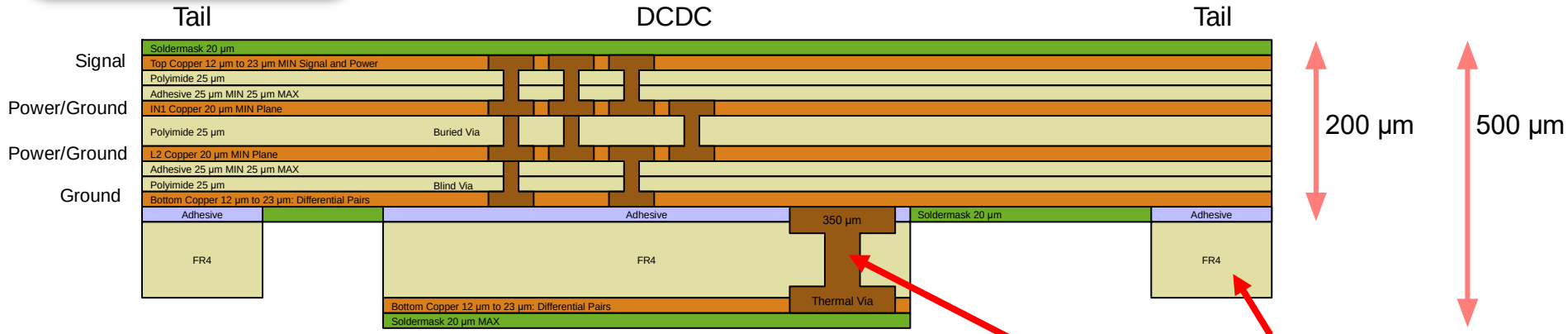


Build-up specification of the 2S-SEH

The 2S-SEH is a five layers build-up, using HDI technology as well. Stacked and blind and buried vias are used. CF stiffener and compensator are laminated to the circuit.



The PS-POH is a 4 layers build-up with HDI technology, but with less demanding feature sizes. No CF stiffener is applied, thermal vias are used to evacuate the heat.



Build-up specification of the PS-POH

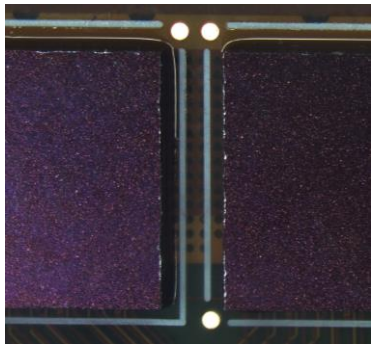
Thermal via in FR4

Connector FR4 stiffener

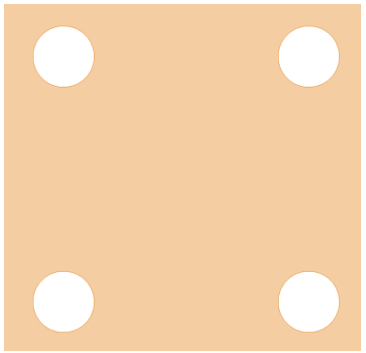
FR4 – Flame Retardant PCB laminate

Few important HDI design practices:

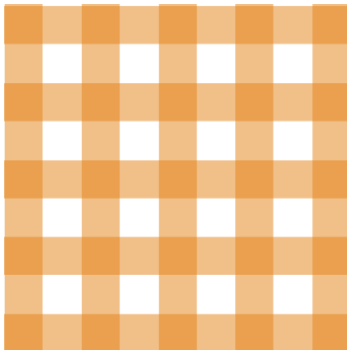
- Use crosshatched copper pattern to improve flexibility.
- Use “teardrops” at trace to pad connections to increase reliability.
- Avoid stacked µvias to further increase reliability.
- Balance copper area to achieve a flat surface, fill unused areas.
- Use “vent holes” to speed-up circuit drying process.
- Use silkscreen or solder mask barriers to control underfill flow.
- Use simulation tools with small size conductors to estimate impedance.



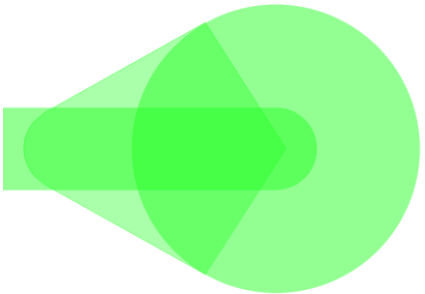
Underfill “barrier”



“vent holes” placed every mm



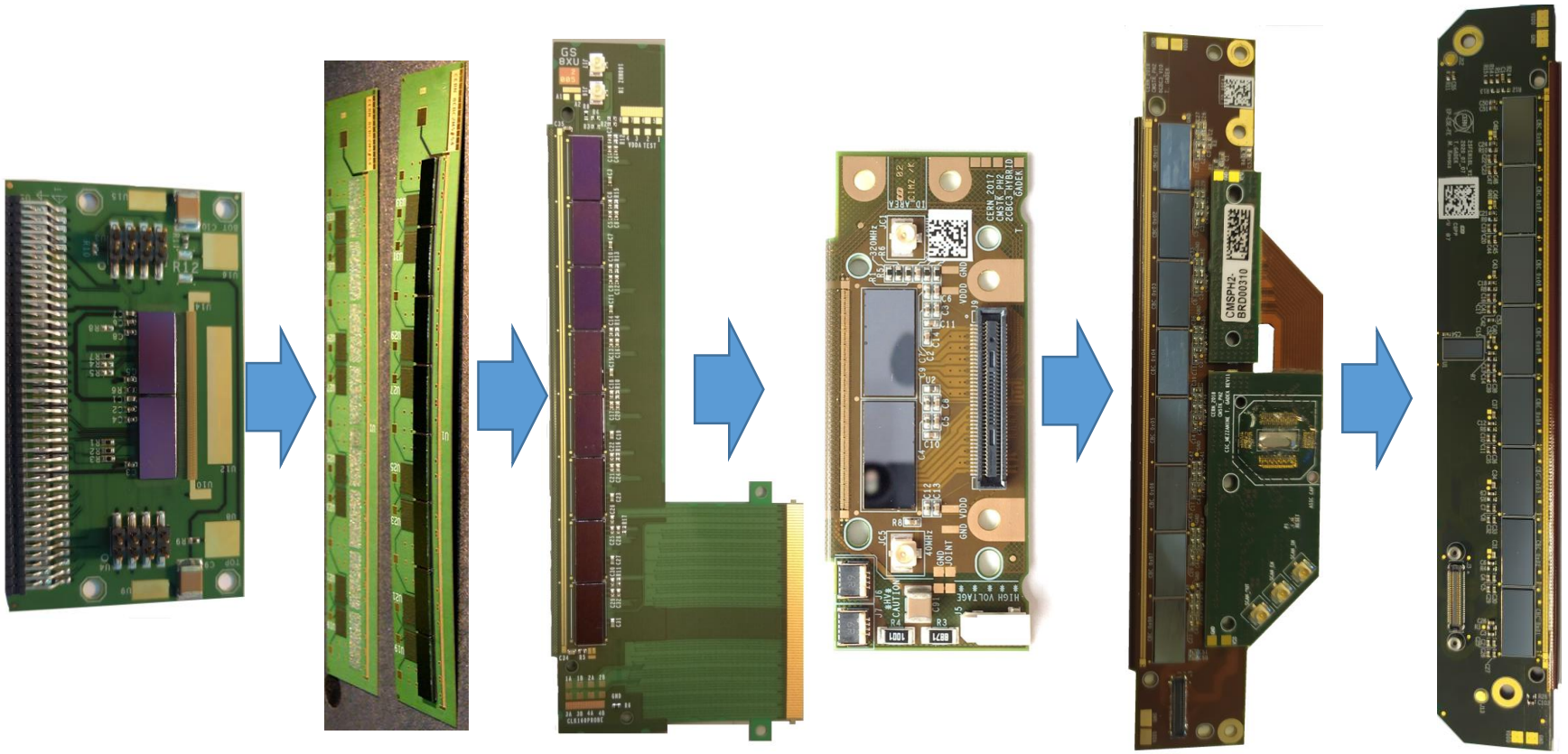
X-hatch can improve flexibility



Teardrop will decrease stress

Many prototype circuits were done for the 2S-FEH development:

- The CF lamination technology was developed using these circuits.



2CBC2 hybrid with rigid 6 layers substrate

8CBC2 mechanical circuit with rigid 6 layers substrate

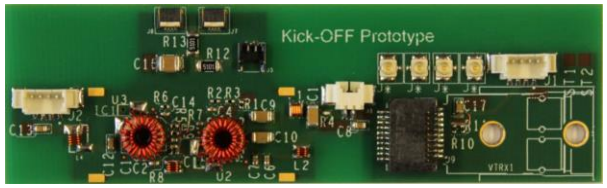
8CBC2 hybrid with CF stiffener glued with double-sided adhesive

2CBC3 hybrid with FR4 stiffened 4 layers flex

8CBC3 hybrid + CIC mezzanine with CF stiffened 4 layers flex and compensator

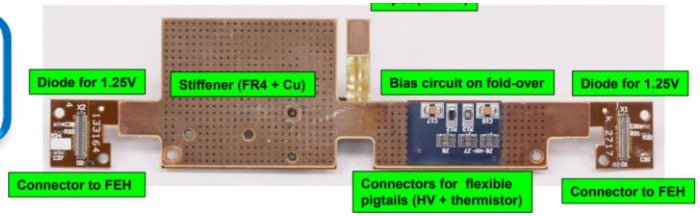
2S-FEH-L with CF stiffened 4 layers flex and compensator, final geometry

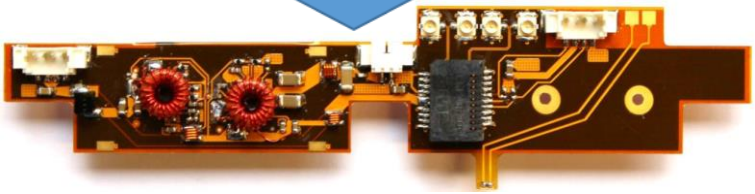
Four prototype circuits were done for the 2S-SEH development:



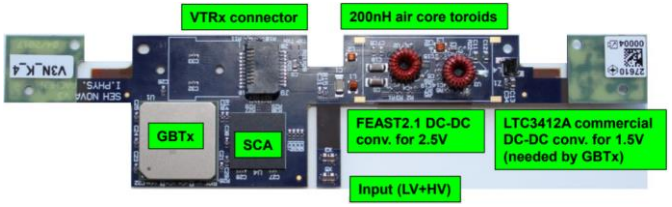
2S-SEH V1 FR4 circuit for first tests

Prototypes by RWTH Aachen

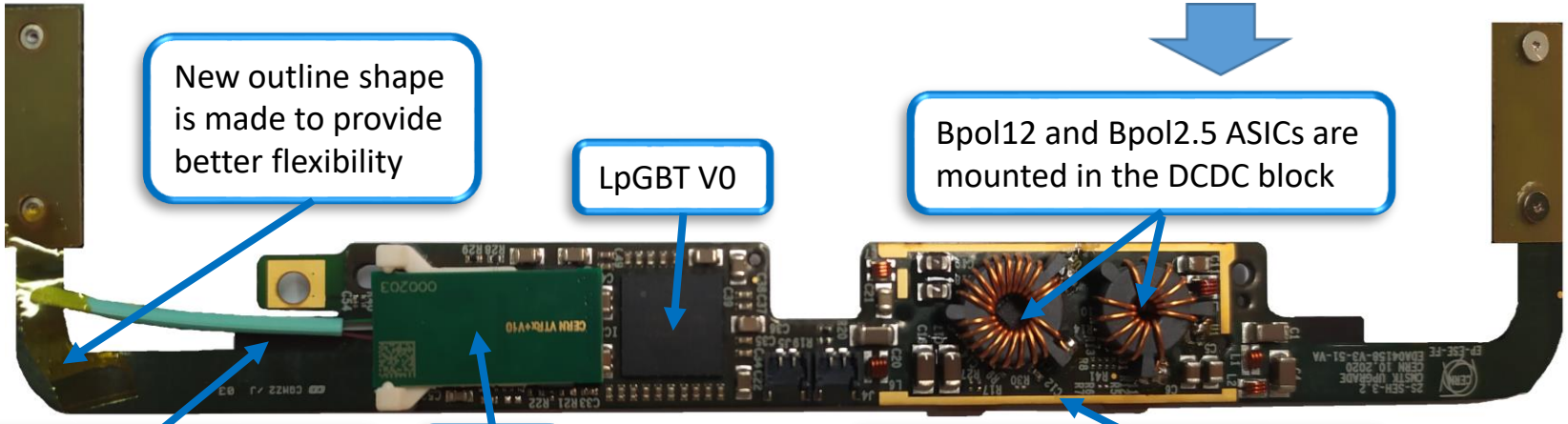




2S-SEH V2 was a two layers polyimide circuit



2S-SEH V3.1 had extended outline, FR4 stiffener and most of it's components were early prototypes



New outline shape is made to provide better flexibility

LpGBT V0

Bpol12 and Bpol2.5 ASICs are mounted in the DCDC block

CF stiffener + compensator

VTRx+

Soldering pad of µmilled shield

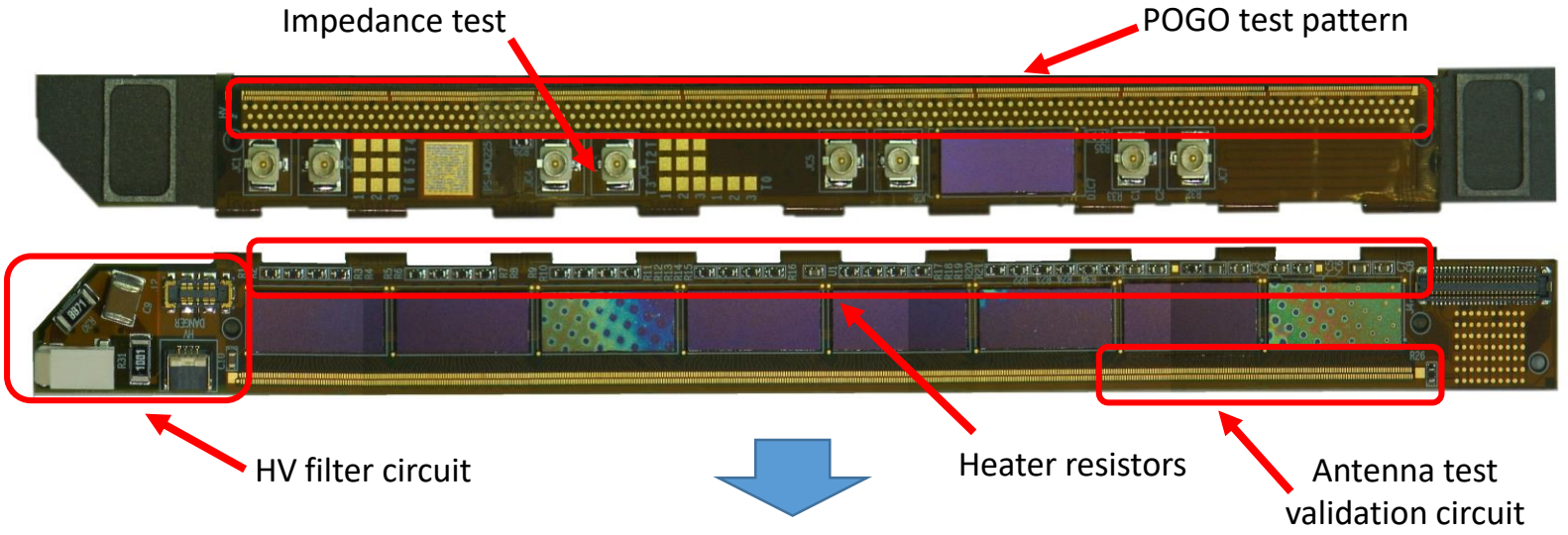
The 2S-SEH V4.1 already uses close-to-final prototypes of all the components. The outline is nearly final.

More details: TWEPP-18 and https://indico.cern.ch/event/1019078/contributions/4444400/

The PS-FEH development started in later phase:

- The experience with PS-MCK and 2S prototypes was essential to succeed with the first prototype.

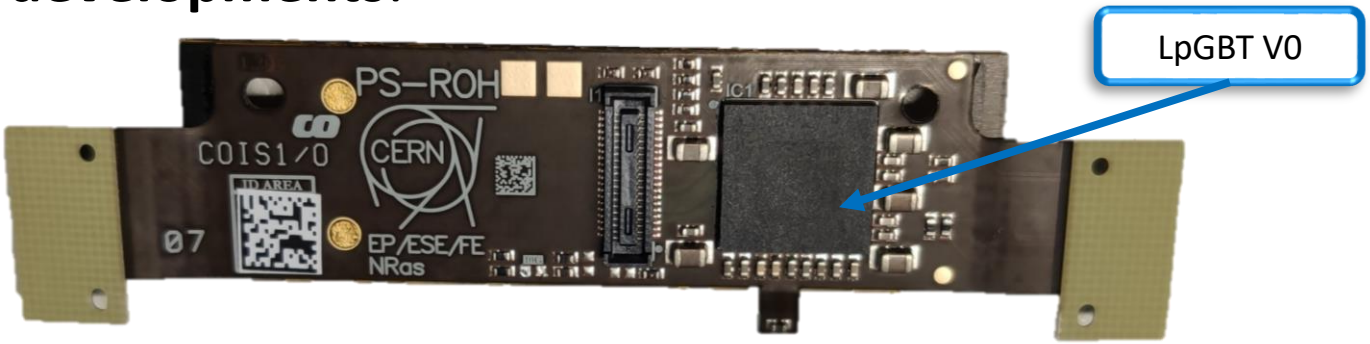
PS-MCK circuit with 4 layers flexible circuit glued with soft adhesive to CF stiffener and folded



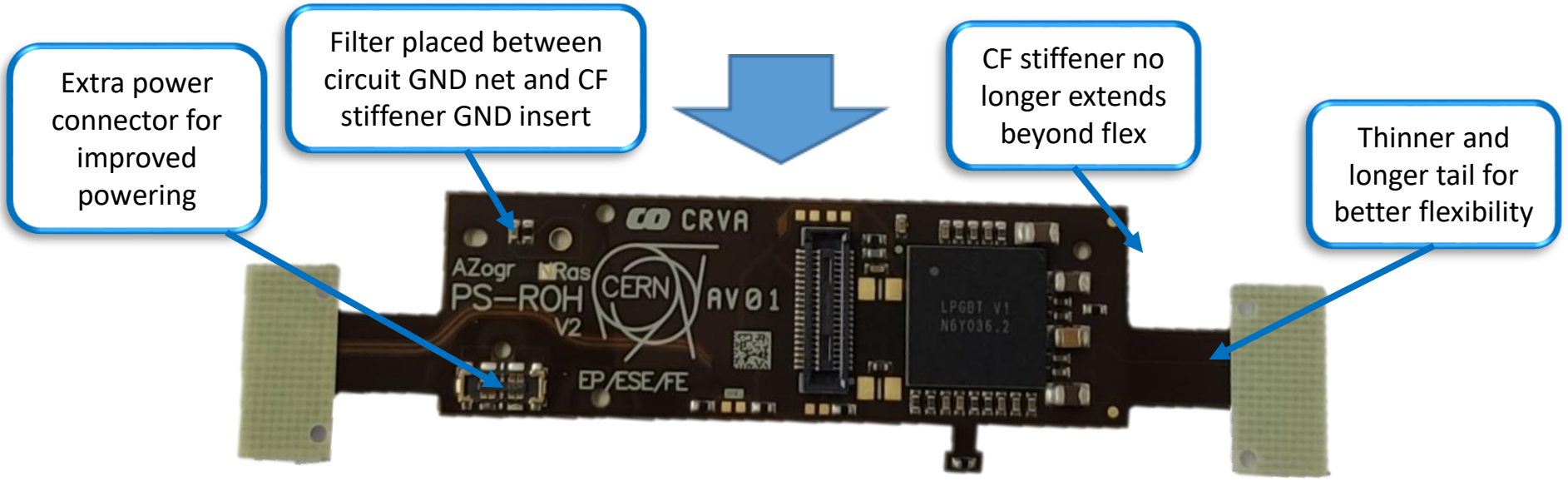
PS-FEH circuit with 4 layers flexible circuit glued with rigid adhesive to CF stiffener and folded

CF – Carbon Fibre

The PS-ROH had two prototypes as it was one of the latest prototype developments:

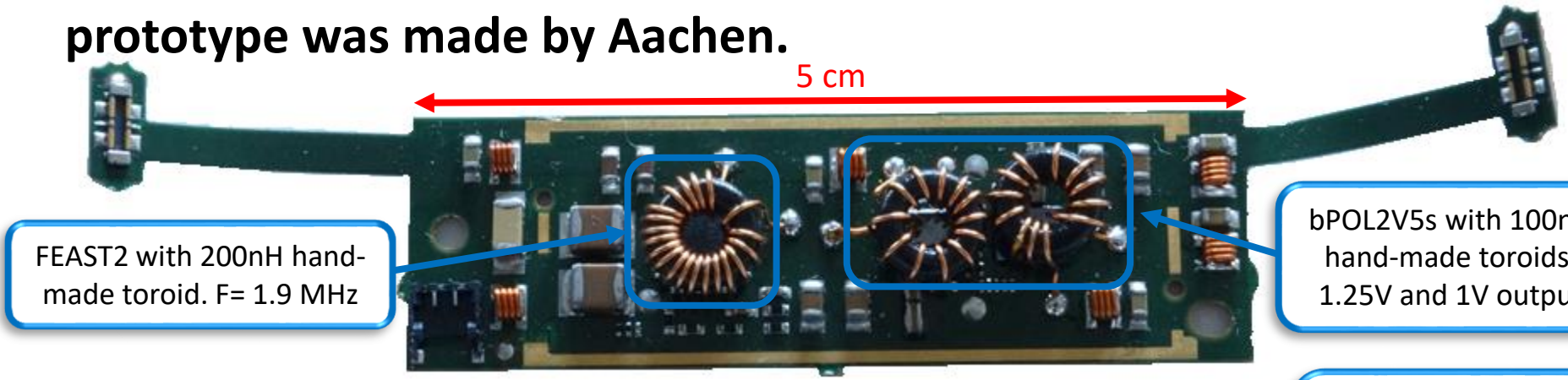


The PS-ROH V1 had an FR4 stiffened version to validate the design.

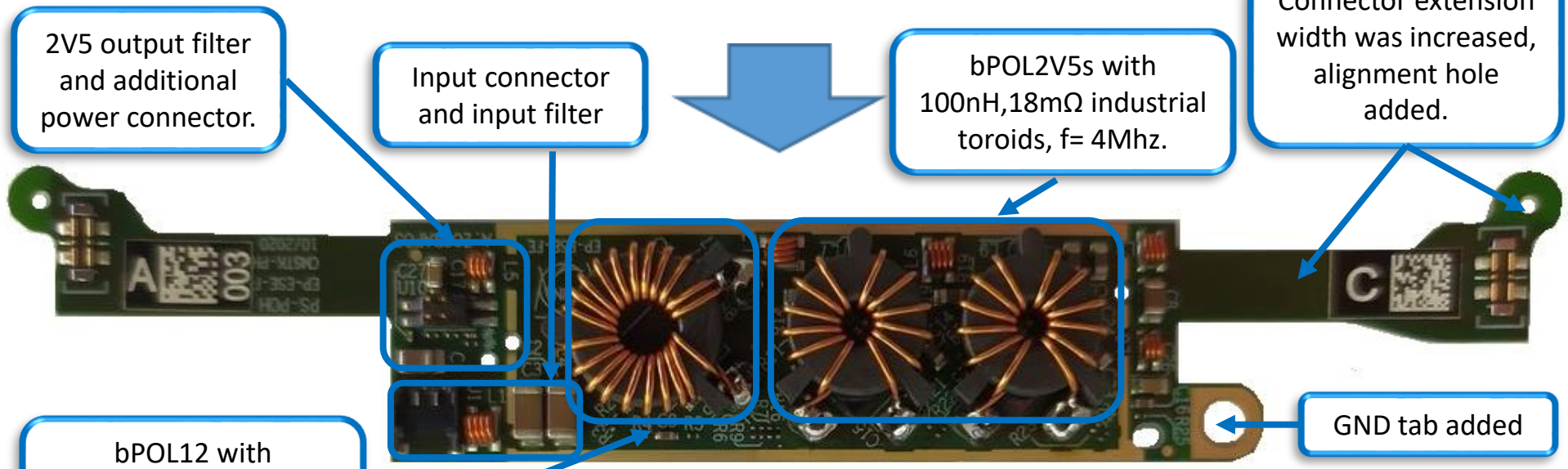


PS-ROH V2 is an FR4 stiffened prototype in order to validate the design changes before the pre-production. Assembly of these circuits was recently completed and validation is ongoing. V2.1 will be the pre-production version.

The PS-POH current version is the second prototype, one previous prototype was made by Aachen.



PS-POH V1 prototype, designed and tested by Aachen.

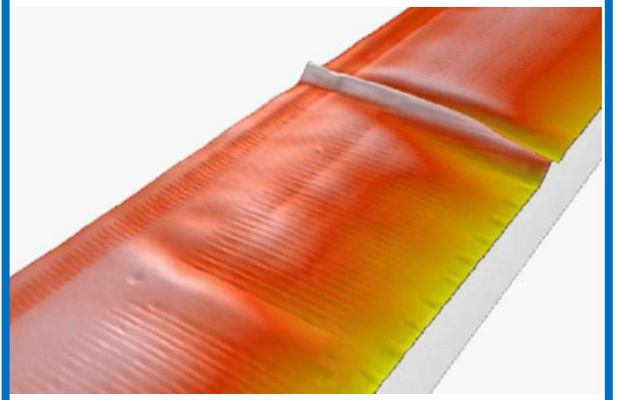


PS-POH V2 prototype, with the latest design updates from CERN.

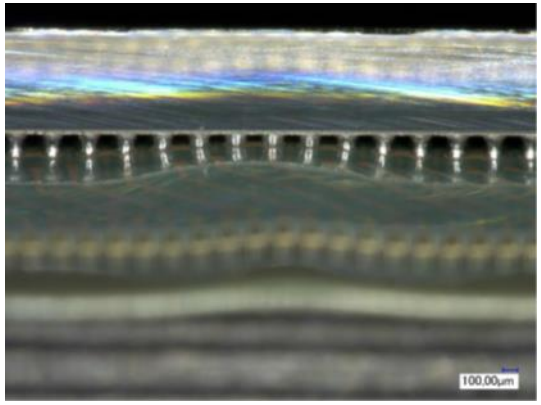
More details: https://pos.sissa.it/370/059/pdf and https://indico.cern.ch/event/1019078/contributions/4444400/

3. Issues discovered during the prototype production

Soft adhesive

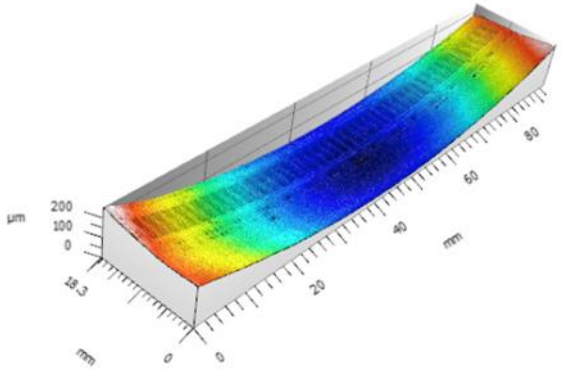


Wave formed during the reflow of a PS-MCK circuit due to insufficient adherence of the soft glue

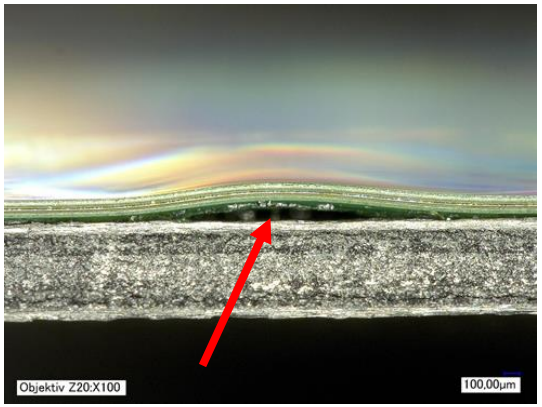


Any surface non-flatness causes partial or catastrophic failure in the flip-chip assembly

Hard adhesive

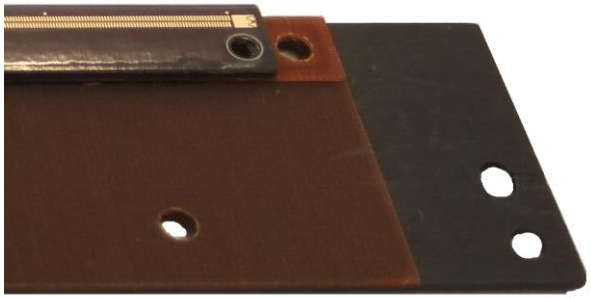


Bow formed due to the CTE mismatch of the flex substrate and the CF stiffener

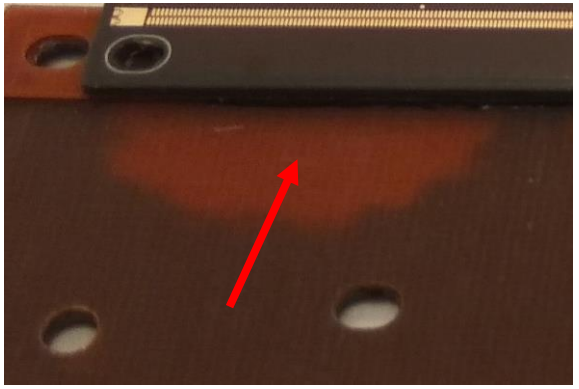


Delamination formed by “popcorn effect” due to insufficient drying of the CF stiffener laminates

Hard adhesive with compensator

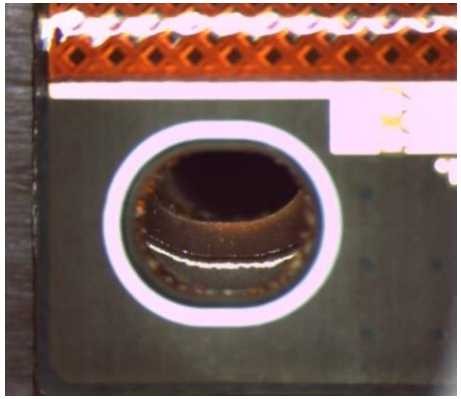


Polyimide-glass CTE compensator laminated on an 8CBC3 circuit with extended dry cycle.

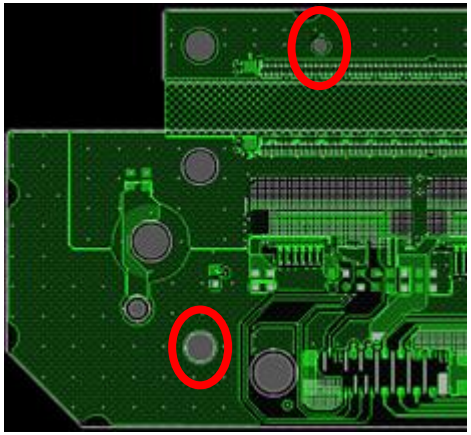


Compensator can delaminate as well during the reflow soldering if the assembly is exposed to ambient for even few hours

Blockage of alignment holes



Alignment hole blocked by misaligned internal layers or adhesive leakage



Solution: New alignment holes to be used during the lamination process

Circuit stretch after CF lamination

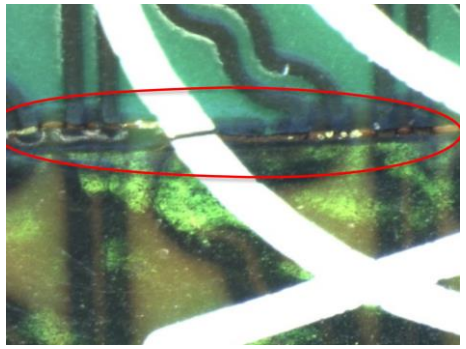
Object	Av. dev.	RMS
PS-FEH	140 µm	23 µm
2S-FEH	147 µm	22 µm

On average the wire-bonding array was 140 -147 µm longer than nominal after the CF lamination. Solution: Gerber data will be scaled.

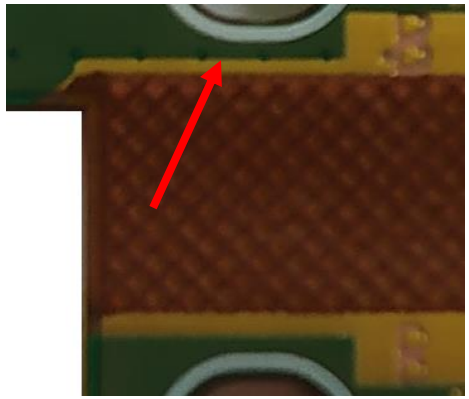
Elevated noise in case of floating CF stiffener

Solution: gold plated aluminium inserts are press fitted into the CF stiffeners and connects them to the hybrid's GND

Soldermask – coverlay transition cracking



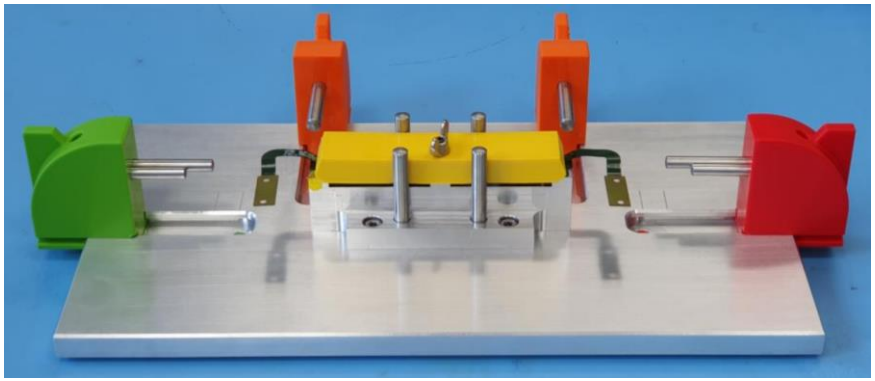
Crack in the soldermask in the transition zone between soldermask and coverlay



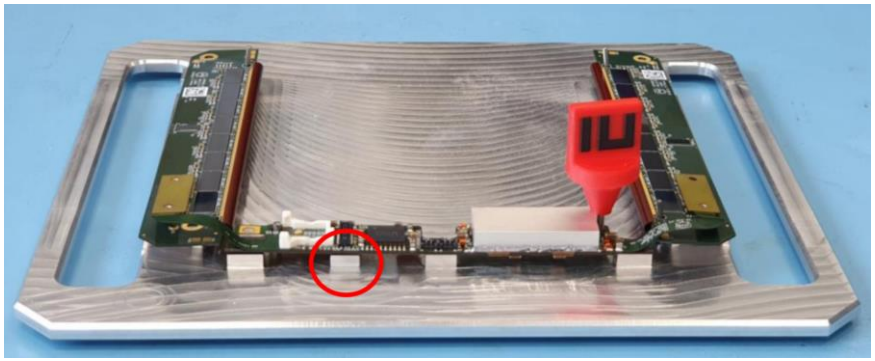
Solution: Plated transition zone between coverlay and soldermask next to the bend-zone

3. Performance of 2S module prototypes from current prototypes

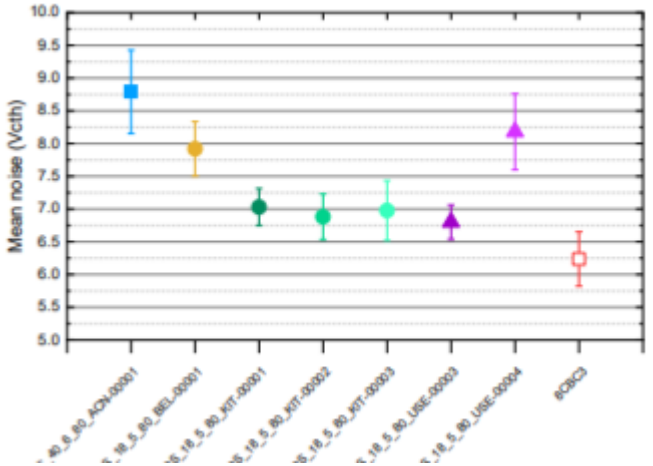
Several module prototypes were built at different assembly centres. Modules are fully functional, powering, communication and control works as intended. Noise level is slightly higher than expected, investigation is currently on-going.



2S-SEH pre-bend tool in operation



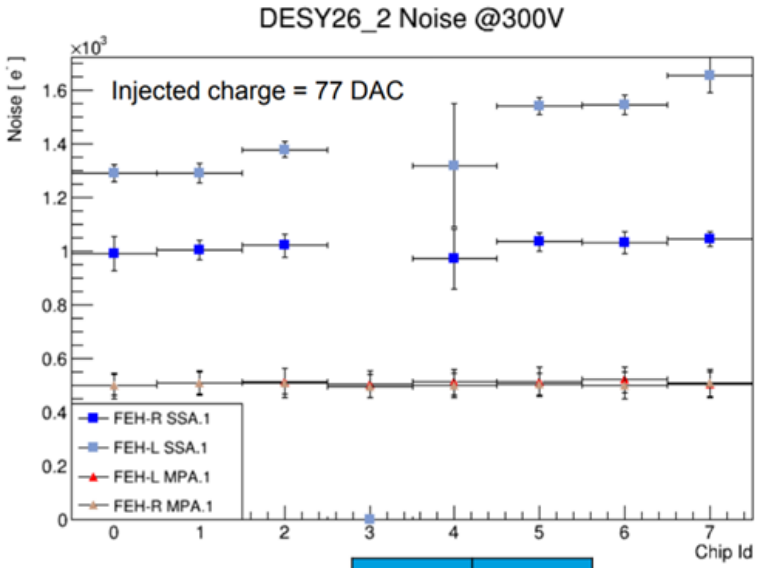
2S skeleton being assembled for a module



Noise levels measured with new 2S-modules. Expected noise level from simulations is 1000 e (6.41 Vcth). 1Vcth = approx. 156e

3. Performance of PS module prototypes from current prototypes

There is a smaller number of PS modules constructed compared the to 2S modules. Modules are fully functional, powering, communication and control works as intended. The noise level in PS modules is also slightly higher than expected. Thermal performance and noise performance in the detector structures are under investigation.

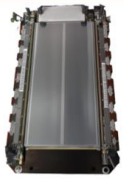


	MPA	SSA
1 ThDAC	94	250
1 CalDAC	220	243

DAC to electrons conversion table

Expected noise level for SSA: 800e
Current noise level of SSA: 1000e – 1500e

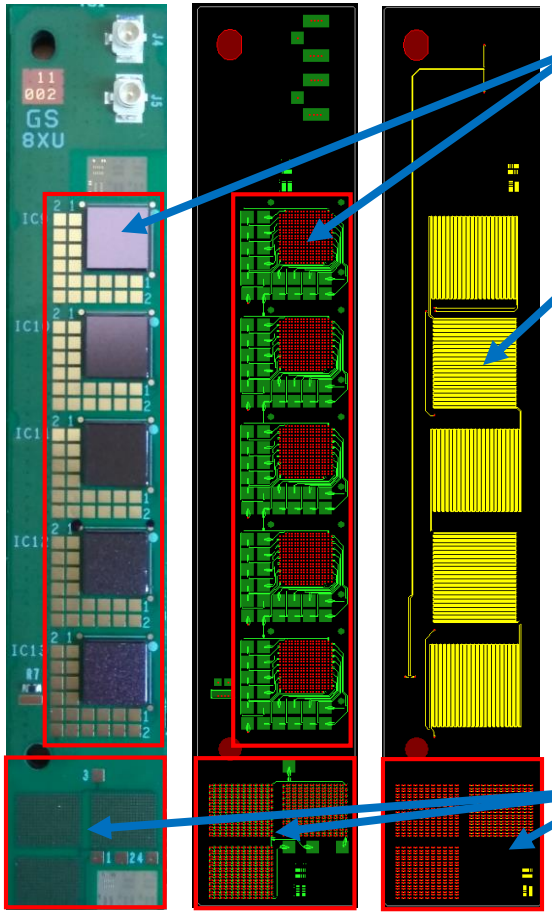
Assembled functional modules

	DESY26_1	DESY26_2	DESY40_3
Module			
ROH	ROH-v1, lpGBT-v0	ROH-v1, lpGBT-v0, (I2C patch)	ROH-v1 - lpGBT-v0
POH	POH-v2	POH-v2	POH-v2
FEH-L	—	CIC1, SSA1, MPA1	CIC1, SSA1, MPA1
FEH-R	CIC2, SSA1, MPA1	CIC1, SSA1, MPA1	CIC1, SSA1, MPA1
Status	Damaged	Functional	Work in progress

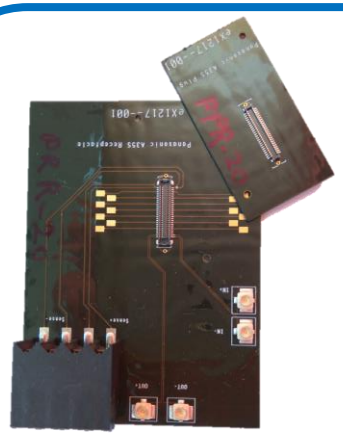
DESY. | System Test Meeting | 04.11.2021 | Younes Otarid 2

Current PS modules constructed or being constructed

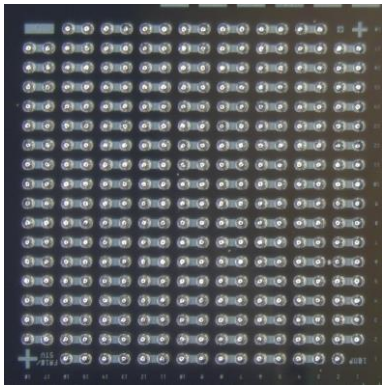
One of the test coupon geometry used



Flip-chips with SAC305 bumps.



Connector test coupons.



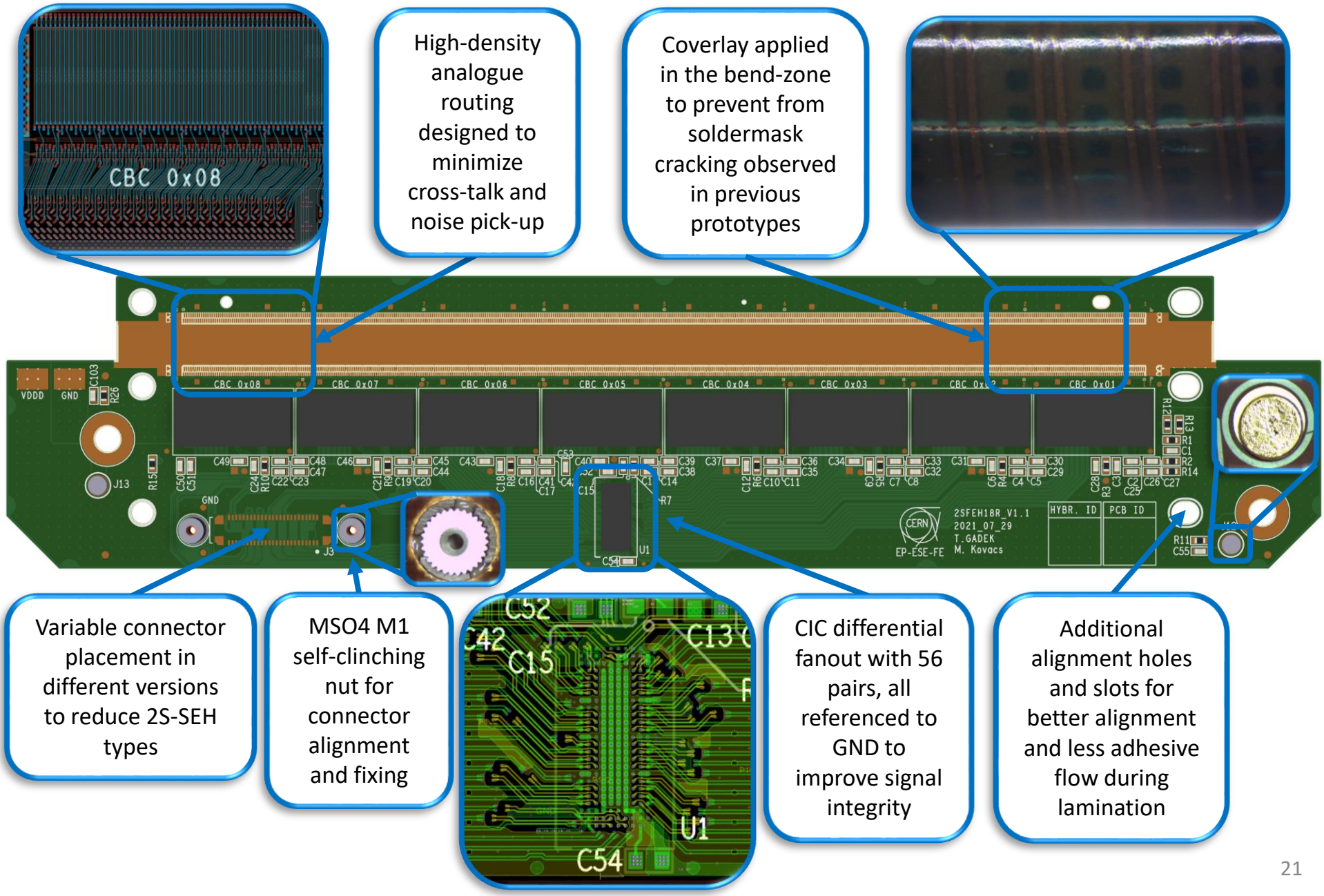
Daisy-chain test flip-chip with 254 µm pitch.

Key points:

- Irradiated samples @ 1MGy
- 1000 thermal cycles from -35 °C to 65 °C, max 7 °C/min slope.
- No via failures, no fine line failures were detected.
- Only very bad quality flip-chip assemblies failed after 1000 cycles.
- HDI circuits and Flip-chip technology are robust.

More details: https://pos.sissa.it/343/146/pdf

4. 2S-FEH design for pre-production



4. 2S-SEH design for pre-production

Long flexible tails to guarantee connection to FEHs

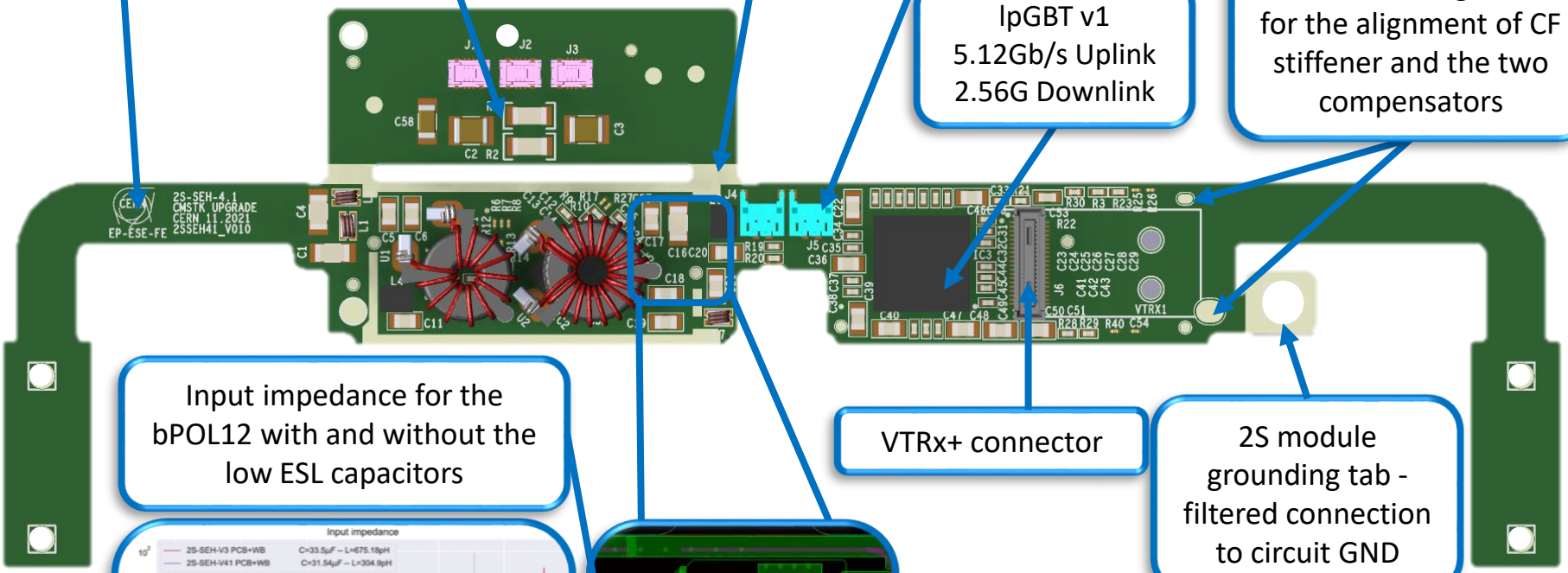
HV circuitry and temperature probe connectors in fold-over zone

Optimized location of flexible zone for the fold-over

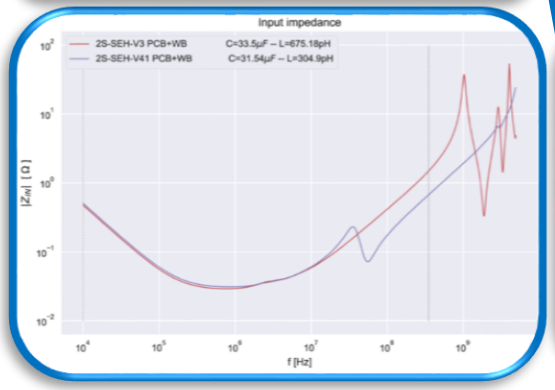
Input LV and HV connectors

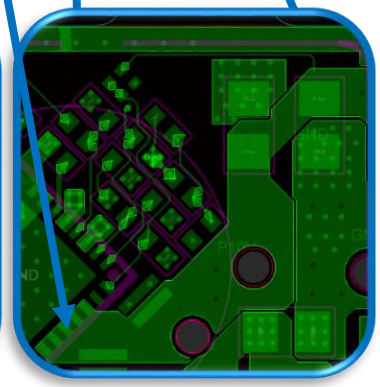
lpGBT v1
5.12Gb/s Uplink
2.56G Downlink

Several tooling holes for the alignment of CF stiffener and the two compensators



Input impedance for the bPOL12 with and without the low ESL capacitors

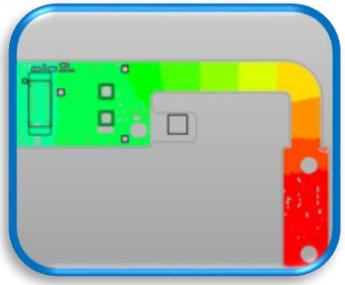




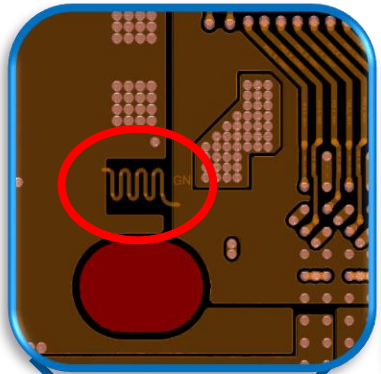
VTRx+ connector

2S module grounding tab - filtered connection to circuit GND

Power integrity simulations for performance optimization



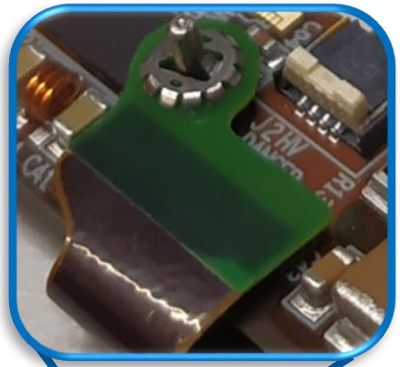
4. PS-FEH design for preproduction

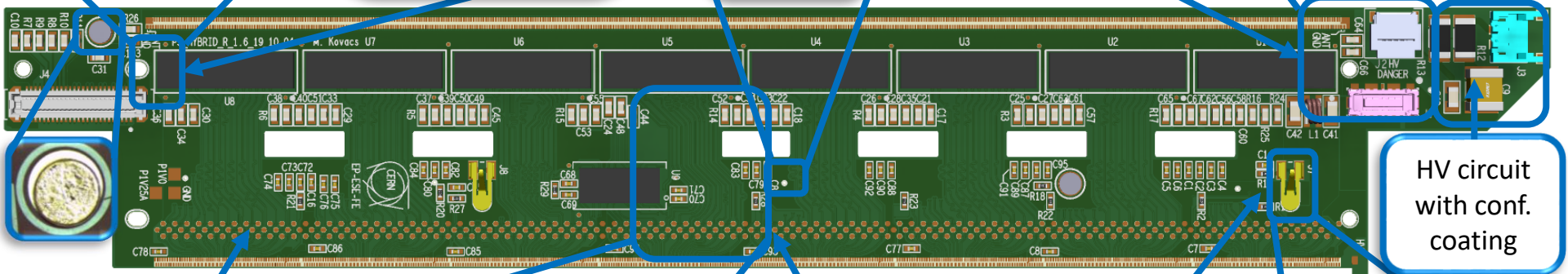


GND plane under analogue part of the front-end ASICs is isolated with resistive and inductive connection to reduce DC drop and noise coupling

Spacer air-pocket vent holes

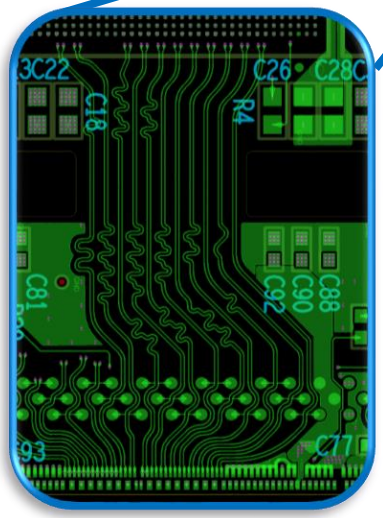
Locking insert fitting in the 1 mm alignment hole can be installed to secure the power connector in place





HV circuit with conf. coating

The POGO connector pattern provides connection for all the SSA output and MPA input signals, providing a full-scale functional testing

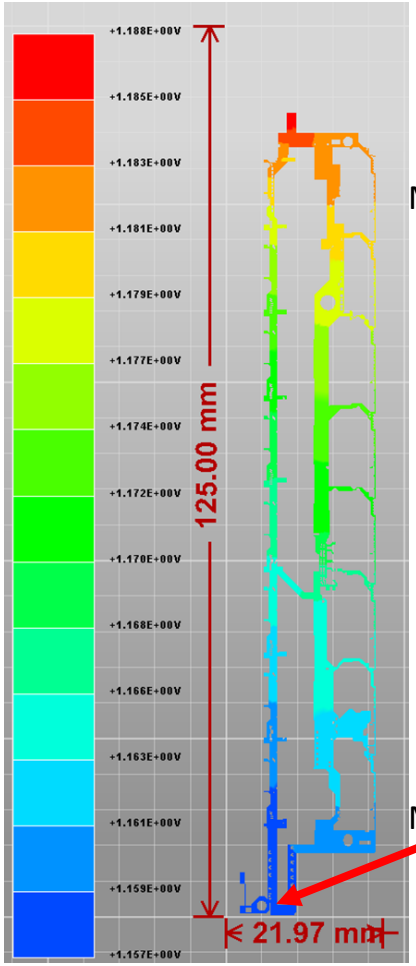


SSA to MPA interconnection is fully length match in order to assure maximum signal quality

Spring connectors are installed on the hybrids in order to provide sufficient GND connection for the CF structures

DC drop simulations were made on the prototype design:

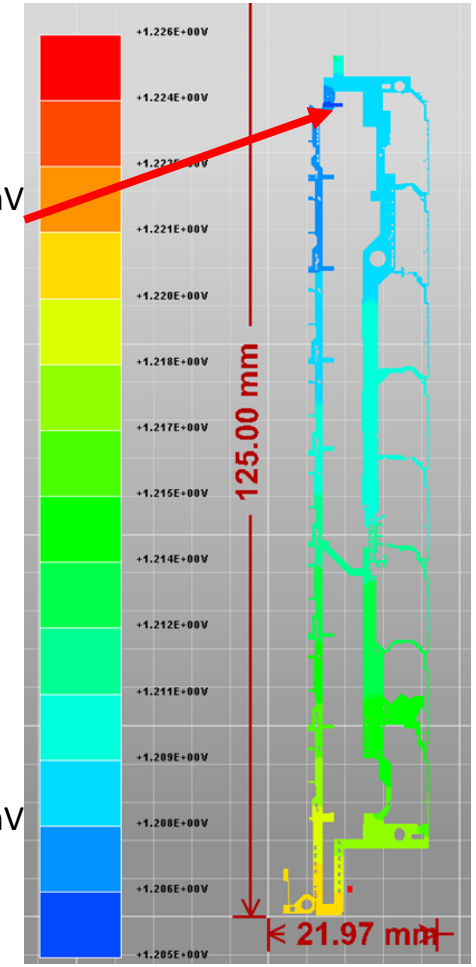
- The simulation results concluded in a change in the powering scheme for 1.25V



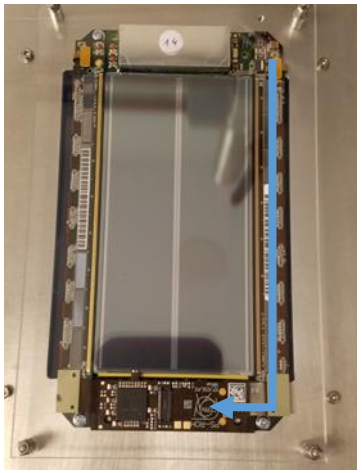
Voltage drop on the 1.25V rail of PS-FEH-R, original scheme

Max 45 mV drop

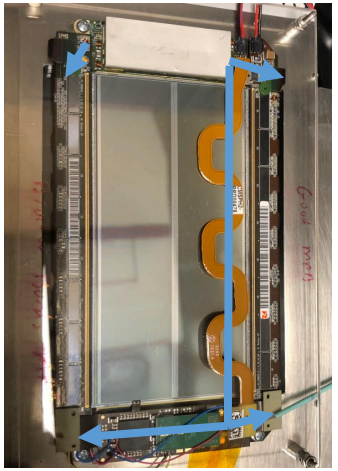
Max 93 mV drop



Voltage drop on the 1.25V rail of PS-FEH-R, updated scheme

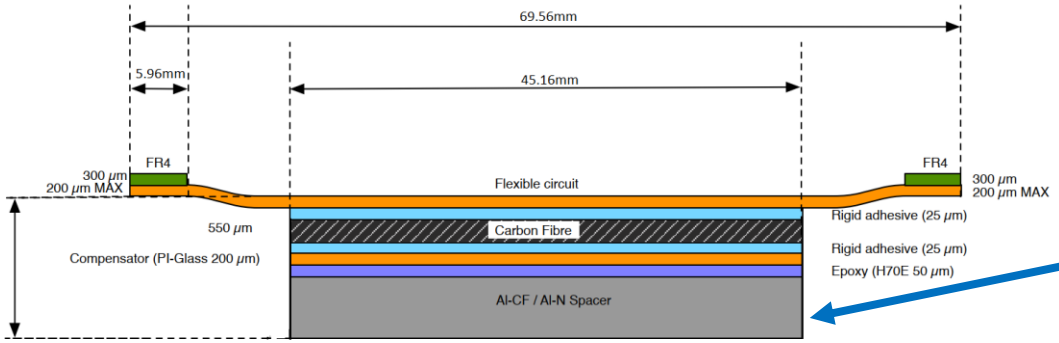


Original current flow scheme for 1.25V



Updated current flow scheme for 1.25V

4. PS-ROH design for pre-production

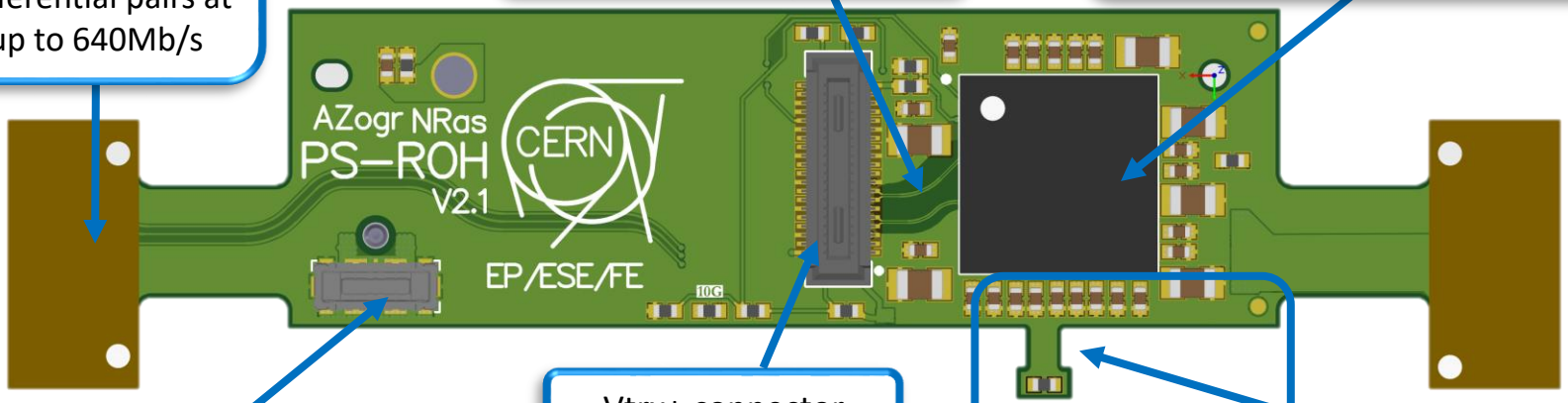


ALN spacer different height for each PS module variant

lpGBT v1
5.12Gb/s or 10.24Gb/s Uplink
2.56G Downlink

Flexible tail with single ended and differential pairs at up to 640Mb/s

100 Ohm differential pairs up to 10.24Gb/s



Vtrx+ connector

WP-10 power connector for 1V25 directly from the PS-POH

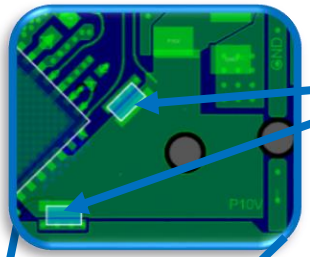
PS-POH to PS-ROH tail

Thermistor – Glued on top of sensor

4. PS-POH design for pre-production

PS module GND tab – filtered connection to circuit GND

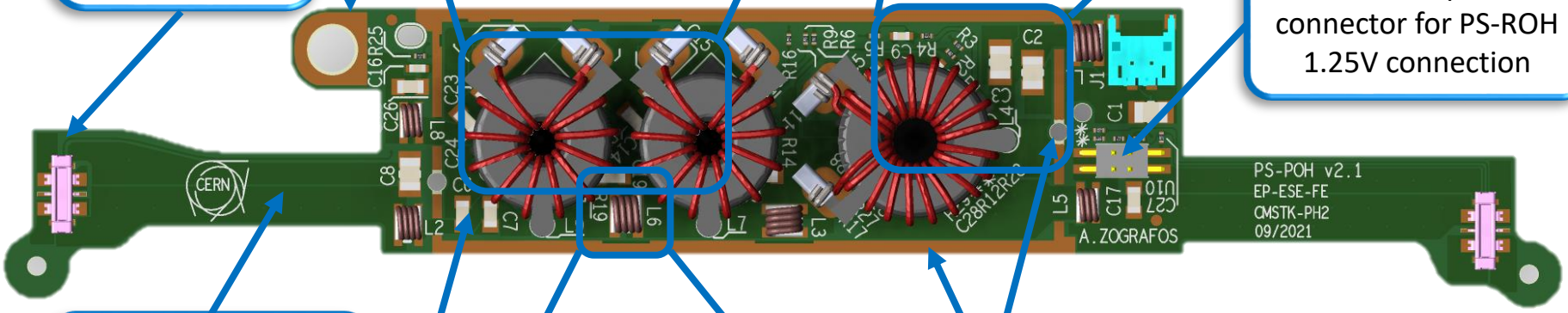
Thermally conductive paste placed on top of coils before shield assembly



Low ESL capacitors at input of bPOL12

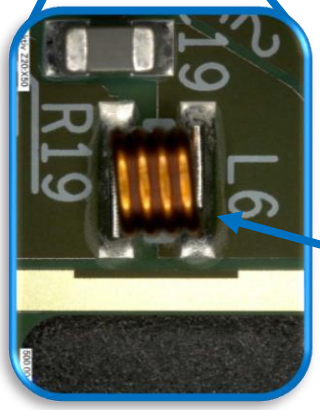
Remote sensing at connectors for 1V25 and 1V05 rails

Additional power connector for PS-ROH 1.25V connection



Long flexible tails to adapt to all PS module variants

Shield soldering pad and alignment holes

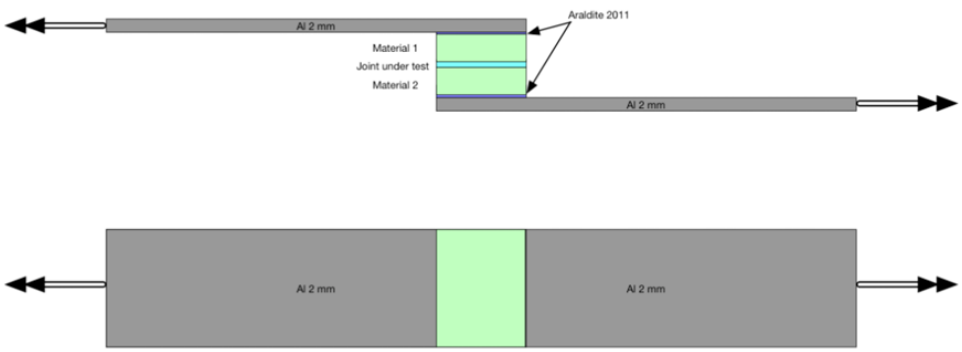


Output/Input pi filter capacitors in opposite facing pairs

Conformal coating in critical areas to avoid shorts with shield

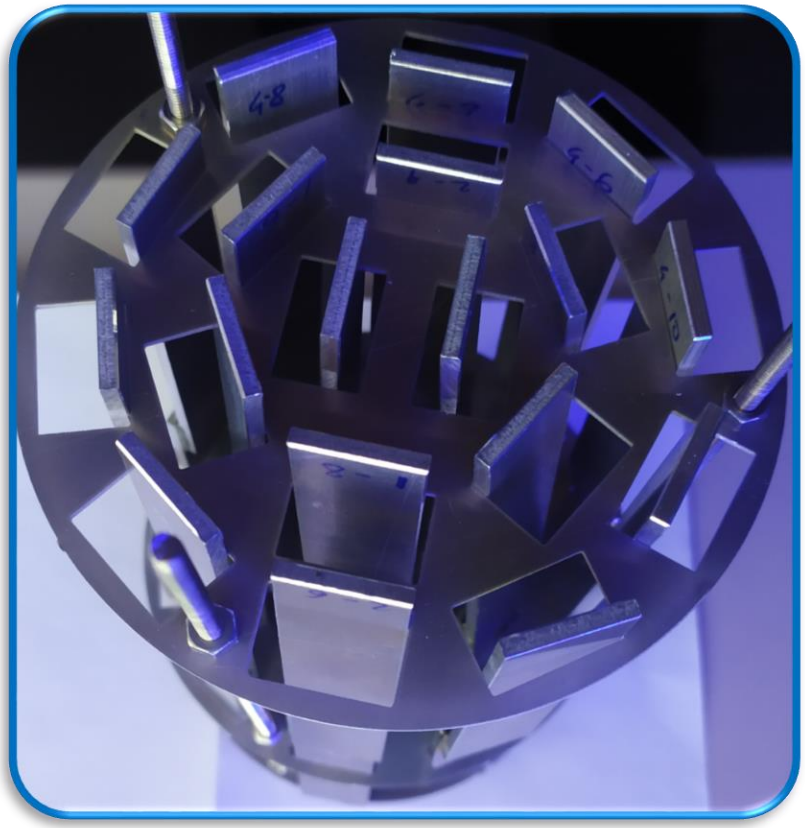
Custom micro-milled Aluminum shield

- A test plan was created to test the radiation tolerance of all the materials used in the hybrids. Test is focusing on the adhesives and the circuit substrate,
- Shear tests will be done before and after irradiation of samples. Irradiation dose will be 1MGy at 6kGy/h.



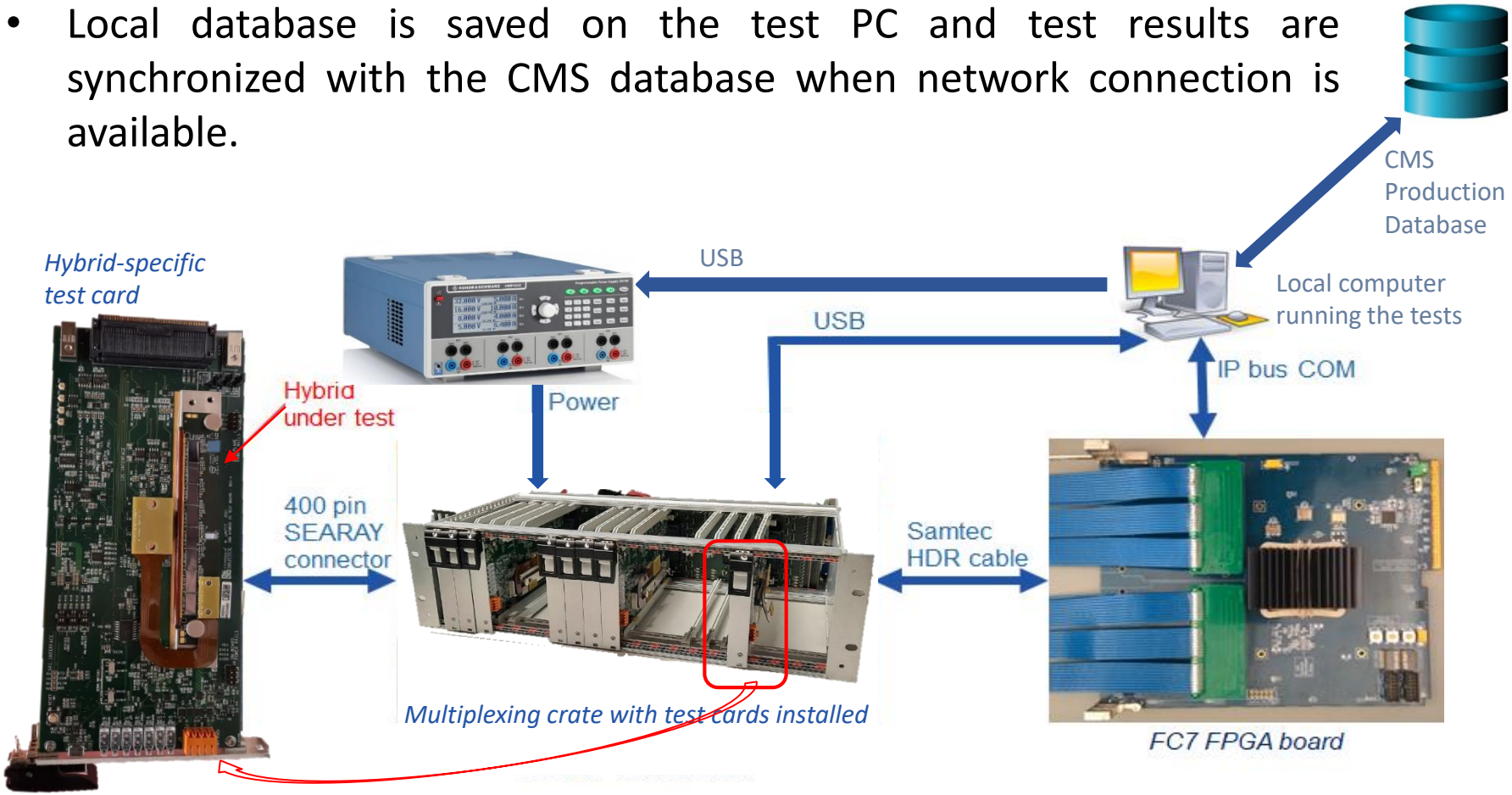
Standard size shear test samples will be used

- Materials tested:
- H70E epoxy, Prepreg, EP48TC thermal epoxy, TNP400 and semicosil for PSFEH fold-over, Nitto adhesive proposed for 2S-SEH fold, Therm-a-Gap GEL30 silicone based thermal paste.
- Flex stackup, carbon fibre laminates, AlN spacers, underfills, conformal coatings.



Samples ready for the irradiation in the research reactor in Zagreb

- A crate based test system was designed in order to provide a platform for the hybrid testing. It is based on a high-speed multiplexer backplane.
- Three backplanes can be mounted in one crate, 12 test card can be inserted.
- Test peripheries are controlled over USB and IOs of the FC7 FPGA board.
- Local database is saved on the test PC and test results are synchronized with the CMS database when network connection is available.



More details: Hybrid test system presentation by Irene and https://pos.sissa.it/370/082/pdf

FPGA – Field Programmable Gate Array

- Common GUI is developed for the testing of all hybrid types. Details are hidden from the operator. Test results are indicated in good/bad format.
- GUI takes care of system scan, firmware and software selection, control of the power supply.

Test PC

GUI and Test Manager

Test procedure in Phase-2 ACF

Testcard driver

Control of peripheries and functionality of the selected test card over USB

Communication with FPGA via IPBus protocol: Control and data

Backplane

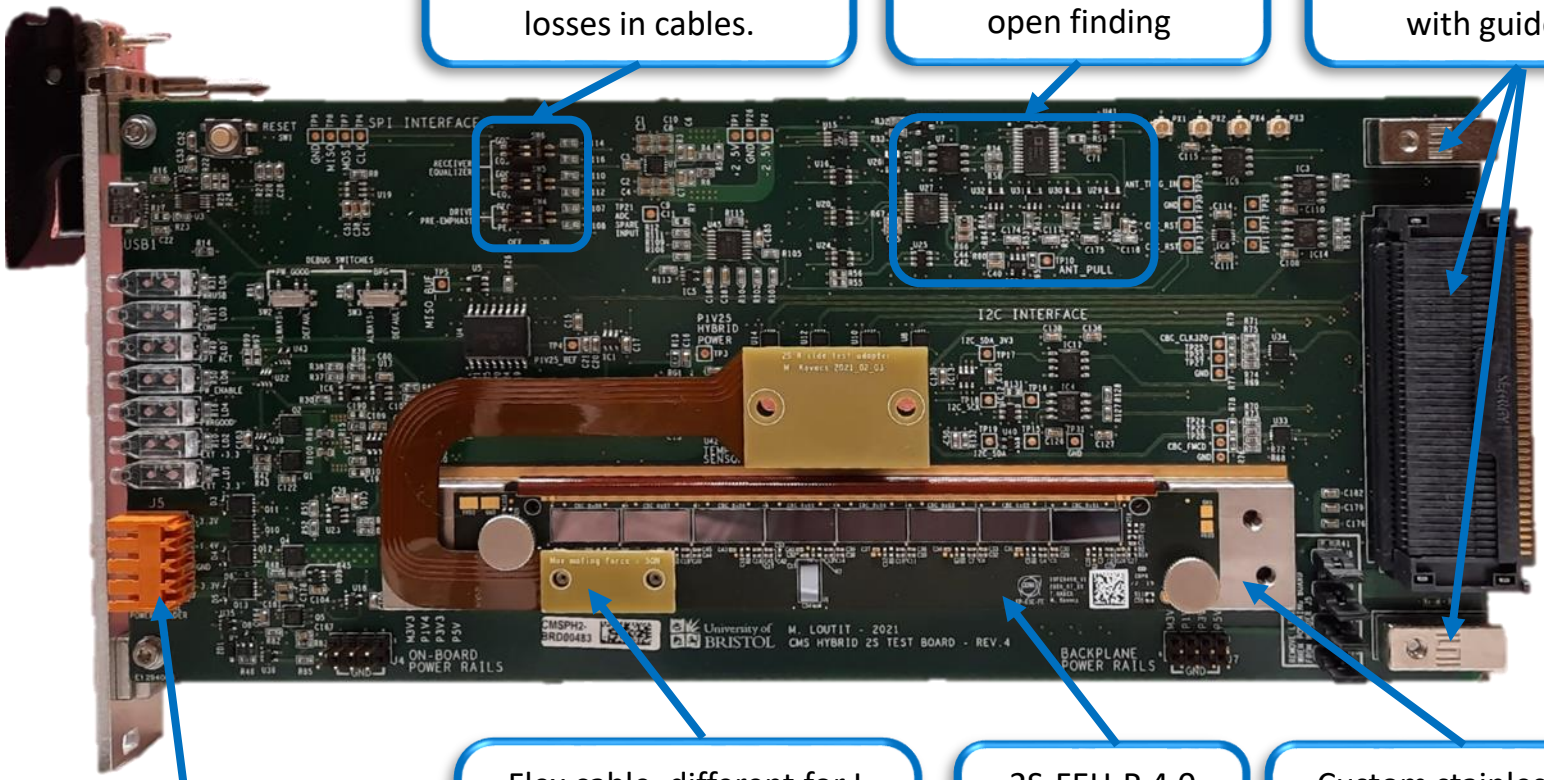
FC7

Test card specific firmware

GUI – Graphical User Interface

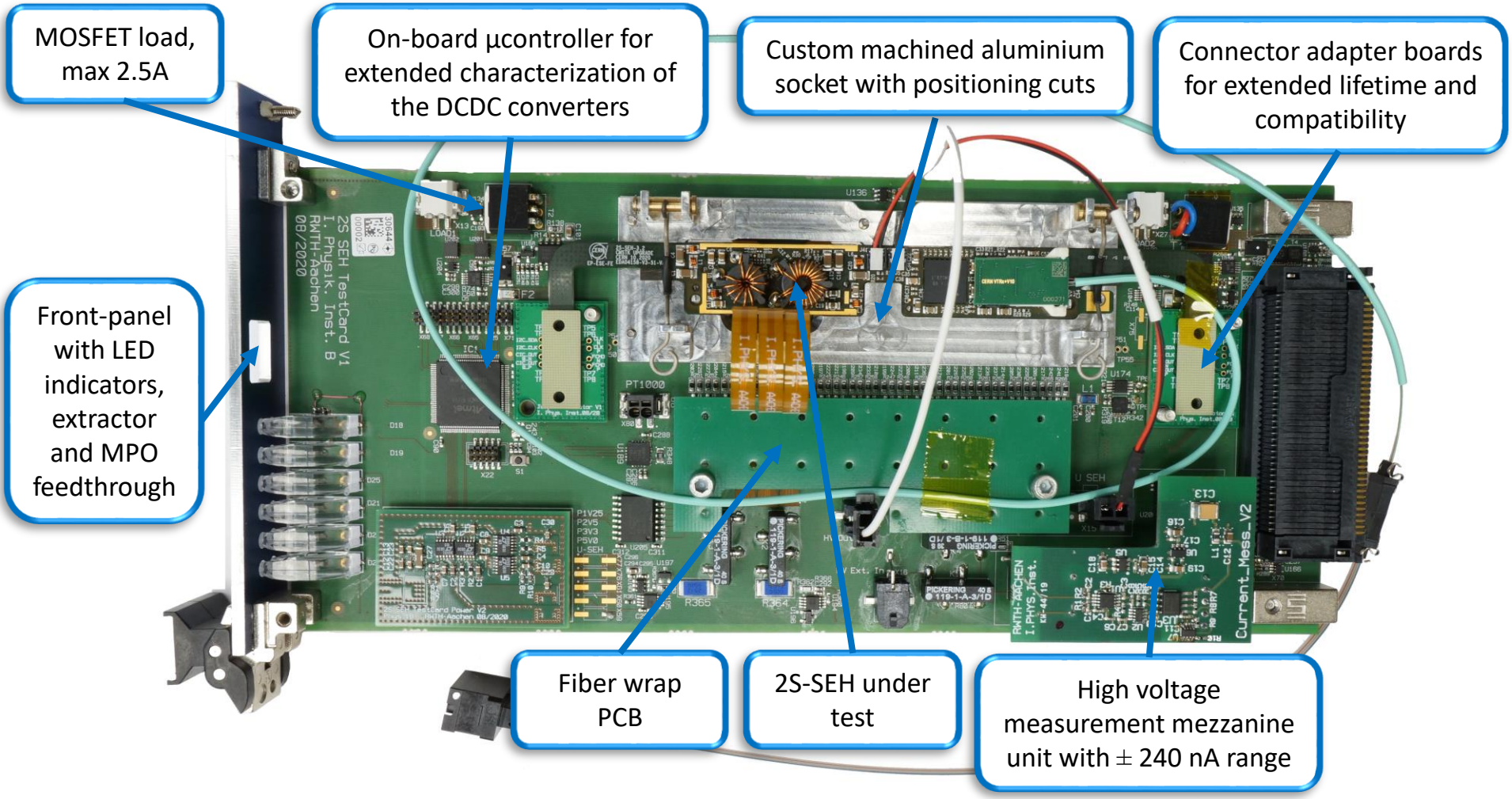
ACF – Acquisition & Control Framework

- Digital tests: All digital communication of the ASICs, I²C lines, CLK, Fast command, Reset lines. Tests can be done at different supply voltages tuned by on-board LDO.
- Analogue tests: Supply voltages and consumption, temperature, CBC inputs for shorts and opens.



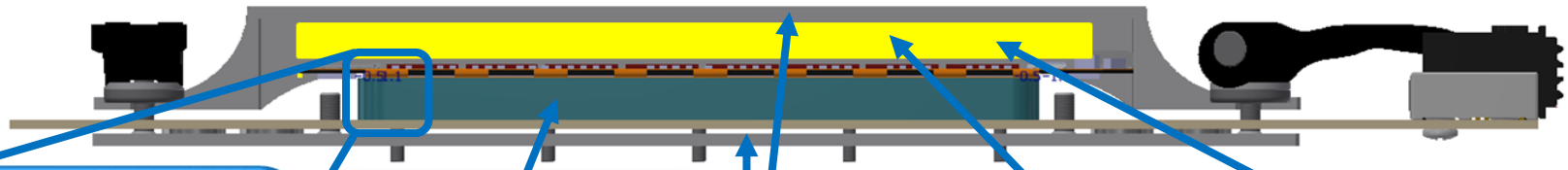
LDO – Low Dropout Regulator

- Test card allows for full digital testing of the LpGBT and VTRx+ communication. Performance of the DCDC converters can be fully characterized (efficiency, setup time, voltage levels). HV leakage can be measured as well. Design by RWTH Aachen.



More details: https://indico.cern.ch/event/1019078/contributions/4444307/attachments/2310365/3931469/poster-93.pdf

5. PS-FEH test card



POGO socket with 300 test points are connecting to the SSA outputs and CIC inputs

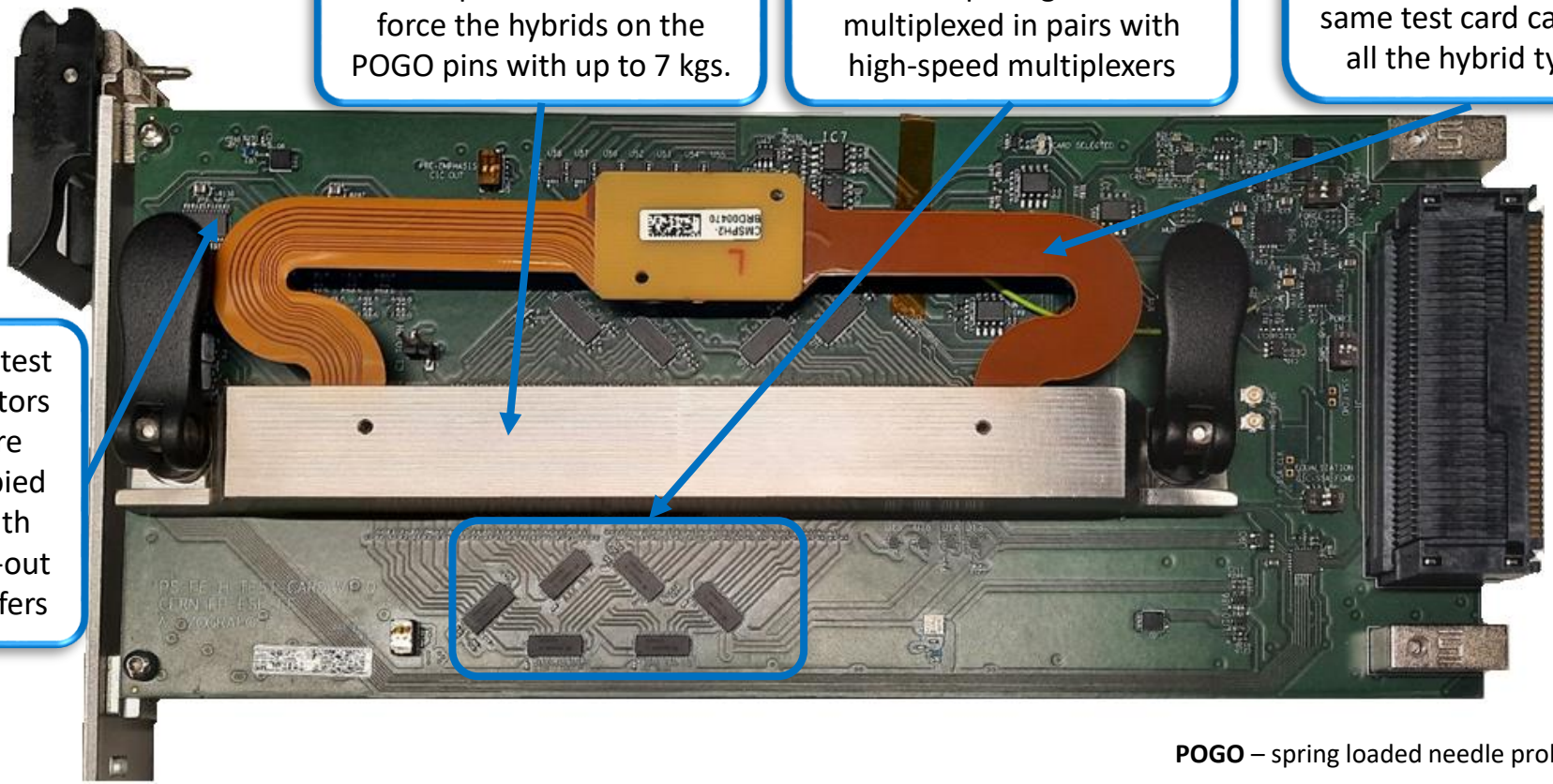
Custom made plastic pusher is pressing the hybrid on areas without components.

Flexible connectors are designed for the L and R hybrid types. The same test card can host all the hybrid types.

Press plates are used to force the hybrids on the POGO pins with up to 7 kgs.

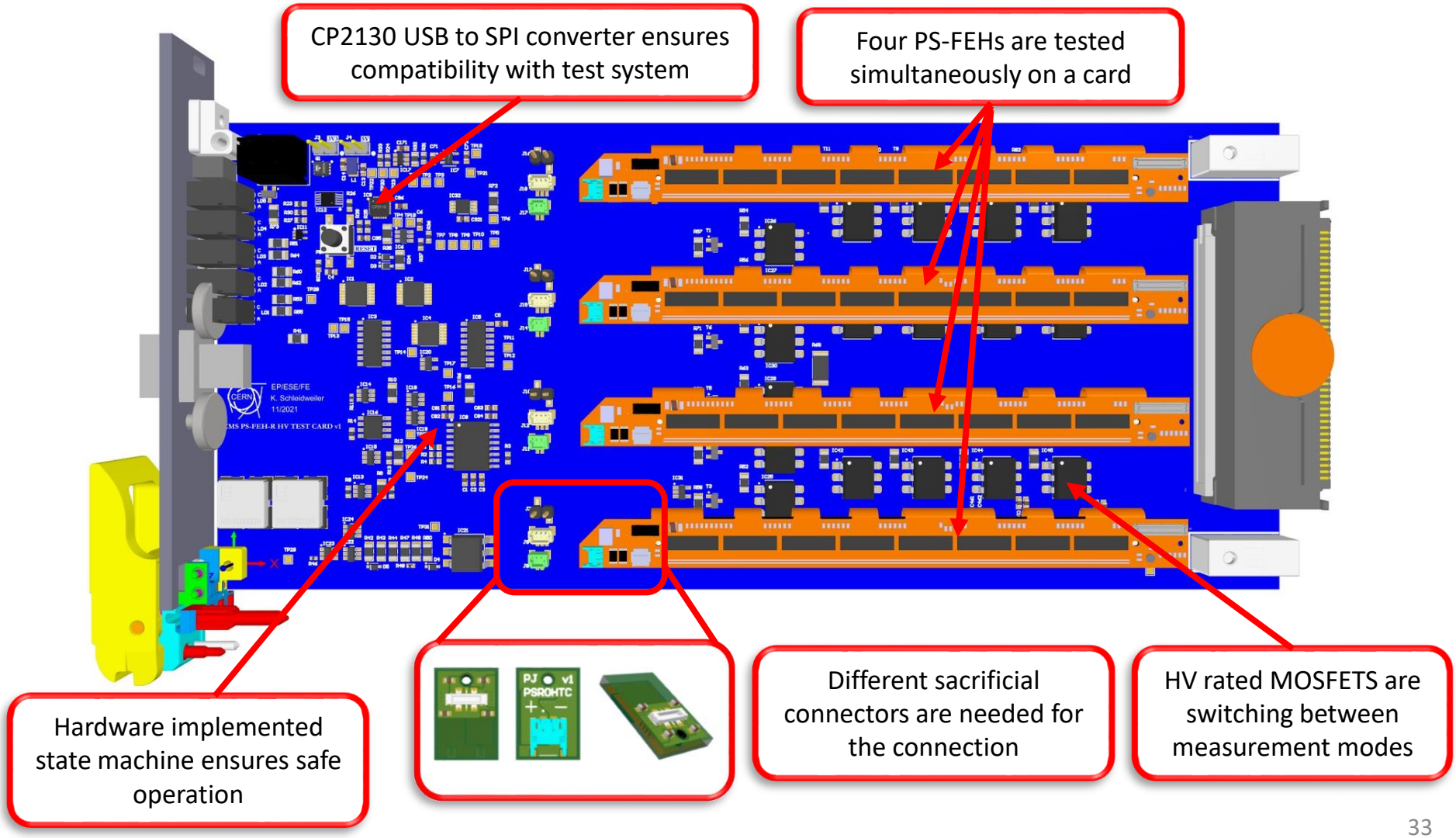
SSA output signals are multiplexed in pairs with high-speed multiplexers

CIC test vectors are copied with fan-out buffers



POGO – spring loaded needle probe

- HV test could not fit in the PS-FEH test card due to the complex geometry needed to press the hybrid on the POGO socket. Routing and fitting of components were also difficult. A separate test card is being designed to carry-out the HV test.

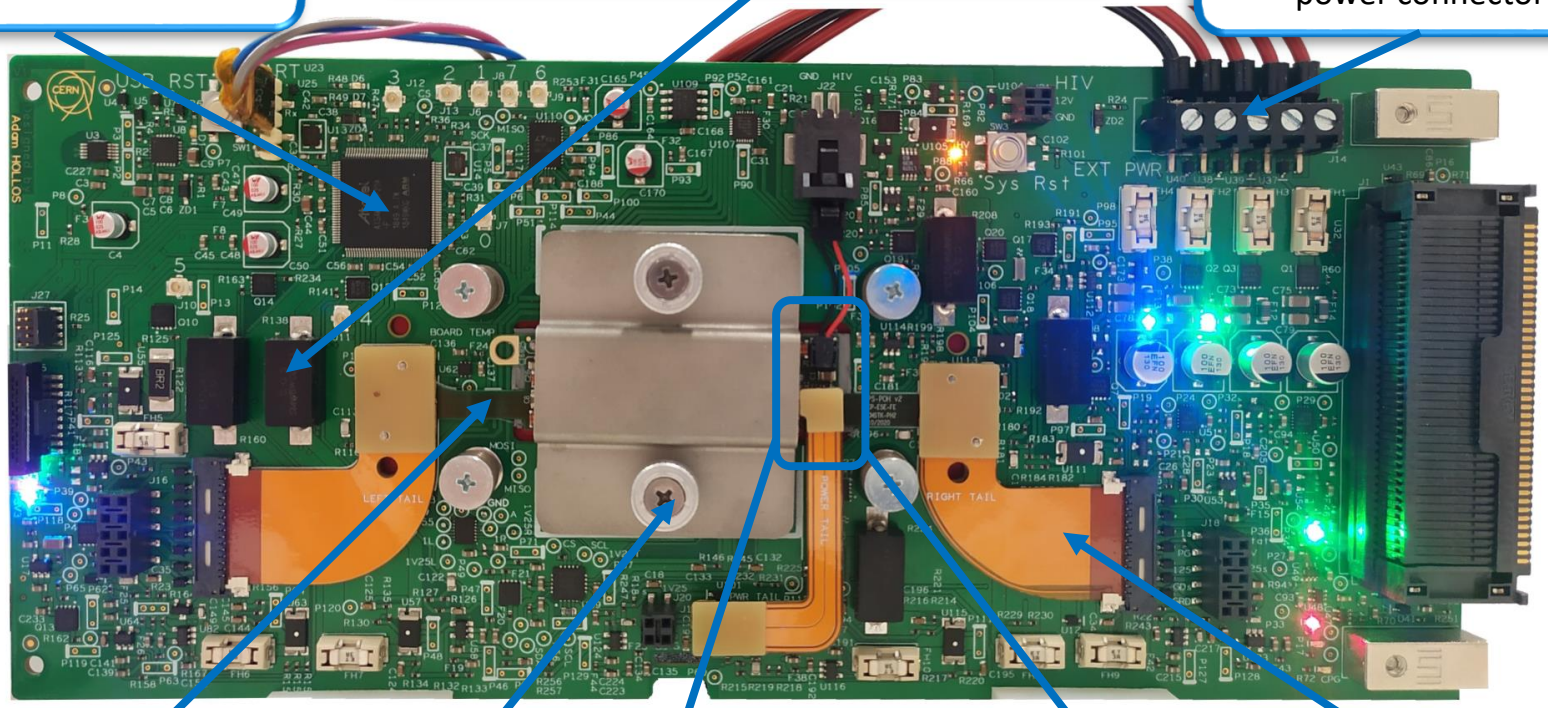


- Test card allows for very precise characterization of the DCDC converters. Measurements: Efficiency, output voltage, output ripple, temperature, setup time.

On-board µcontroller for extended characterization of the DCDC converters

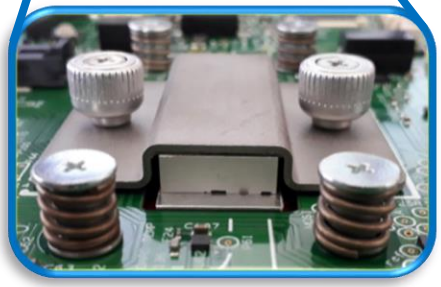
MOSFET and resistor in series to optimize the heat load of the MOSFET.

Standalone operation with the usage of external power connector



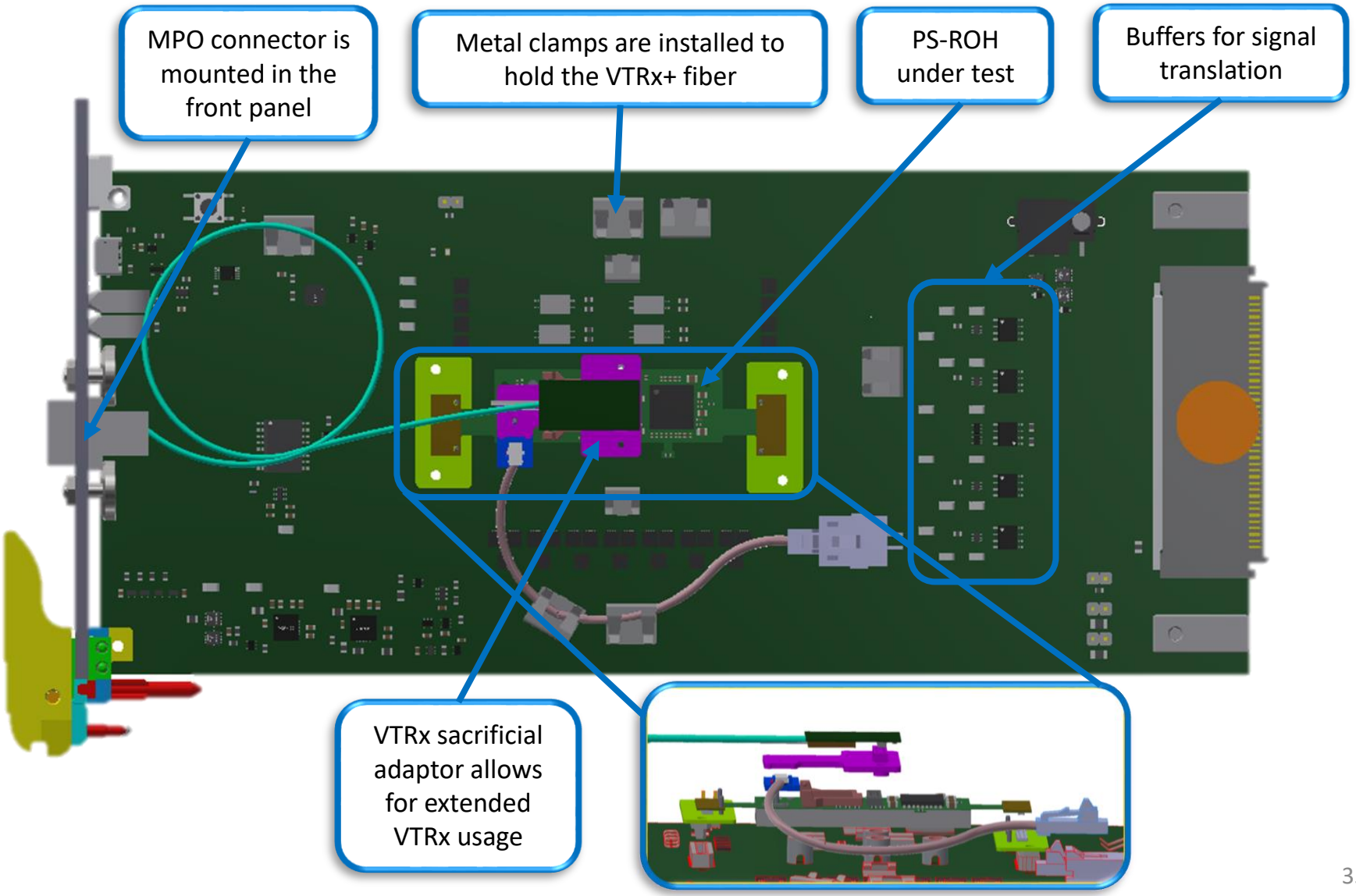
PS-POH under test

Special pressure limiting screws are used to tie down the pressure plate



Flexible sacrificial connections to extend the lifetime of the board and compatibility

- Test card allows for the testing of the digital IOs and fusing of the LpGBT. Functionality of the connectors and the VTRx+ are tested as well.



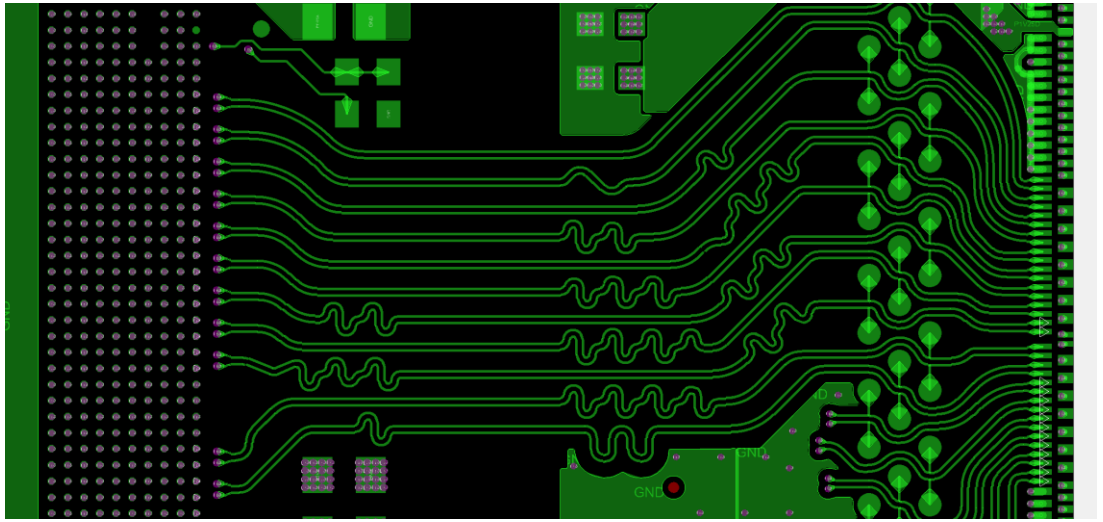
- The test system was used to test all the prototype hybrids. Test procedures were developed with the prototypes.
- A cold test plan was set-up and currently in progress to validate the operation of the system in cold.
- Currently more than 300 thermal and mechanical cycles are done. No failures were developed during the tests apart from the initial bugs identified.

Stage 1	Operation at -35°C with single backplane V1 and single test card.
Stage 2	Operate at -35°C with all hybrid types: 1 test card per type.
Stage 2.5	Operate full crate at -35°C with available test cards.
Stage 3	Operate full crate at -35 °C : test with 3 backplanes with 12 test cards (3 of each type).
Stage 4	Thermal cycling with full backplane.

Test crate in the climatic chamber during the cold testing

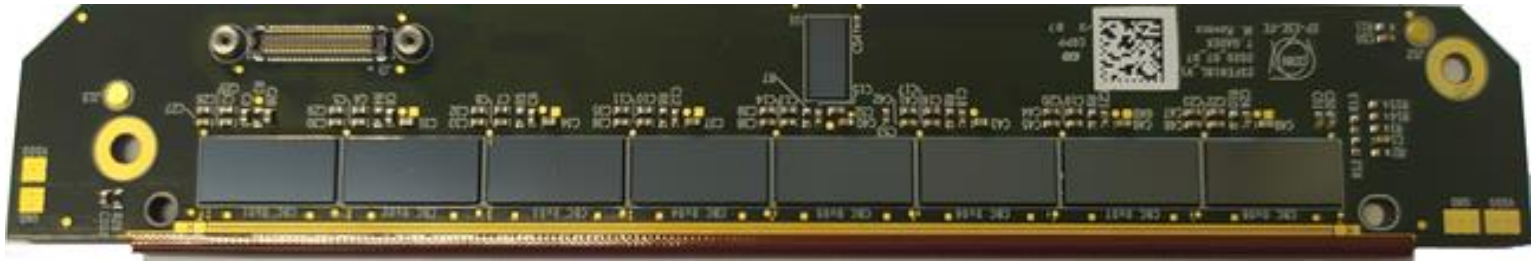
- Design for testability was a key aspect during the hybrid design phase. The first architecture of the PS module had the clock and FCMD distributed from the MPA.
- As the hybrid has no MPA during the test phase, the buffering was replaced to the SSA. Other test features were implemented in the SSA such as programmable test vectors on the serial outputs.

- The optimization of the SSA and MPA pinout was with high importance. Any of the IOs crossing would have made the design unroutable.



MPA and SSA interconnection was fully optimized in order to help the success of the hybrid design.

- Many hybrid prototypes were developed in the last 10 years. This activity was essential to reach the maturity of the designs and the manufacturing processes.
- Many issues were discovered during the prototyping phase. Most of these issues are resolved today and the hybrids are fully functional and ready for the pre-production.
- Module prototypes are being built from the hybrids. Mechanically and electrically the modules are functional and no major issues were discovered. Noise performance of the modules is slightly worse than expected problem is being explored currently.
- A crate based test system was developed for the production testing of the hybrids. Six test cards were (are) developed for the testing. The verification of the system is currently on-going. No major issues were discovered so far.
- Collaboration between ASIC design and hybrid design was essential during the design phase. The PS-FEH could not be designed without this level of optimization.
- Still a lot of work is ahead to arrive to the mass production of hybrids and modules, but we can see the light in the end of the tunnel!



Thank you for your attention!
Big thanks for the hybrid design team!

Davide Ceresa will continue with the ASIC details